Competitive Semiconductor Manufacturing

Program Update

Profs. Robert C. Leachman & David A. Hodges
Program Co-Directors
Engineering Systems Research Center
University of California at Berkeley

Agenda

- Introduction to CSM Program
- Technical metrics of fab performance
- Performance in economic terms
- Key practices underlying leading performance

CSM Program

- Since 1992, the largest interdisciplinary research program at Berkeley (10 faculty, 20 students from Business, Economics and Engineering)
- Fab performance benchmarking
- Focus studies (MS and PhD projects)
- 48 CSM reports may be ordered on the Web at

  http://euler.berkeley.edu/esrc/csm

Benchmarking fab performance

- 1992-96: Studied 29 fabs in USA, Japan, Korea, Taiwan and Europe under sponsorship of Alfred P. Sloan Foundation
- Mostly 6-inch wafer fabs (six 5-inch, two 4-inch) operating process technologies ranging from 10 micron down to 0.4 micron line widths

Benchmarking fab performance (cont.)

- New phase of study 1997 to the present sponsored by Sematech, SIRIJ/EAIJ, TSMC, UMC, Winbond, Samsung, Micrus, Cypress
- Fab lines running 8-inch wafers in 350nm technologies and below
- 7 lines studied to date, 7 more budgeted

Factory data collection

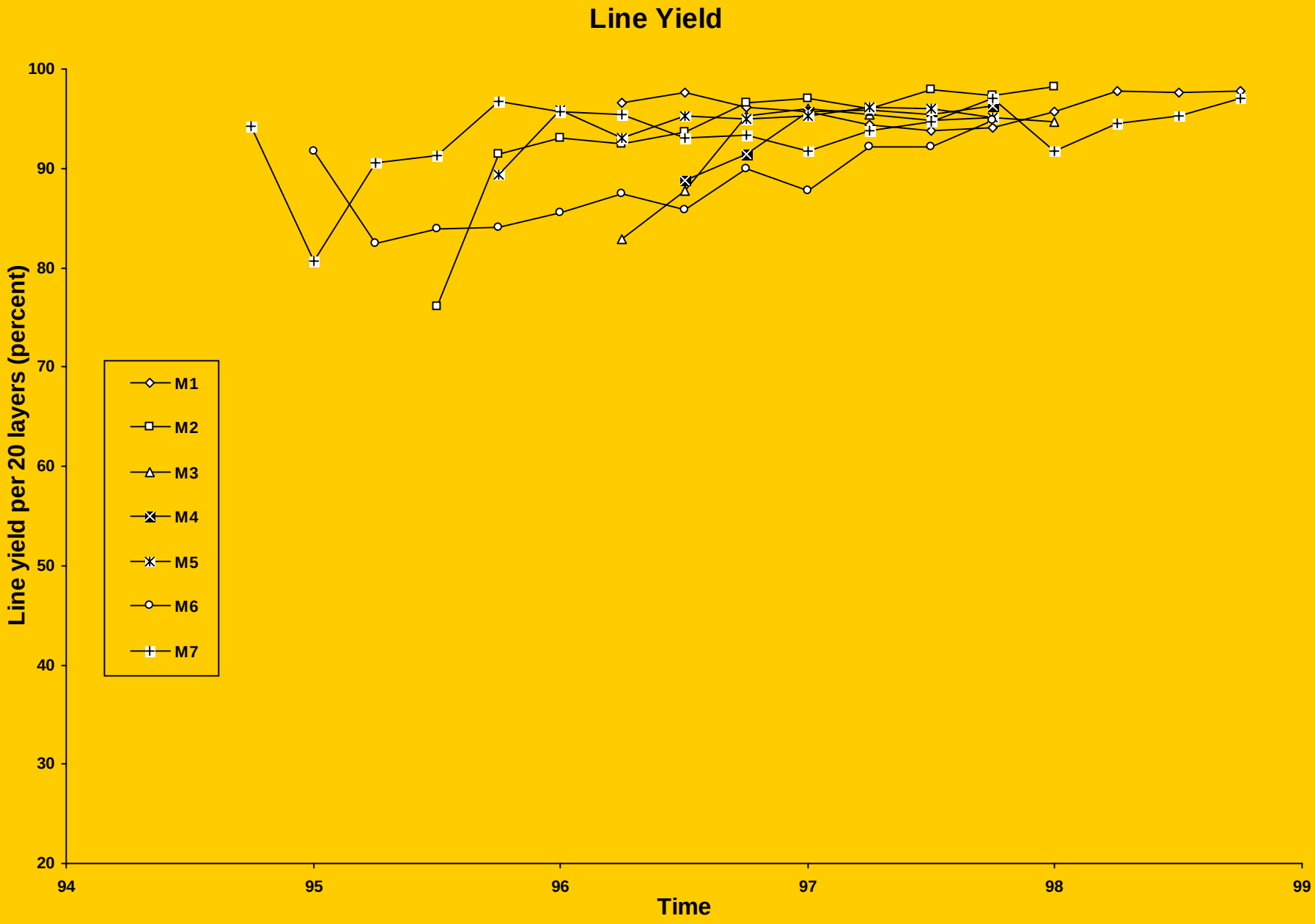
- Mail-Out Questionnaire (MOQ)
- 2-3 years of fab history (plus updates)
  - process technologies, production volumes, yields, cycle times
  - equipment and facilities
  - headcount and HR data
- We compute technical metrics from these data. Identities of fabs are kept confidential.

The “Berkeley metrics”

- Line yield per 20 mask layers **(LY20)**
- Defect density (die yield plugged into Murphy Model) **(DD)**
- Integrated yield (line yield times die yield) **(IYD)**
- Throughput of photo equipment (wafers processed per stepper per day) **(STP)**
- Integrated stepper throughput **(ISTP)**
- Direct labor productivity (wafer layers per operator per day) **(DLP)** and total labor productivity (wafer layers per headcount per day) **(TLP)**
- Cycle time per mask layer **(CTPL)**
- Process development and qualification time **(VT)**
- Time to ramp to mature die yield **(RT)**

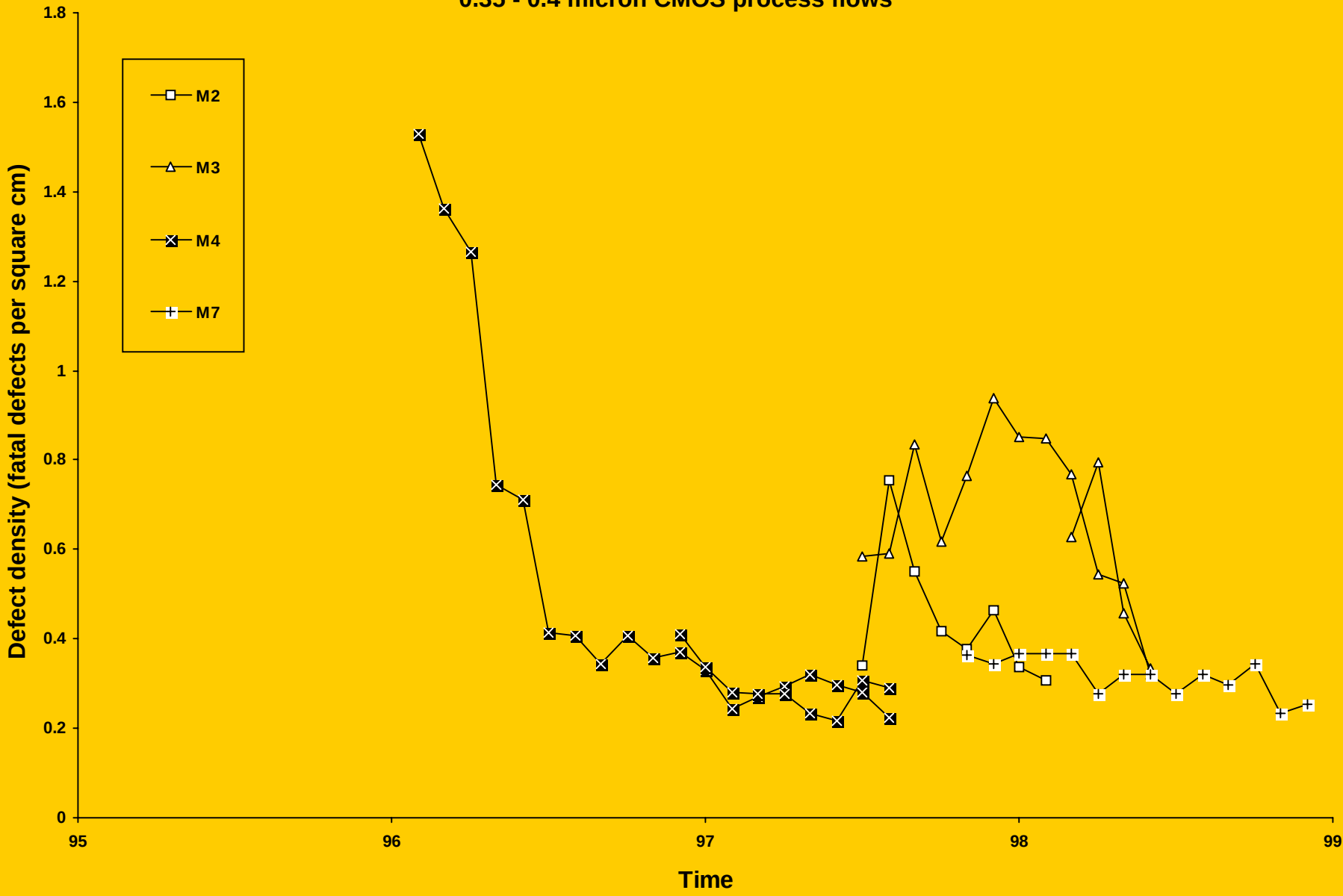
Performance benchmarks (8-inch)

- **LY20 = 98%** for both logic and memory
- **DD = 0.05** per sq cm for memory (after repair), **0.20** per sq cm for logic
- **IYD = 93%** for memory, **89%** for logic (assuming a 0.5 sq cm device area)
- **STP = 1,000** for logic, **600** for memory
- **ISTP = 800** for logic, **550** for memory
- **DLP = 85** for memory, **55** for logic
- **TLP = 55** for memory, **37** for logic
- **CTPL = 1.4** for both logic and memory (at full volume)
- **VT = 4** months for similar process, **7** months for very new one
- **RT = 4** months


Line Yield
Line yield per 20 layers (percent)
100
90
80
70
60
50
40
30
20
94
95
96
97
98
99
Time
M1
M2
M3
M4
M5
M6
M7

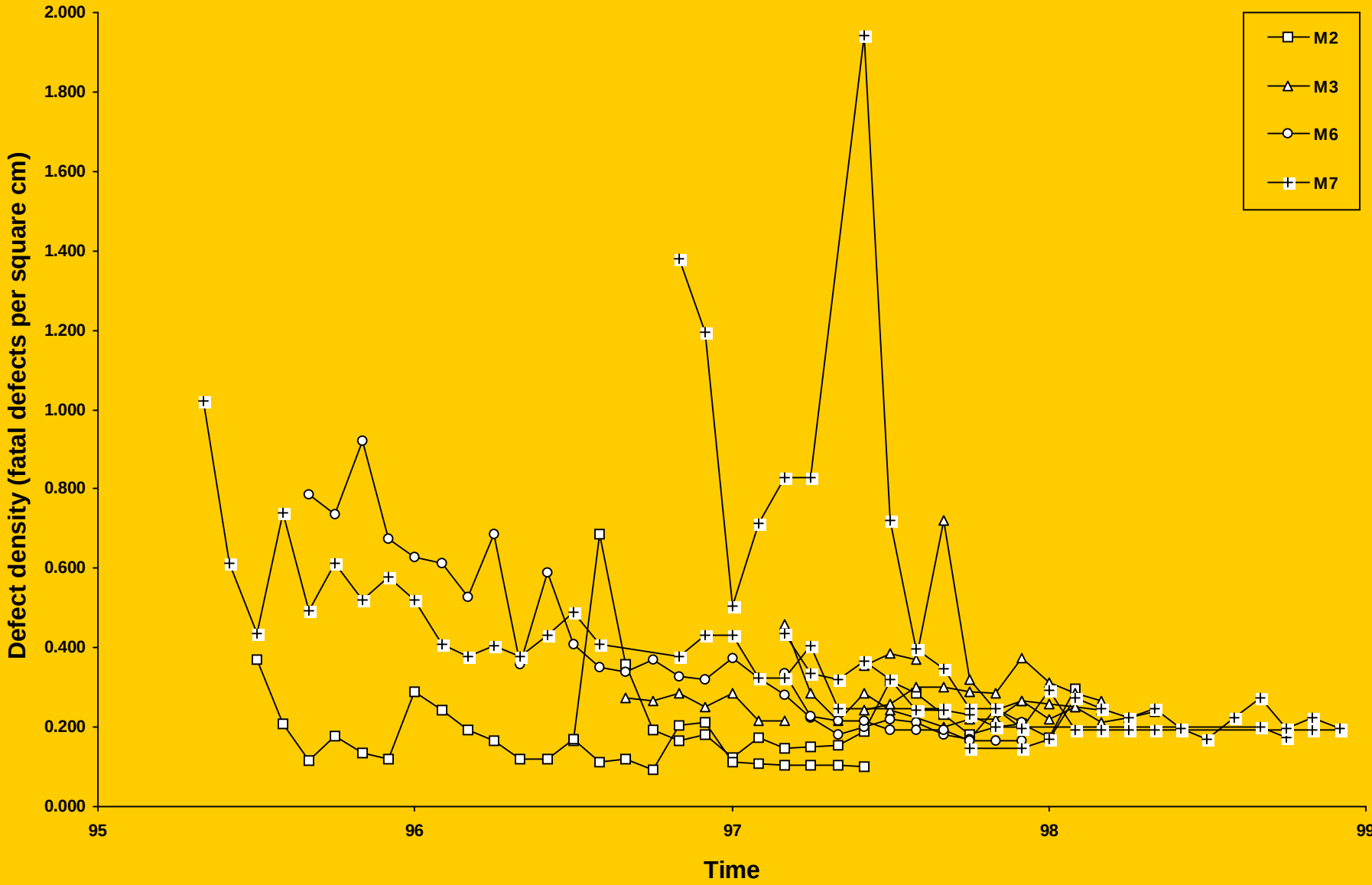
CMOS Logic Device Defect Density

0.35 - 0.4 micron CMOS process flows



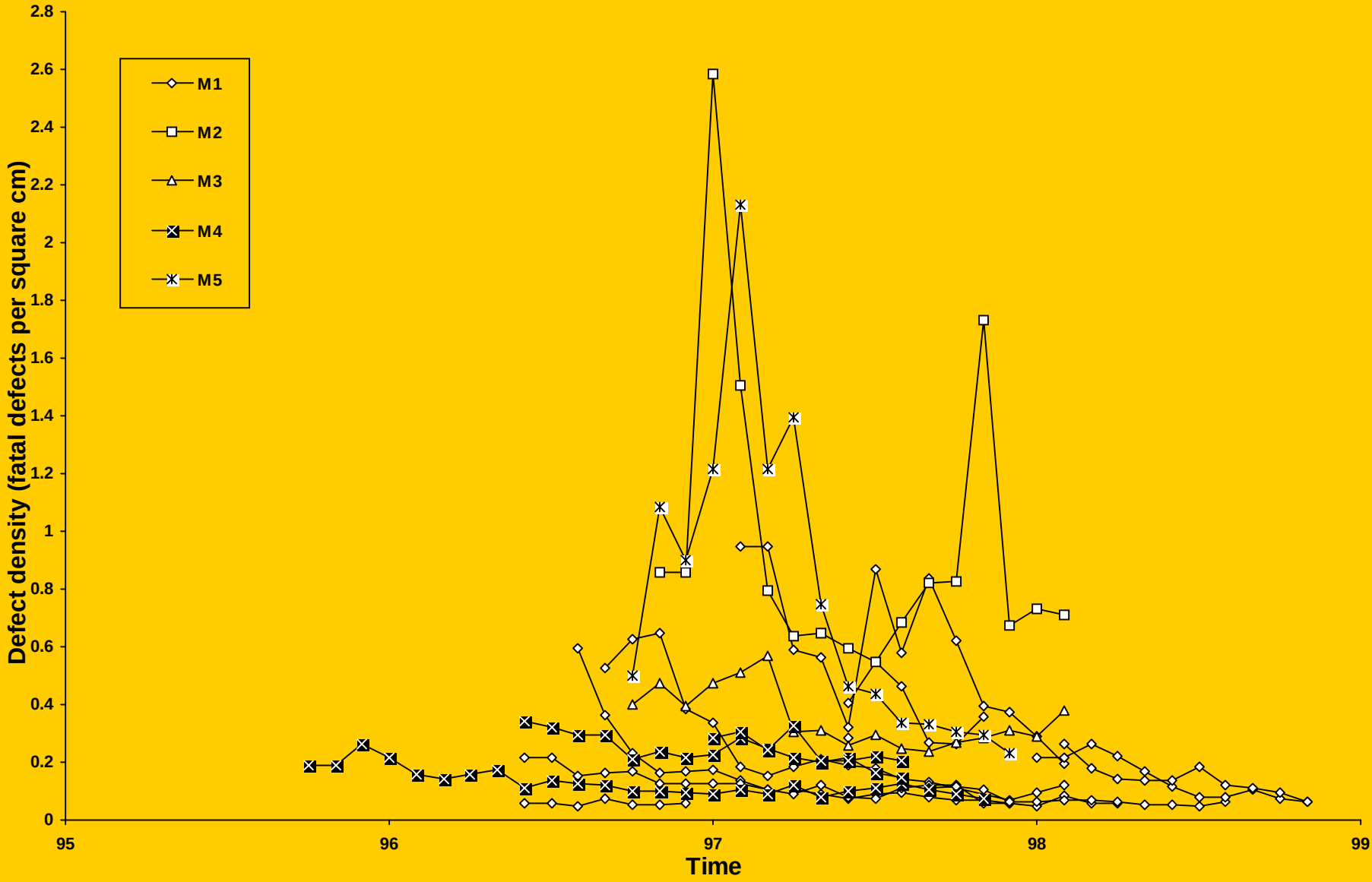
CMOS Logic Device Defect Density

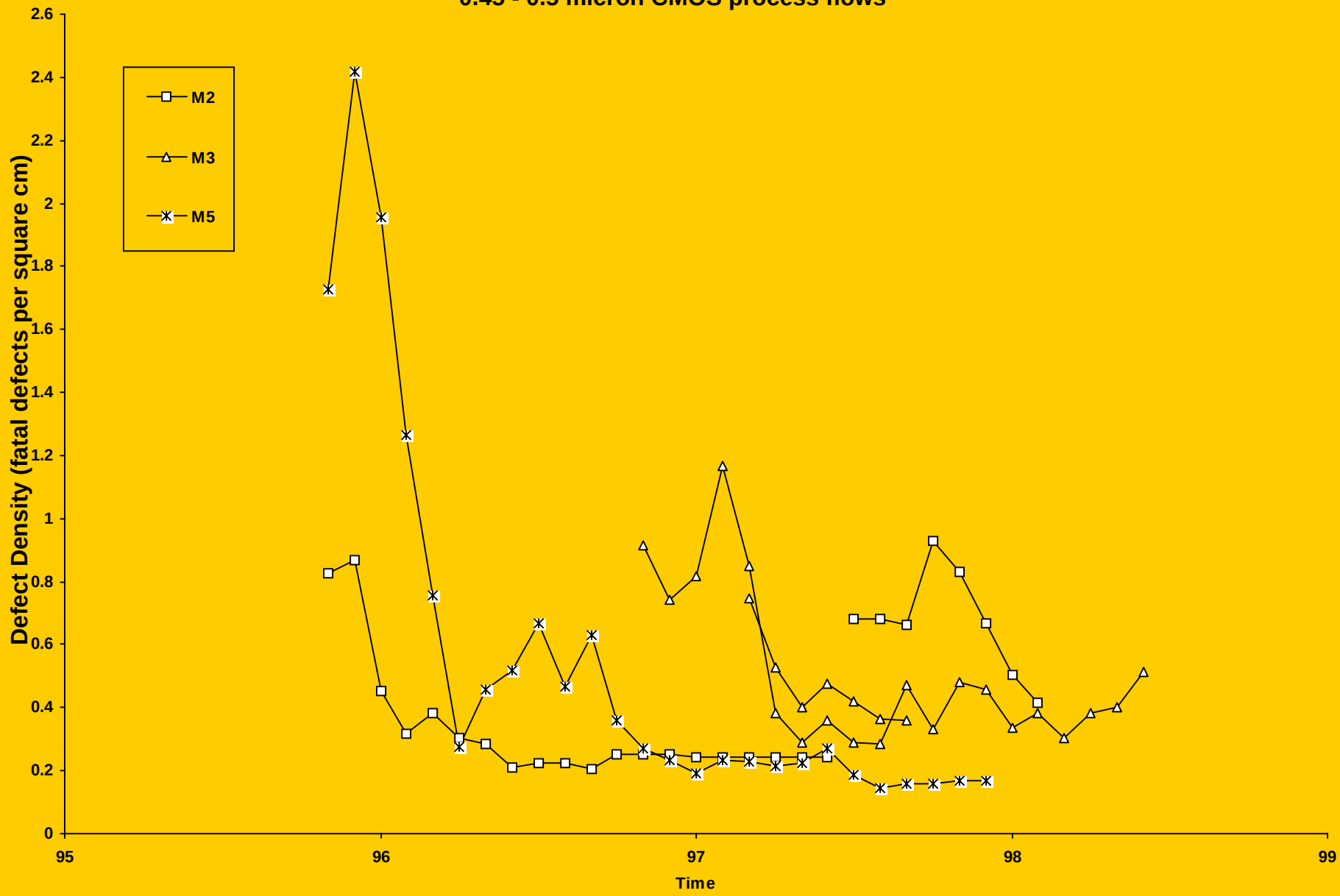
0.45 - 0.6 micron CMOS process flows



Memory Device Defect Density (after repair)

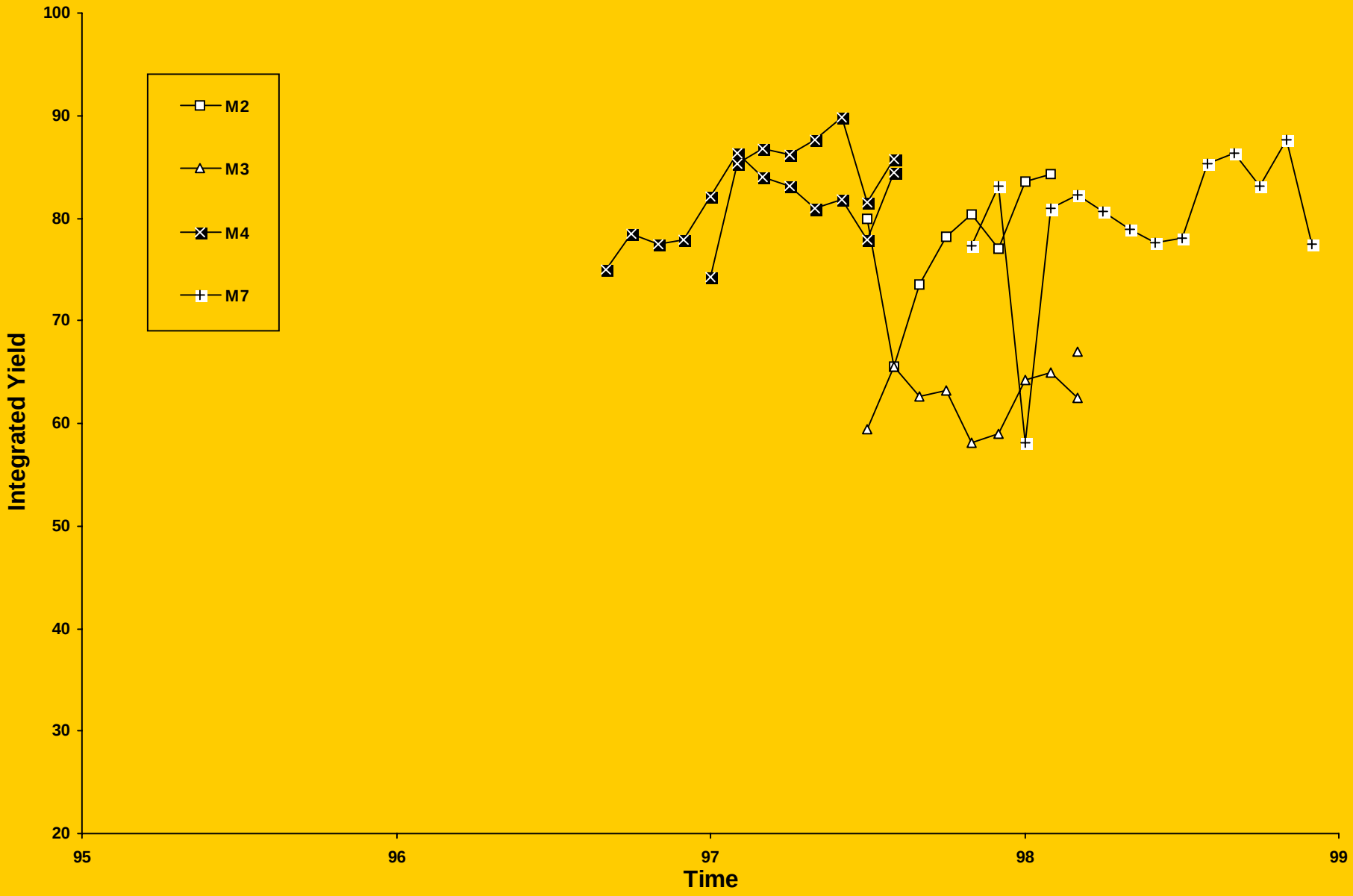
0.33 - 0.4 micron CMOS process flows

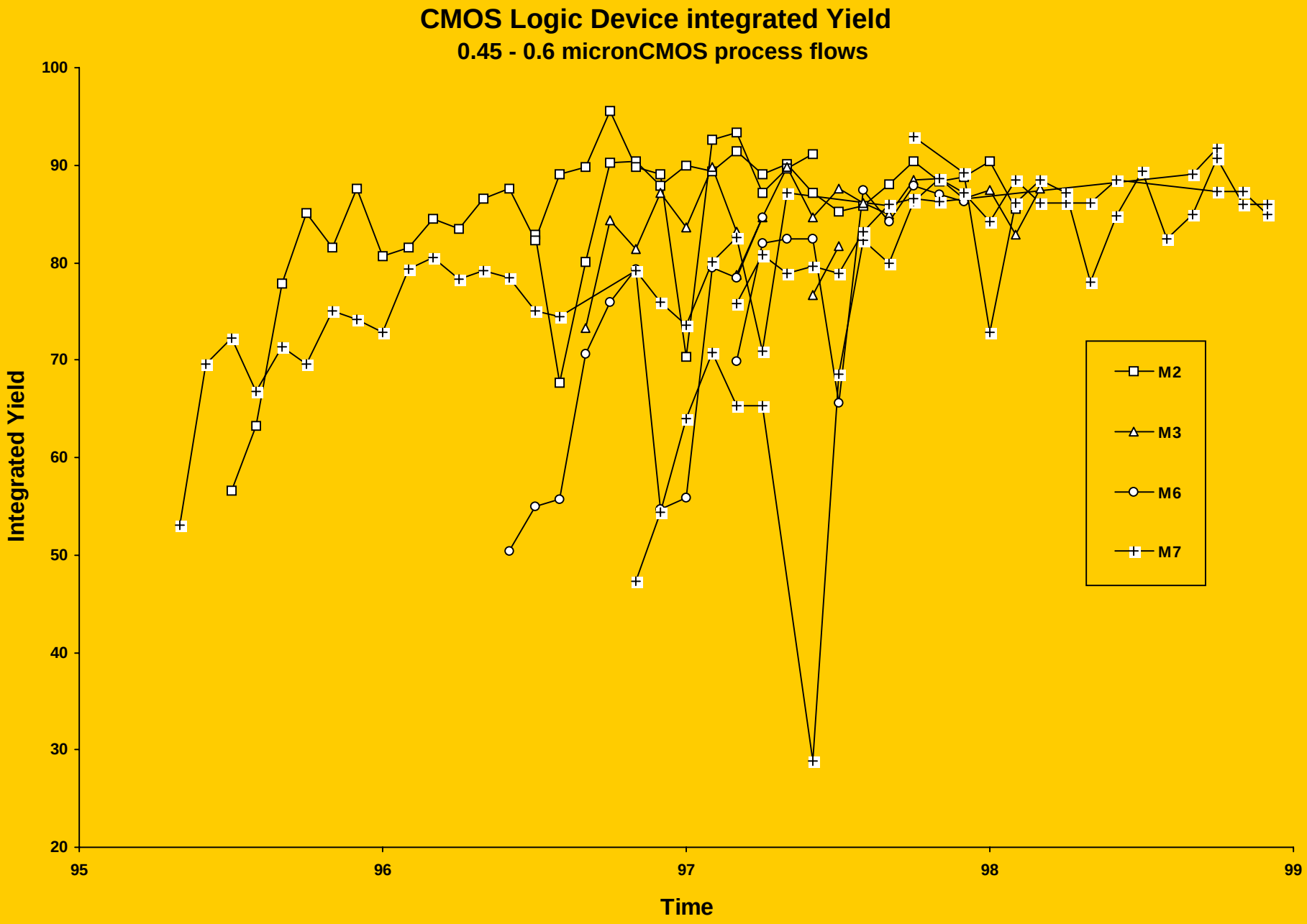



Memory Device Defect Density (after repair)
0.45 - 0.5 micron CMOS process flows
Defect Density (fatal defects per square cm)
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
M2
M3
M5
95
96
97
98
99
Time

CMOS Logic Device Integrated Yield

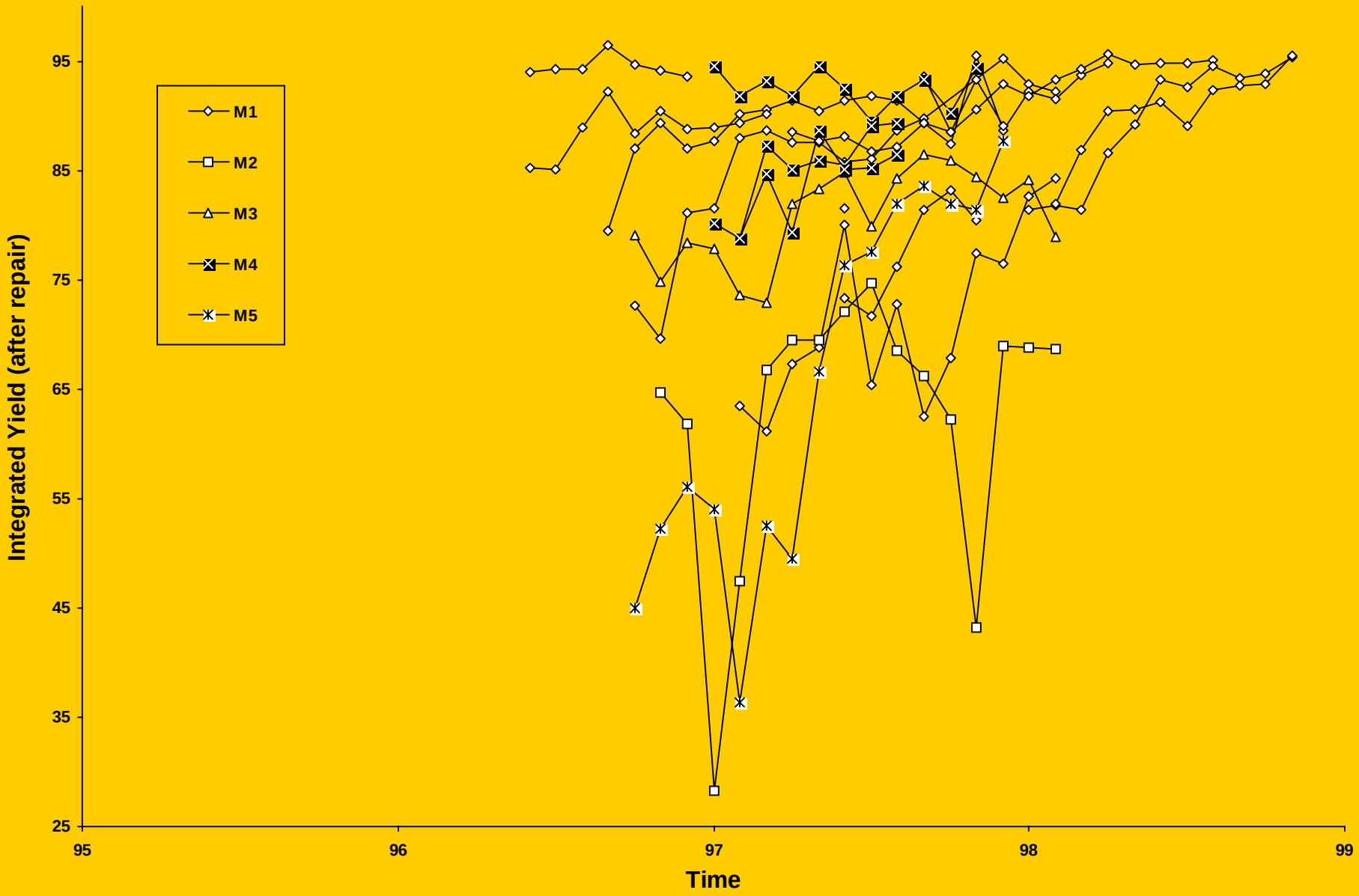
0.35 - 0.4 micron CMOS process flows

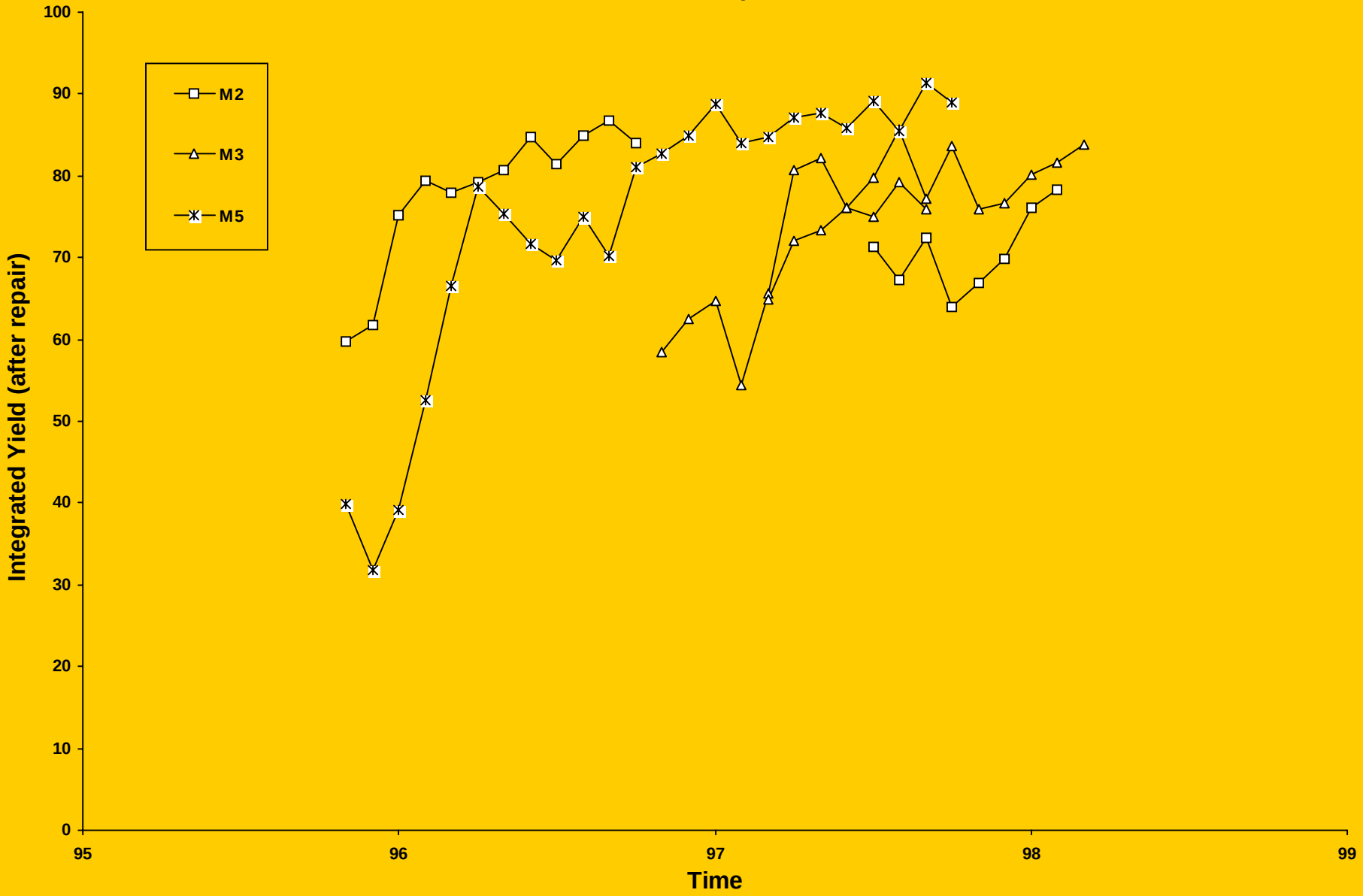



CMOS Logic Device integrated Yield
0.45 - 0.6 micronCMOS process flows
Integrated Yield
100
90
80
70
60
50
40
30
20
95
96
97
98
99
Time
M2
M3
M6
M7

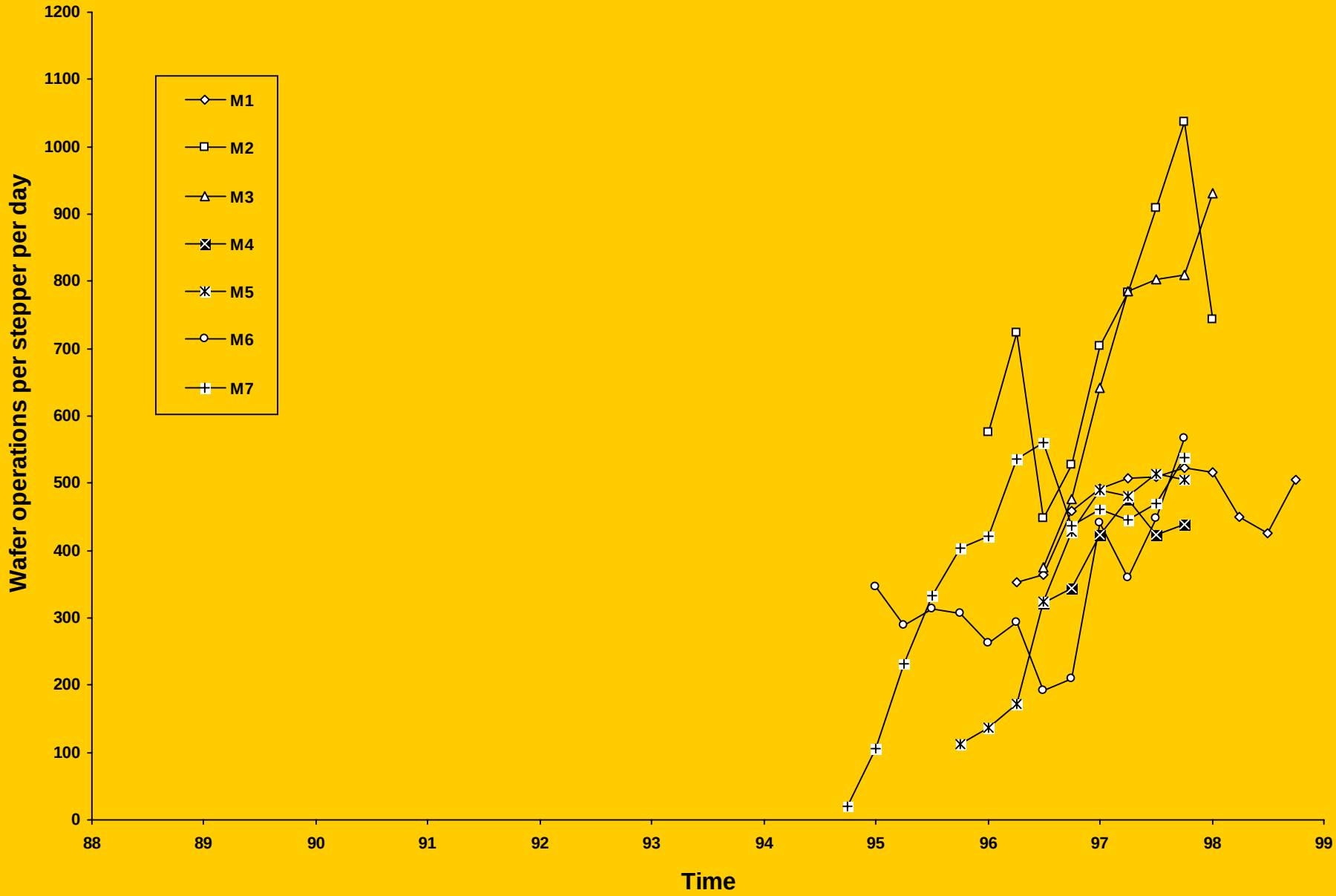
Memory Device Integrated Yield

0.33 - 0.4 micron CMOS process flows

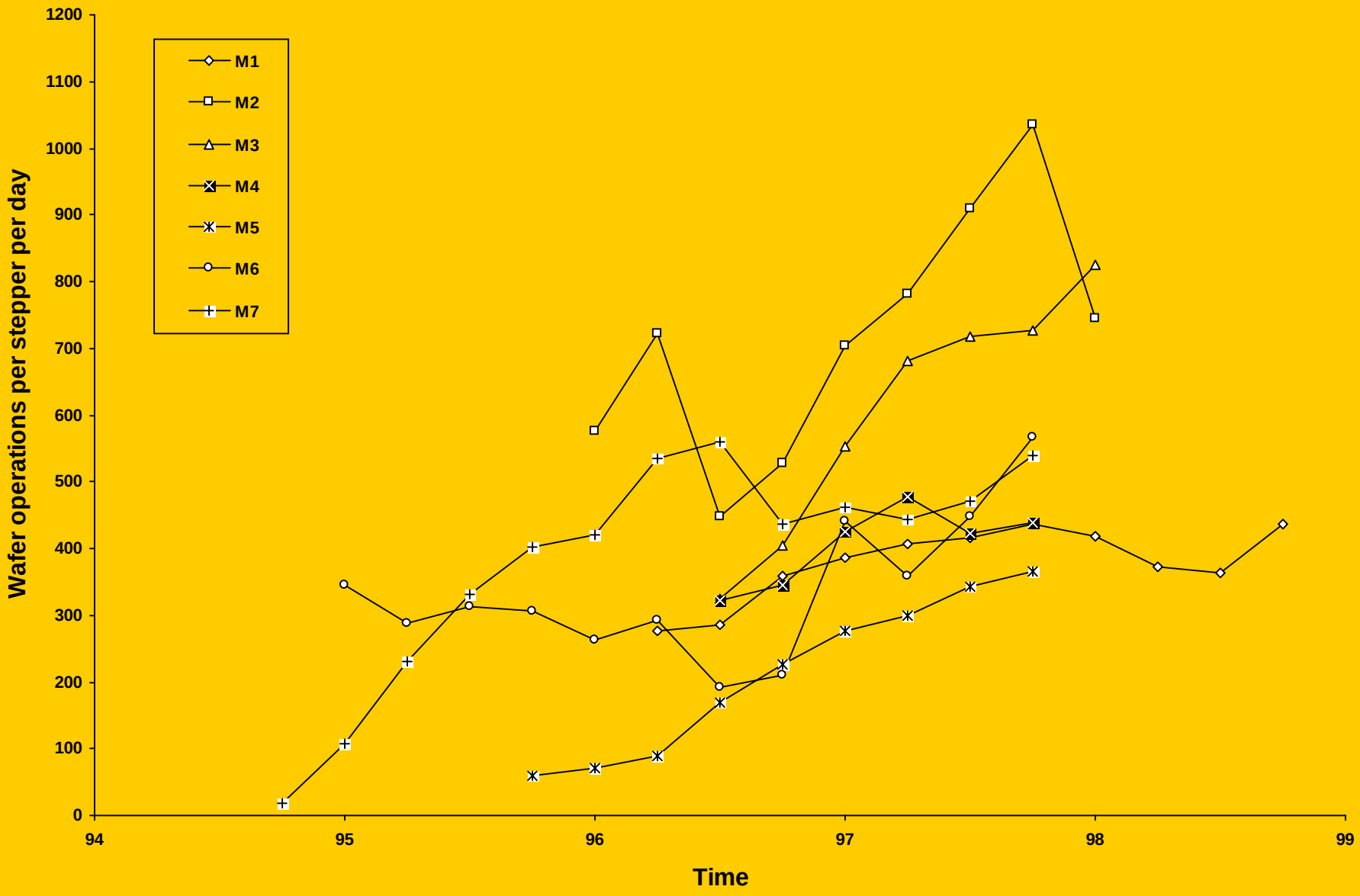



Memory Device Integrated Yield
0.45 - 0.5 micron CMOS process flows
M2
M3
M5
Integrated Yield (after repair)
100
90
80
70
60
50
40
30
20
10
0
95
96
97
98
99
Time

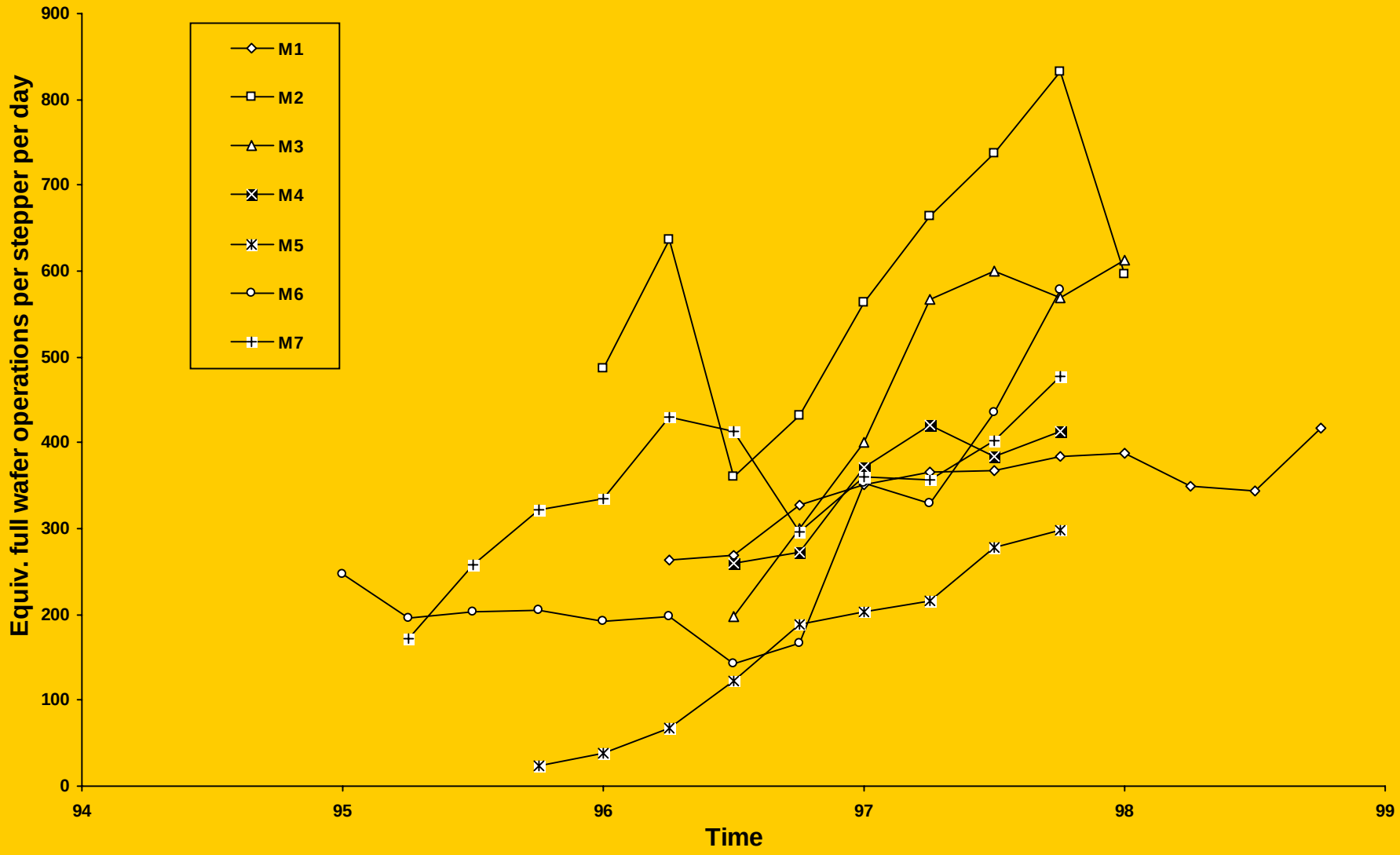
Stepper Productivity (all types of steppers)

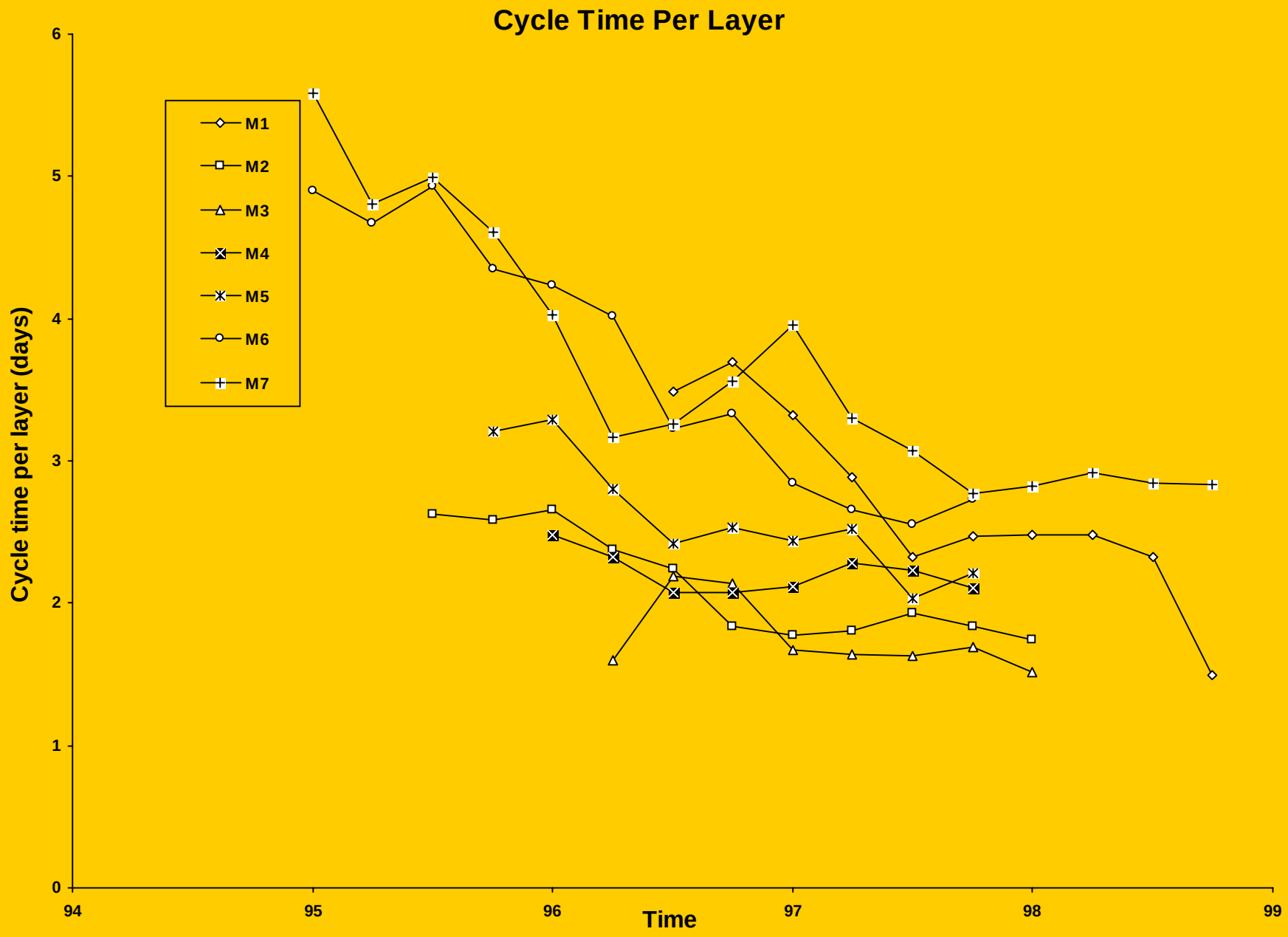


I-Line 5X Stepper Productivity

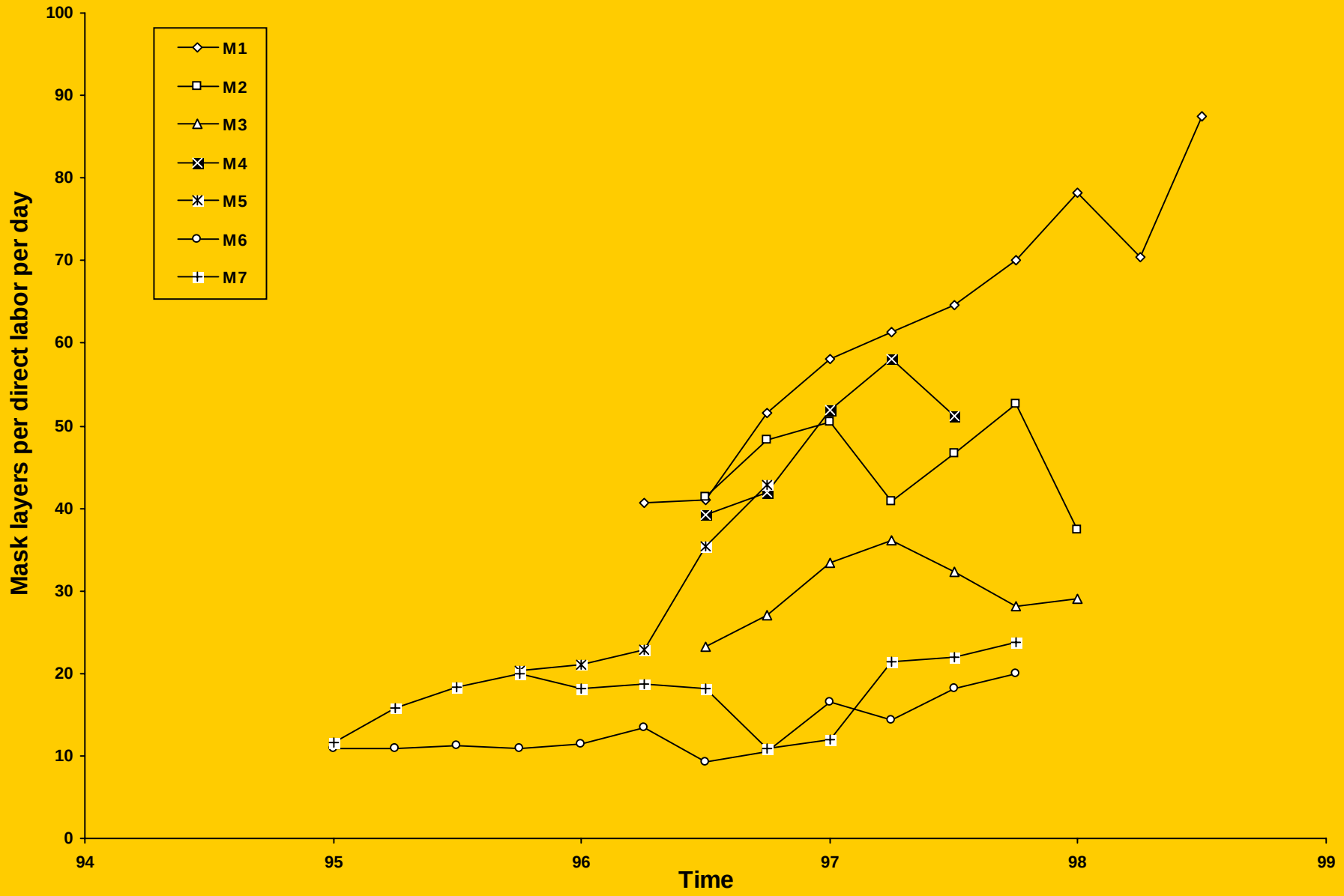


Integrated Stepper Throughput

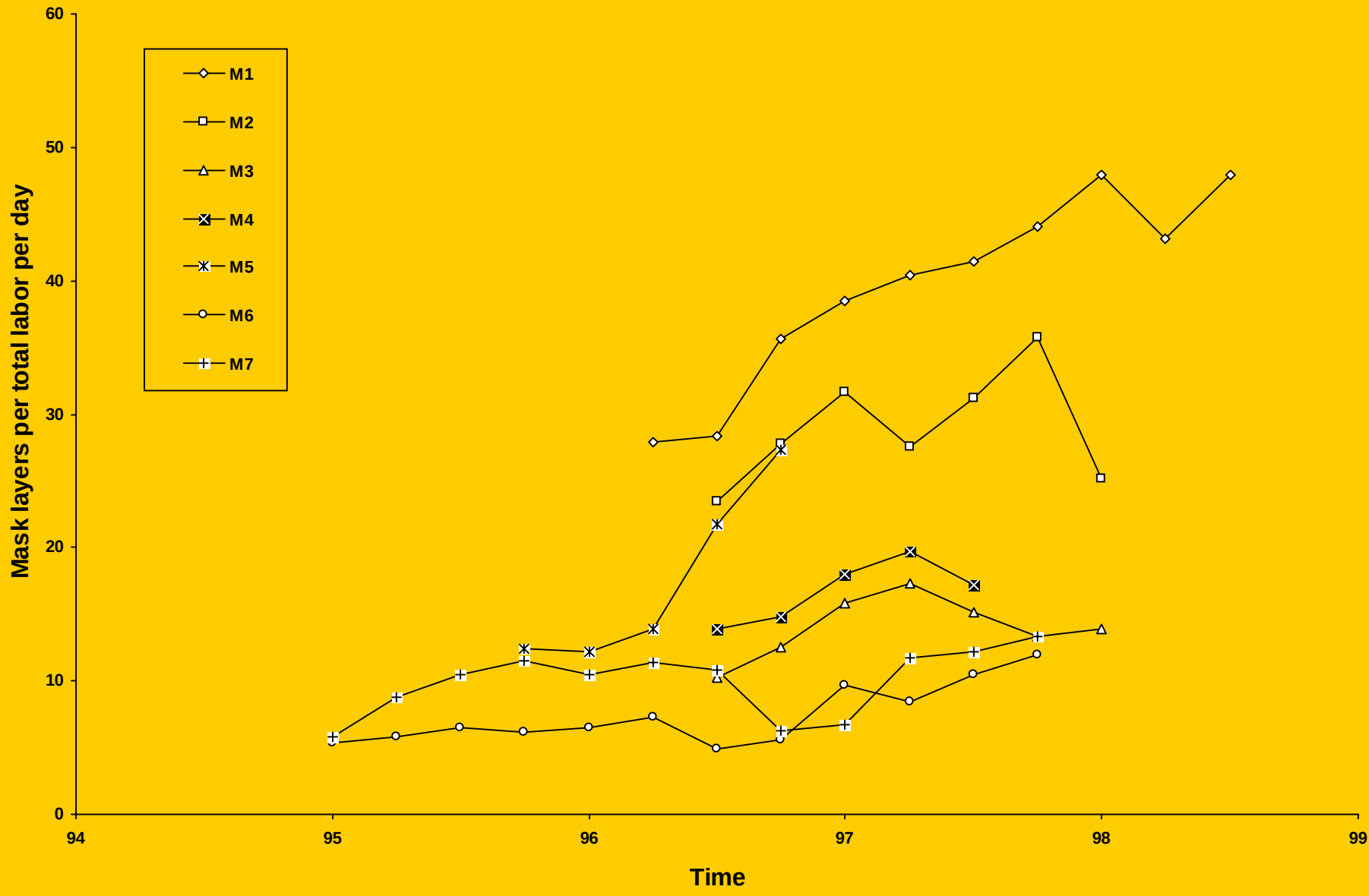



Cycle Time Per Layer
Cycle time per layer (days)
0
1
2
3
4
5
6
94
95
96
97
98
99
Time
M1
M2
M3
M4
M5
M6
M7

Direct Labor Productivity



Total Labor Productivity



Performance trends

- Generally, we find parity in mature yield performance among CSM participants
- Process development time, cycle time, ramp time and equipment efficiency seem to be the chief discriminators of current performance

Trade-offs between metrics

- It seems to be increasingly difficult to simultaneously achieve high yield, high wafer throughput and low cycle time
- Case-study example: photo-limited yields for advanced memory devices
  - Multiple poly layers for which perfect alignment is quite difficult

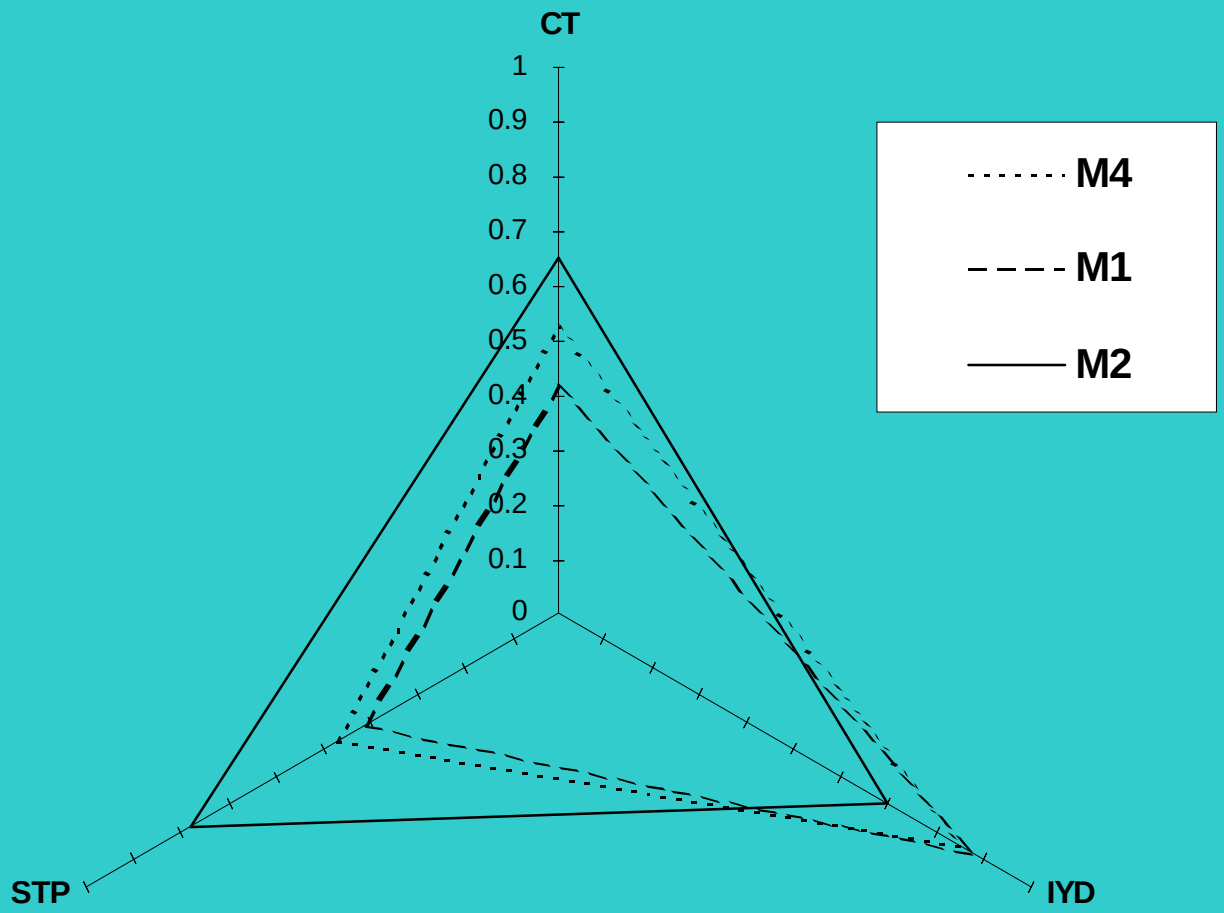
Alternative photo strategies

- Fab M4: must use exactly same stepper at all three critical layers
- Fab M1: given the selection of stepper at first layer, restrict choice of stepper at layers 5 and 9 to three particular machines
- Fab M2: no restriction on stepper selection

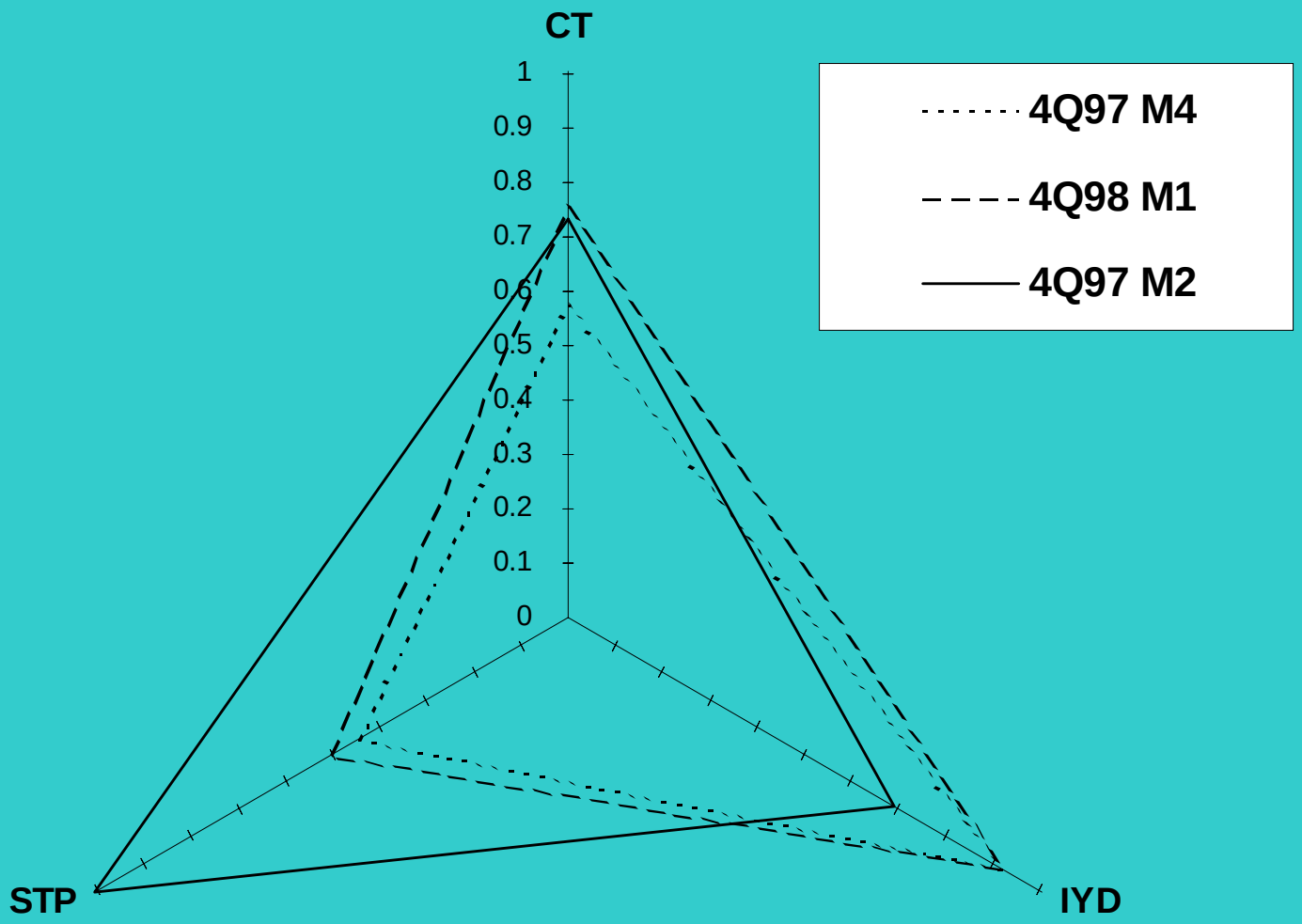
Three-dimensional performance plots

- Yield axis: we plot integrated yield, IYD = (LY20)(Murphy die yield for 0.5 sq cm device)
- Wafer throughput axis: we plot normalized stepper throughput, (STP)/1000
- Cycle time axis: we plot normalized reciprocal of cycle time, 1.2/(CTPL)

2Q97 performance



Subsequent performance



Modeling economic performance

Fab performance impacts two different cash flows:

- **Manufacturing expenses** (influenced by equipment efficiency and yield)
- **Lost revenues** (a.k.a. “delay costs”, influenced by time required for process development and qualification, time elapsed during yield ramp, and manufacturing cycle time) **since prices are falling**

Benchmarking economic performance

- Cost models have been developed to compute fab expenses and delay costs as a function of fab technical performance parameters
- These models are down-loadable free of charge from the CSM web site:

http://euler.berkeley.edu/esrc/csm

Benchmarking economic performance (cont.)

- CSM performance benchmarks for the seven 350nm fabs in Korea, Taiwan, Japan and USA were input to the fab expense and delay cost models
- Models were exercised on Sematech's 250nm logic process technology in a "greenfield" fab with 5-year equipment life

Economic benchmarks (250nm logic fab, 5-year life for all-new equipment)

- Fab expenses: **$1,880** per 100%-yielding wafer
- Delay costs: **$1,770** per 100%-yielding wafer (assuming initial selling price of $10K per 100%-yielding wafer)

Economic benchmarks (cont.)

- Difference between benchmark and average fab expenses: **$80** per 100%-yielding wafer
- Difference between benchmark and average delay costs: **$700** per 100%-yielding wafer
- **Speed, not yield, differentiates the leaders**

Economic value of speed

Value of a one-day reduction in

- process development time: **$3.40**
- yield ramp time: **$1.70**
- manufacturing cycle time: **$3.00**

These are values per 100%-yielding wafer, for every wafer produced over 5 years (assuming an initial sales price of $10,000 per 100%-yielding wafer, declining 25% per year).

Economies of scale in wafer fabrication

- "Small fabs are bad fabs" - Cy Hannon, EVP, LSI Logic
- Cost penalty vs. fab size:

Wafers/month	10K	20K	30K	40K	50K	60K
Cost/wafer	1.24	1.08	1.04	1.02	1.00	0.99

(50K cost = 1.00)

Source: Leachman et al, "Understanding Fab Economics," Report CSM-47

Studying practices: the site visit

- **Team of 6-8 faculty and graduate students**, plus interpreter if required, **for a 2 or 3 day visit**
- **Tour fab** (focus on evidence of self-measurement, communication, problem-solving activity
- **Interview cross-section of organization** (managers, engineers, technicians, operators)

Site visit (cont.)

- **Sessions to discuss approaches to problem areas** (yield improvement, equipment efficiency improvement, cycle time reduction, on-time delivery improvement, new process introductions)
- **Sessions to discuss problem-solving resources** (CIM and information systems, process control, work teams, human resource development)

Determining best practices

- Based on our notes from the site visits, **we searched for practices that were correlated with the metric scores.**
- **Typically, a good practice positively influences several metrics.** Participants tended to score well or score poorly across several metrics.
- Even so, **almost every participant had at least one practice that the other participants would benefit by adopting.**

Six basic themes for best practices

- **Automate information handling** and make manufacturing mistake-proof
- **Collect detailed process, equipment and test data, integrate the data and analyze it statistically**
- **Wisely manage development and introduction of new process technology**

Six key practices (cont.)

- Eliminate lost time on steppers and other bottleneck equipment
- Implement intelligent scheduling and WIP management
- Reduce division of labor, up-skill the workforce, develop a problem-solving organization

Automation of information handling

- 100% auto-recipe download
- 100% auto-WIP tracking
- 100% auto-metrology upload
- Fully automated and interlocked SPC

Data integration and analysis

- **Integrated yield analysis database** fitted with convenient and powerful statistical tools
  - Complete audit trail of product, process and equipment in one database
  - Process engineers do much of the analysis
- **Extensive in-line defect monitoring** (blending electrical and optical inspection) based on intelligent sampling plans

Managing process development and transfer

- **Control the number of simultaneous engineering variables:**
  - Staggered introductions of processes, devices and wafer sizes
  - Steady rate of introduction of new process modules in each generation

Managing process development and transfer (cont.)

- **Minimize complexity of hand-off**
  - "Copy exactly" policy:
    - identical equipment sets and recipes (ideally, same fab)
    - identical CIM systems
  - Concurrent engineering in same fab line:
    - sustaining engineers qualify all new equipment
    - regular manufacturing system handles all processing for development

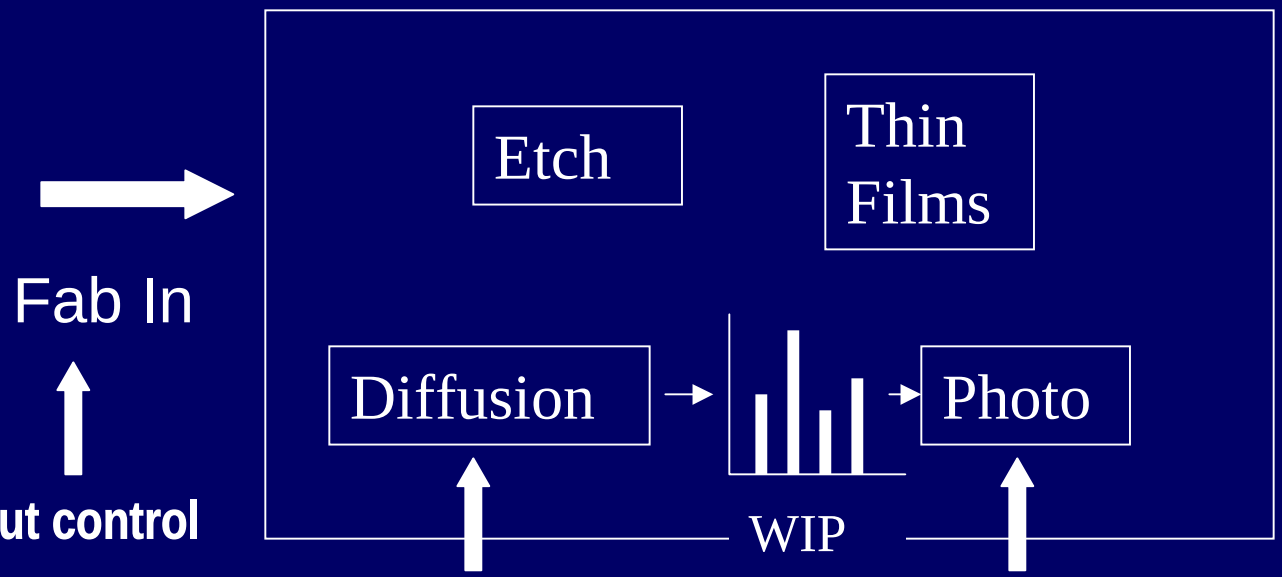
Equipment efficiency improvement

- Software permitting “cascading” of different recipes
- Auto-feedback control to eliminate test wafers and send-aheads
- Review of SECS-II data to discover hidden losses in machine cycles
  - SPC-type alarms for inferior equipment speed
- TPM teams for improved machine operation and maintenance

Scheduling and WIP management

- Intelligent detailed, on-line scheduling based on downstream WIP situation and intelligent targets
- Fab-out scheduling and fab-in control according to true capacity and current WIP
- Target cycle times and target WIP levels based on bottleneck starvation avoidance and statistical analysis
- No judgement, just systems

Automated Scheduling Modules



Input control

•Control fab in according to IPQ's

Non-bottleneck scheduler

•Schedule equip-ment to complete IPQ's and prevent steppers from starving

Bottleneck scheduler

•Schedule steppers to complete IPQ's and to maximize utilization

Target setting

•Target cycle times and target WIP

Output planner

•Identify bottlenecks and schedule target fab out according to WIP level and stepper capacity

Up-skilling the work force

- TQM or TPM teams of operators and technicians supported by engineers
- Upgrade operator into “Self-sustaining technician” or “Self-help lady”
- Upgrade technician into “Equipment owner” or “Key man”

Reduced division of labor

- Merging of manufacturing and equipment maintenance groups
- Reduced division of labor between engineering groups
  - Joint equipment and process engineering organization
  - Yield analysis carried out by process engineers

Summary of findings

- **Biggest single factor explaining performance is the focus or "religion" of the organization:**
  - TQM and statistical process control
  - Statistical analysis of yield vs. in-line data
  - Cycle time reduction and on-time delivery
  - TPM and equipment throughput
- **Weak performers in a given category do not have the relevant focus**

Summary of findings (cont.)

- TQM & SPC was strong almost everywhere
- Statistical analysis of yield vs. in-line data was strong almost everywhere
- **Cycle time and on-time delivery focus was strong in US and Taiwan, weak in Japan,** mixed in Korea
- **TPM and equipment throughput focus was strong in Japan, weak in US and Taiwan,** mixed in Korea

Some conclusions

- **We find major differences in technical and economic performance.**
- **Trade-offs** between various metrics **are optimized differently** among the participants.
- For everyone, **fast ramp-up of production processes to high yield and high throughput while driving down cycle time** is the name of the game.

Conclusions (cont.)

- **Fast improvement depends on rapid problem identification, characterization and solution by a large, diverse organization**
- **Common themes of successful approaches:**
  - Leadership and development of personnel
  - Organizational participation, communication, accountability and responsibility for improvement
  - Information strategy and analytical techniques to support improvement

CSM sponsorship

We seek renewed support for our continuing research:

- Web-based self-benchmarking
- Fab economics studies
- Automated equipment efficiency diagnosis
- Efficient scheduling and WIP management systems
- Management of design/manufacturing interface

How to get in touch

- To order any of the almost 50 CSM reports, visit our web site at

http://euler.berkeley.edu/esrc/csm

- You can reach us via email at

csm@esrc.berkeley.edu