

**Competitive Semiconductor Manufacturing:
Final Report on Findings from
Benchmarking Eight-inch, sub-350nm Wafer Fabrication Lines**

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Executive Summary

Competitive Semiconductor Manufacturing (CSM) is an interdisciplinary research program at the University of California at Berkeley. Faculty, scholars and graduate students from the College of Engineering, the School of Business Administration and the Dept. of Economics participate in the program. Originally funded by the Alfred P. Sloan Foundation, since 1998 the program has been entirely funded by industry sponsors.

A major element of the CSM program is to survey world-wide fabrication performance and managerial practices. This report summarizes findings from benchmarking ten manufacturing facilities processing eight-inch silicon wafers to fabricate digital devices with feature sizes of 350nm and smaller. All of these fabrication plants were constructed in the 1993 – 1996 time frame. Performance data were collected from each participant for some or all of the time frame 1996 – 2000. The individual identities of the participants are confidential.

Sponsors of this survey include SEMATECH, the Electronics Industry Association of Japan, the Semiconductor Research Institute of Japan, Taiwan Semiconductor Manufacturing Corp., United Microelectronics Corp., Winbond Electronics, Samsung Electronics Corp., Micrus, Inc., Cypress Semiconductor, and ST Microelectronics. The survey was conducted without oversight or direction of the sponsors, and the conclusions expressed herein are not necessarily consistent with the views of any sponsor.

Fabrication benchmarks presented in this report include the following:

- * Fabrication line yield per twenty layers;
- * Defect density (accounting for all die yield losses, whether random or systematic) for 500, 350 and 250nm memory and logic CMS process technologies;
- * Integrated yield (line yield times die yield for a 0.5 cm² device with 20 layers) for each of the above technology generations;
- * Stepper throughput;
- * Integrated stepper throughput (integrated yield times stepper throughput);

- * Productivity of clean room floor space;
- * Productivity of direct labor and of total facility workforce;
- * Fabrication cycle time per mask layer;
- * Time required for process development and qualification in the mass production facility; and
- * Time required process qualification until mature die yield is attained.

Compared to previous CSM surveys, there was more closure in mature yield performance among the participants, and in this survey yield performance was not distinguished by region of the world. However, there was considerable disparity among the participants in the time required to develop, transfer and qualify for mass production each generation of process technology, in the initial yields achieved at time of qualification, and in the subsequent time required to ramp to mature yield. Large variations in equipment throughput, labor productivity, space productivity and manufacturing cycle time also were observed. About a 40 percent gap between average and benchmark performance was observed in the metrics for development time, yield ramp time, cycle time, and stepper throughput.

Benchmarks also are presented for availability and utilization of major types of process equipment. Again, more closure in performance was observed than in previous phases of the CSM survey. Benchmark equipment availability was above 80 percent for all types of equipment, reaching about 95 percent for steppers. Utilization of most equipment types at all participants was generally in the 70s or the 80s. CMP, poly etch and metalization were the only major equipment types with benchmark utilizations below 80 percent.

In process technologies with geometries of 350nm and less, the participants faced difficult trade-offs among three basic dimensions of manufacturing performance: yield, equipment throughput and cycle time. A specific case is illustrated in this report concerning photo-limited yields of advanced memory devices. Three CSM participants producing similar memory products approached this trade-off in very distinct ways, exhibiting in a 20 percent variation in integrated yield, and 35 percent variation in stepper

throughput and a 24 percent variation in cycle time performance among them. The participant with the best cycle time and best stepper throughput achieved the worst yield, while the participant with the best yield achieved the worst cycle time and the worst stepper throughput. Compared to the latter participant, a third participant was two percentage points behind in yield, but ahead in both stepper throughput and cycle time by 10 percentage points.

This report also provides an economic analysis of the performance gaps between average and benchmark performance observed in this survey. The observed performance levels were assumed to apply to SEMATECH's 250nm, five-metal-layer logic process, and differences were calculated in average wafer cost and average revenue per wafer over a five-year life for this process technology operated in a new fabrication facility at a volume of 25,000 wafer starts per month. Gaps in equipment throughput translated into a 19 percent difference in wafer cost or about \$265. Gaps in performance along the dimensions of development time, yield ramp time, and cycle time translated into a 15 percent difference in revenue per wafer or about \$565. Simply put, differences in manufacturing speed among the CSM participants seem about twice as significant economically as differences in manufacturing efficiency.

Managerial, organizational and technical practices underlying these performance gaps may be summarized in terms of six key practices. Leading fabs automate information handling, rendering manufacturing much more mistake-proof and promoting higher equipment throughput, faster cycle time, and higher-quality engineering data collection. They wisely manage the development and transfer of new process technology, minimizing the number of simultaneous engineering variables and mitigating the difficulties of technology transfer. They integrate and analyze process, equipment and test data to more swiftly uncover and resolve losses of yield and throughput. They detect and eliminate lost equipment time, including lost time internal to process cycles. They intelligently schedule and manage WIP, and they carefully plan their equipment installations, qualifications and volume ramps. Finally, the leading fabs develop strong

problem solving organizations, up-skilling their organizations and reducing the division of engineering tasks and the division of technical knowledge.

While industry was willing to take over sponsorship of CSM benchmarking activities from the Sloan Foundation, the CSM program found individual semiconductor manufacturing firms to be more reluctant to participate compared to previous phases of the CSM survey. Japanese industry associations provided funds to study four participants in Japan, but only two Japanese companies were willing to participate. SEMATECH provided funds to study four US member-company participants, but only two were willing to participate. Three Taiwan foundry companies provided funds to sponsor the survey, but only two were willing to participate. Perhaps this increased reluctance reflects increased confidence of manufacturing performance across the industry. Or perhaps it reflects a reluctance to make the considerable investment of staff time to participate in our survey.

The staff of the CSM program wishes to express our heartfelt gratitude to the sponsors and participants. We trust the participants found their investment well worthwhile.