Material & Process Compatibility Policy

1.0 Title

Material & Process Compatibility Policy

2.0 Purpose

This document is designed to provide quick reference for material and compatibility policy in the Microlab and will be reviewed by staff with updated information on a regular basis. This information in addition to equipment manual chapters and should provide answer to some of the frequently asked questions about material and process compatibility in the Microlab. Microlab members are expected to contact staff for any questions that may not be clear in their mind and/or not covered by the pertinent equipment lab manual chapters, including this one.

3.0 Scope

This chapter defines furnace pre-clean, metal substrate/pyrex/borofloat glass restrictions in the Microlab. This is a quick reference and by no means encompasses all the issues and concerns that may be raised about MOS, Non-MOS and old lab process/operation. Microlab users should adhere to specific guidelines spelled out in the operation manuals in addition to the information provided here to make their final decision on "what is allowed" and "what is not allowed" in the Microlab. As always ask when in doubt. Process Engineering and/or technology manager should be consulted for any issues or concerns you may have regarding material and process compatibility, not covered in the lab manual chapters. Furthermore, any new chemical and material introduced in the Microlab must be reviewed by staff and Material Data Sheet (MSDS) form posted in the blue binders at the entrance of the Microlab.

4.0 Applicable Documents

Revision History

5.0 Definitions & Process Terminology

N/A

6.0 Safety

N/A

7.0 Statistical/Process Data

N/A

8.0 Available Process, Gases, Process Notes

Review specific equipment manual in addition to the policies outlined in Section 9.0.

9.0 Material & Process Policy (Cross-Contamination Prevention Measures)

9.1 VLSI / Furnace Restriction

No gold in any VLSI tools; no gold in the VLSI area including Bank 5 and Lam 3. Certain metals are allowed in specific furnaces, as described below. If you do not see your metal described, discuss with staff before proceeding.

9.2 Basic Wafer Cleaning Policy (furnace pre-clean for silicon and 100% quartz (fused silica) wafers)

New wafers receive 1 piranha clean. Photoresist coated wafers need to have their PR stripped, then receive 2 piranha cleans (Non-MOS followed by MOS). Metal wafers (wafers with metal layer/s on them) should never be exposed to piranha, as it will attack the metal film and major contamination to the sink will occur.

- ► New 4" and 6" wafers must be cleaned in Sink 6 piranha prior to loading into an MOS or Non-MOS furnace.
- ► Resist coated 4" and 6" wafers with no metal layers on them, must be stripped with PRS3000 or O_2 plasma, and then cleaned in Sink8 piranha followed by Sink6 piranha clean, prior to loading into a MOS or Non-MOS furnace.

9.3 Specialized Procedures for Furnace Processing of Metal-Coated Wafers

- ► Only specific metals are allowed in specific non-MOS furnaces.
- ► Do not attempt to clean any metal-coated wafers in any piranha.
- ► Metal wafers (wafers with metal layer/s) 4” & 6” wafers may be processed in specific non-MOS furnaces after being cleaned in the sink5 metal clean bath followed by dump rinse (QDR) and SRD steps at Sink5, as well.
- ► Resist coated 4" & 6" metal wafers (wafers with metal layer/s) may be processed in specific non-MOS furnaces after resist stripping with PRS3000 and/or O_2 plasma, followed by cleaning in the sink5 metal clean bath, then dump rinse (QDR) and SRD steps also at Sink5.
- ► Non-MOS furnaces presently approved for processing of metal wafers (wafers with metal layer/s) are:

  - **Tystar4** for annealing

  - **Tystar16** for amorphous or poly silicon deposition

  - **Tystar17** for low stress nitride and HTO deposition

  - **Tystar18** for sintering process

  - **Tystar12** and **tystar20** for LTO and poly-Ge/poly/SiGe film deposition, respectively.

9.4 Specialized Procedures for Furnace Processing of Non-Quartz Glass Wafers

For information on different types of non-quartz glass wafers, see Process Module 31.

- ► Non-quartz glass wafers should Never be cleaned at Sink6.
- ► New 4" and 6" non quartz glass wafers must be cleaned in Sink 8 piranha prior to loading into a Non-MOS furnace.
- ► Resist coated 4" and 6" non-quartz glass wafers must be stripped with PRS3000 or O_2 plasma, and then cleaned in Sink8 piranha prior to loading into a Non-MOS furnace.

9.5 Special Restriction on Etch Equipment

- ► No metal etching is allowed in Lam1, Lam2, Lam4 and Lam 5. Use Lam3 (metal etcher) for metal etch process, only.
- ► No non-quartz glass wafer (e.g.,Pyrex or borofloat) etching is allowed in Lam4 and Lam5. Non-quartz glass wafers may be etched in P-therm. See Chapter 1.3, Process Module 31 for more information.
- ► Do not grow C4F8 based polymers thicker than 1 micron in STS.
- ► No metal hard masks are allowed in the STS. Oxide/nitride and photoresist etch masks only.

9.6 Additional Information

Tystar 20 has specifically been developed to enable deposition of poly-Ge and poly-SiGe films on top of completed CMOS wafers. T efore, expected metal contaminants in Tystar 20 may include: Al, Al2%Si, Ti, W.

Furnace Pre-cleaning Requirement Table

Acceptable 4" and 6" substrates: Si, SOI, quartz
(Non-quartz glass wafers (pyrex/borofloat) in Tystar16, Tystar12, and Tystar20, only)

Equip.	Description	Pre-Cleaning Required for					
		New Si, SOI, Quartz Wafers	**PR Coated Si, SOI, Quartz Wafers**	**New Non-Quartz Glass Wafers**	**PR Coated Non-Quartz Glass Wafers**	**Metal (blank film)**	**PR Coated Metal Wafers** (See tube specific notes)
Tystar1	**Atmos. Furnace (MOS)**	Sink6	**Restricted** See Tystar1 manual	NA	NA		NA
Tystar2	**Atmos. Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar3	**Atmos. Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar4	**Atmos. Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	Sink8	Wet Strip or Matrix + Sink8	Sink5 metal clean bath + Sink5 QDR/SRD *See Notes 1 and 2	Wet Strip or Matrix + Sink5 metal clean bath+ Sink5 QDR/SRD *See Notes 1 and 2
Tylan5	**Atmos. Furnace (MOS)**	Sink6	**Restricted** see Tystar1 manual	NA	NA	NA	NA
Tylan6	**Atmos. Furnace (MOS)**	Sink6	**Restricted** see Tystar1 manual	NA	NA	NA	NA
Tylan7	**Atmos. Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tylan8	**Atmos. furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar9	**LPCVD Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar10	**LPCVD Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA

Tystar11	**LPCVD Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar12	**LPCVD Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	Sink8	Wet Strip or Matrix + Sink8	Sink5 metal clean bath + Sink5 QDR/SRD *See Notes 1 and 2	Wet Strip or Matrix + Sink5 metal clean bath+ Sink5 QDR/SRD *See Notes 1 and 2
Tystar13	**Atmos. Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar14	**Atmos. Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar15	**LPCVD Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar16	**LPCVD Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	Sink8	Wet Strip or Matrix + Sink8	Sink5 metal clean bath + Sink5 QDR/SRD *See Note 1	Wet Strip or Matrix + Sink5 metal clean bath+ Sink5 QDR/SRD *See Notes 1 and 2
Tystar17	**LPCVD Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	Sink5 metal clean bath + Sink5 QDR/SRD *See Note 1	Wet Strip or Matrix + Sink5 metal clean bath+ Sink5 QDR/SRD *See Notes 1 and 2
Tystar18	**Atmos. Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	Sink5 metal clean bath + Sink5 QDR/SRD +Sink8 SRD *See Note 1	Wet Strip or Matrix + Sink5 metal clean bath+ Sink5 QDR/SRD *See Notes 1 and 2
Tystar19	**LPCVD Furnace (MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	NA	NA	NA	NA
Tystar20	**LPCVD Furnace (Non-MOS)**	Sink6	Wet Strip or Matrix + Sink8 + Sink6	Sink8	Wet Strip or Matrix + Sink8	Sink5 metal clean bath + QDR+ SRD in sink5 *See Notes 1 and 2	Wet Strip or Matrix + Sink5 metal clean bath+ Sink5 QDR/SRD *See Notes 1 and 2

Note 1: No metal wafers with melting points below 1500ºC are allowed in this furnace.

Note 2: Wafers with Al/2%Si allowed in this furnace.

VLSI Sinks Definition Table

Sink	Tank	Chemical Type Allowed	Wafers Processed			Spin Rinse Dryer	
			Pre-Clean Before		Wafers w/ PR	4"	6"
			MOS Furnace	Non-MOS Furnace			
sink6 (MOS)	left heated tank	Piranha	yes	yes	no	SRD6 stack (Sink6)	SRD6 stack (sink6)
	right heated tank	Piranha	yes	yes	no		
	left center-tank	25:1 HF	yes	yes	no		
	right center-tank	10:1 HF	yes	yes	no		
	left QDR	DI-water	yes	yes	no		
	right QDR	DI-water	yes	yes	no		
sink7 (General use)	left heated tank	Staff general use+ heated H2O2 for poly Ge etch	no	no	no	SRD8 stack (sink8)	SRD8 stack (sink8)
	right heated tank	phosphoric acid (Si3N4 etch only)	no	no	no		
	left center-tank	Silicon etch + general use, but no piranha/sulfuric (non-MOS)	no	no	yes		
	right center-tank	100:1 HF+ general use, but no piranha/sulfuric (MOS)	no	no	yes		
	left QDR	DI-water	no	no	yes		
	right QDR	DI-water	no	no	yes		
sink8 (Non-MOS)	Left heated tank	Al etch	no	no	yes		
	center tank	5:1 BHF	no	no	yes		
	right heated tank	piranha (Non-MOS clean, also wafers post PR strip allowed)	no	no	no		
	left QDR	DI –water	no	no	yes		
	right QDR	DI- water	no	no	yes		
sink9 (Gate oxide pre-clean)	left heated tank	Piranha	yes	no	no	SRD6 stack (Sink6)	SRD6 stack (sink6)
	left center-tank	25:1 HF	yes	no	no		
	right center-tank	No chemical (consult with staff, if need it)	N/A	N/A	N/A		
	right heated tank	No chemical (consult with staff, if need it)	N/A	N/A	N/A		
	left QDR	DI-water	yes	no	no		
	right QDR	DI-water	yes	no	no		

Other Sinks Definition Table

Sink	Tank	Chemical Type Allowed	Wafers Processed			Spin Rinse Dryer	
			Pre-Clean Before		Wafers w/ PR	4"	6"
			MOS Clean Furnace	Non-MOS Clean Furnace			
Sink3 (Non-MOS)	Left heated tank	KOH	no	no	no	N/A	N/A
	Right heated tank	TMAH	no	no	no		
	Right QDR	DI-water	no	no	no		
	Left Rinse tank	DI-water	no	no	no		
Sink5 (General use)	Left heated tank	PRS-3000	no	no	yes	SRD5 stack (Sink5)	SRD5 stack (Sink5
	Center heated tank	PRS-3000	no	no	yes		
	Right heated tank	SVC-14	no	no	no		
	Left QDR	water	no	no	yes		
	Center developer tank	water	no	no	yes		
	Right glove wash	water	no	no	yes		

Notes: The right tank in sink5 is dedicated to Pre-furnace cleaning for metal wafers allowed in certain furnaces, as described earlier.

Sinks 4, 432A and old lab sinks are general acid/solvent sinks and do not have specific chemicals assigned to them.