MEMORANDUM

To: Katalin Voros, Operations Manager
From: **Sia Parsa**, Process Engineering Manager
Subject: 2009 Year-End Report
Date: 25 January 2010

I. OVERVIEW

This memorandum documents process engineering group activities for the calendar year 2009. Last year, I supervised the process engineering group comprised of 4 process engineers (one MEMS-Exchange engineer), on the average three lab assistants (undergraduate students), and one graduate student researcher, as well as our baseline research associate.

This was a very busy year for us; sustaining our normal operation in the Microlab, while preparing for the move to the new Marvell Nanolab. Process staff participated in planning and defining specifications for all our new acid/solvent sinks, going into the new lab. We continued our training classes on the Crestec E-beam writer, on a regular basis (~ 2 days/month); also developed processes on the new tools; compiled facility connections for all current tools moving into the new lab (the list was signed off by the equipment engineer in charge of each tool). MEMS-Exchange, ETR runs, and mask making requests were completed on time. One baseline run was completed with great results. We also generated CAD layouts, and necessary documentation for new lab projects assigned to us.

The following summarizes Process Engineering activities for 2009.

II. NEW LAB PREPARATION/SUPPORT

- Met with Bill Flounders, Manager of the Marvell Nanofabrication Laboratory (MNL), twice a week to discuss lab members' request and technical questions, as well as plan ahead for the move. Wet sink specification for the new lab were defined during these meetings. Process Group also provided input, as well as generated CAD layouts and PDF versions of these schematics for MSink1, Msink3, Msink4, Msink5, Msink6, Msink8, Msink16 and Msink18, prior to submitting orders for the fabrication of new sinks at the vendor site. The sinks have turned out great, installed in the new lab. Msink6 and Msink8 our primary VLSI sinks are currently functional, and, as planned, ahead of furnace release in the Marvell lab.
- Added program2 to YES prime oven to phase out sink HMDS (bubbler in the new lab).
- Investigated available recipes (process parameters) for the new AMAT EPI machine.
- Storage inventory of the current Microlab was prepared to be used as a reference (template) for the new Marvell Lab preparation.
- Facility requirements for each equipment in the current lab was compiled by Attila Szabo and reviewed by equipment engineers in charge of each tool. This information have been used to plan facility connection for reinstallation of the tools in the new Marvell facility.
- Performed baseline tests on evaporators and sputter machines in the old lab area of the Microlab, prior to relocating them over to the new Marvell Nanofabrication laboratory. These collected baseline data should help us resolve possible problem/s that may occur during equipment reinstallation. As of now, half of the old lab tools have moved over to MNL site without any problems.

III. EQUIPMENT UPGRADE, NEW INSTALLATION & PROCESSES

Centura-MET Metal Etch Process

A new DPS metal etch chamber and associated passivation/resist strip + cooling stations were added onto our AMAT Centura platform (total of 3 new chambers) at the end of the previous year. Metal etch (BCl3/Cl2 chemistry) and passivation processes were promptly characterized and released, alongside the online equipment manual in January 2009. Great metal etch rate, uniformity, and selectivity to oxide were achieved in the "Metal Etch" chamber by our standard process, as well a fast resist removal process that was implemented in the passivation/resist strip chambers, as follows:

Metal Main Etch

Metal etch rate/min: 6744 Å/min
Average within wafer non-uniformity ~ 3.4%,
Selectivity to: LTO = 9, PSG =8.4, I-line and DUV resists ~ 2.1

Metal Over Etch

Metal etch rate/min: 4361 Å/min
Average within wafer non-uniformity ~ 3.6%
Selectivity to: LTO = 6.7, PSG = 6.6, I-line and DUV resists ~ 2.0

Passivation Process

Resist etch rate/min: 0.6 µm/min
Average within wafer non-uniformity ~ 3.9%

Resist strip process

Resist etch rate/min: 4 µm /min
Average within wafer non-uniformity ~ 8%

High Temperature Oxide (HTO)

Low and high deposition rate type HTO recipes were set up on our tystar17 furnace, for MEMS and other special application processes. Process parameters including deposition temperature, were changed to arrive at different deposition rates required by thin and thick HTO processes.

	Low Deposition rate HTO	High Deposition Rate HTO
Deposition Rate	3 Å/min	25 Å/min
Within wafer Non-uniformity	<2%	<4%
Wafer to wafer uniformity	~9%	~ 12%

Table 1 - High Temperature Oxide (HTO) Process Data

Parylene Process

A series of tests were performed by Attila Szabo our MEMS-Exchange engineer, to determine thickness of deposited parylene film vs. dimer (di-para-xylylene) mass used for both of parylene "N" and "C" processes. This data was included in the equipment lab manual, as reference data for dimer usage and expected deposition rate, for members using these processes.

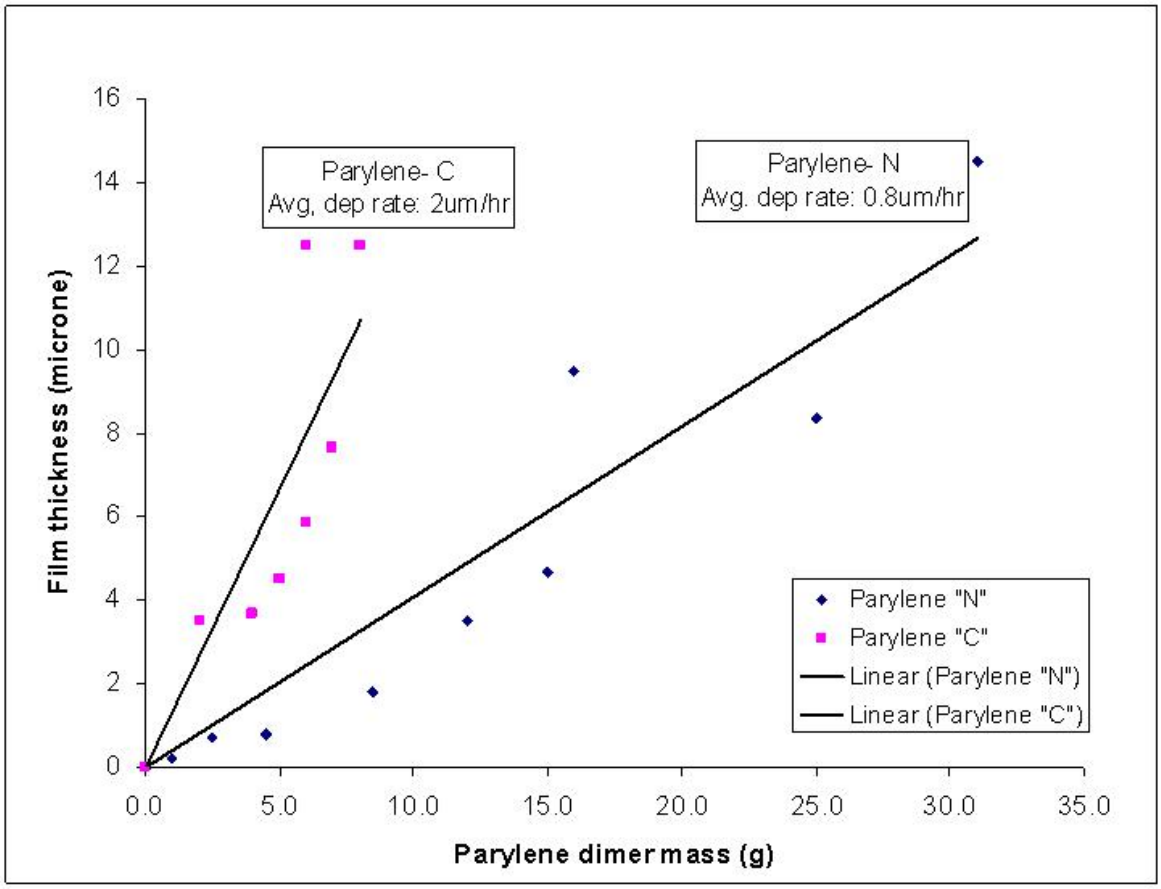


Figure 1 - Parylene N and Parylene C Deposition vs. Dimer Use

IV. PROCESS DEVELOPMENT, SUSTAINING & IMPROVEMENT ACTIVITIES

Modified and New Processes

Plasma Quest ECR recipes were modified to generate good films of SiO2 with proper refractive index values. This included changing the oxygen to silane ratio in the oxide recipe that targeted refractive index of around 1.4, as per follows:

O2 flow:	30 sccm
SiH4 flow:	100 sccm
Argon flow:	120 sccm
Process Pressure:	25 mTorr
Chuck Temperature:	24ºC
Upper Magnet:	185 Amps
Microwave Power:	350 Watts
Deposition Rate:	310 Å/min

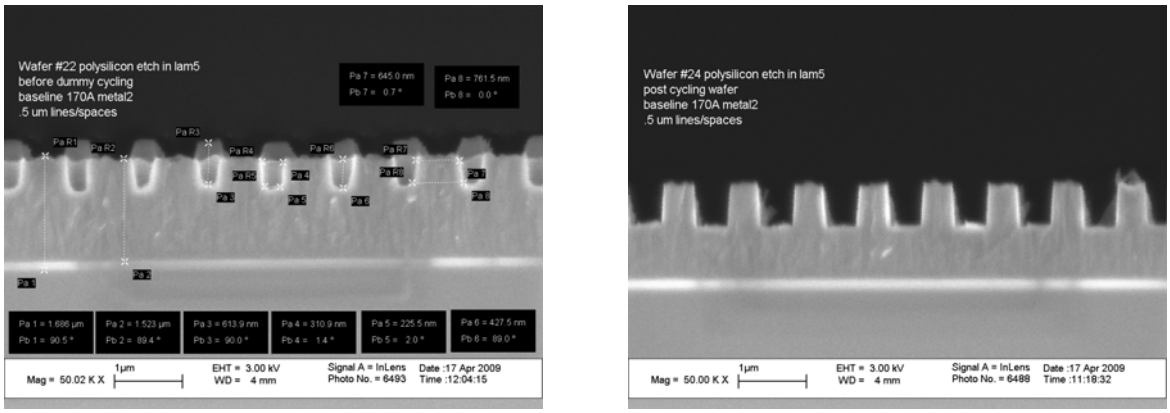
- ITO Process - This year Daniel Queen GRS working in the process group, embarked on an interesting project. Daniel compared indium tin oxide (ITO) film deposited in the Microlab (40 nm and 230 nm) to commercially available samples for, their transparency and conductivity characteristics (important parameters in building good photovoltaic devices). Daniel reported comparable transparency for the ITO film evaporated in our NRC machine,

as compared to 140 nm ITO films supplied by Delta Technologies and National Renewable Energy Lab (NREL). Optical transmission (I/I_0) of these ITO samples (Microlab and others) were comparable (>95% over the visible spectrum). Transparency values were obtained on the Sopra ellipsometer/spectrometer in the Microlab. The resistivity of ITO film from Microlab was also measured at 2.4×10^{-4} Ω·cm, which was comparable to data reported in the literature (good acceptable film comparable to commercially available products). Process parameters used for the Microlab ITO process in the NRC evaporator were as follows:

Source Material:	Indium -Sn (10 wt.%) 5N Purity ESPI Metals P/N: KNC6069	
Evaporation Source:	Boron nitride crucible (R.D. Mathis P/N: C1-BN) Tungsten Basket heater (R.D. Mathis P/N: B8A3X.030W)	
Base Pressure:	1×10^{-6} Torr	
O_2 Partial Pressure:	2.5×10^{-4} Torr	
Substrate Temperature:	175°C	
Filament Current:	50 A	
Deposition Rate:	18 Å/min	
Nominal Crystal Thickness Monitor Settings:	Density: Z-factor:	7.1 g/cm^3 0.439

- Daniel Queen's ITO report is currently available on our website:
  http://microlab.berkeley.edu/text/processreports/ITO.pdf
- New Developer - A new developer (MF26A) was fully tested and implemented to replace LDD-26W developer that had been used for our DUV lithography process up until February 2009. This was done to comply with the new Environmental Protection Agency (EPA) ruling, banning Perfluoroalkyl sulfonates (PFAS) in products such as LDD26W. The alternate product, MF26A without the PFAS (surfactant) offered the same level of performance as the LDD-26W developer, both in terms of CD control and minimum feature size resolved.
- New I-Line Resist - A new photoresist (OiR 700-10) was fully characterized to replace OCG OiR897 10i I-line resist that had been used for our standard I-line lithography process on GCAWS6, Karl Suss and other contact aligners up until February 2009. This was again due to EPA's ruling banning Perfluoroalkyl suffocates (PFOS) in products such as the OiR 897-10i resist. The new OiR 700-10 I-line resist developed slightly faster than the old OiR 897-10i resist; however, the performance of the two resists were identical (sidewalls, CDs, plasma etch resistance). Process staff (Kim) was able to resolve 0.6 µm lines with both the new and old I-line resist at the resolution limit of the GCAWS6 stepper. Program1 on SVGCOAT1 & 2 tracks were modified to coat about1.25 µm of the new resist at spin speed of 3200RMP for an optimal process.
- New HMDS Prime Program - Program2, a short version of our standard HMDS prime program1 was set up in the YES prime oven to eventually phase out the sink HMDS (bubbler) process. Kim experimented with both blank and resist pattern wafers and concluded that good resist adhesion and higher contact angles can be achieved in the prime oven; just as good if not better than Sink4 HMDS (bubbler), paving the way to eliminate the HMDS bubbler process in the new Marvell lab.
- Lam5 Poly Etch Issue - The Lam5 poly etch process was evaluated to address etch performance issues reported by the device group. A series of tests were performed to identify, ultimately to eliminate issues impacting high selectivity etch recipes in lam5.

This included etch rate, selectivity check, as well as etch profile study on samples etched, before and after cycling/etching 25 poly dummy wafers through the system (cleaning the chamber). Figure 2 and Table 2 below, showed noticeable etch uniformity and selectivity improvement, after cycling 25 poly dummy wafers through the system. It was also reported that the end point signals improved considerably by cycling poly dummy wafers through the system (stable signal). Good etch rate (3889 Å/min) and low etch non-uniformity (2.35%) were achieved by the main etch, as well as high selectivity to oxide and stable signal at the over etch step (228:1, poly:oxide).



(a) (b)

Figure 2 - SEM Image of Lines Spaces Etched Before (a) and After (b) Cycling 25 Dummies

Poly Etch Rate/Selectivity To Oxide, Before and After Cycling 25 Wafers (avg. of 3 wafers)

	Pre-Dummy Cycle		Post-Dummy Cycle			
	Poly		Poly		Oxide	
	Etch Rate (Å/min)	non-unif. (%)	Etch Rate (Å/min)	non-unif. (%)	Etch Rate (Å/min)	Selectivity Poly/Oxide
Main Etch	3889	11.26%	3229	2.35%	336	11.6
Over Etch	1580	12.69%	1775	7.54%	7	228

Table 2 - Poly Etch Rate/Uniformity

- A new distributor was approved for supplying our Tetramethylammonium Hydroxide (TMAH) based on the fact that they were able to offer the same chemical mix (25% TMAH in water), as was provided by our previous distributor no longer in a position to reliably supply us with the TMAH needed in the Microlab.

Lab Manual Update, Process Monitoring, & Qualification Tests

Last year, Process, BSAC, and Baseline Engineers updated all our lab manual chapters that had revisions older than 2 years; also wrote/released new qualification tests for newly installed tools.

New Qualification Tests

New qualification test for Centura-MET chamber was released.
New qualification test for Picosun ALD machine was released.

New and Rewritten Manual

Chapter 1.3 - New MOD38 for high quality indium tin oxide film deposition was added (03/09)
Chapter 5.8 - Initial write up of Tystar8, compound Semiconductor oxidation chapter (10/09).
Chapter 5.32 - Initial write up of the new Heatpulse2 machine (03/09).
Chapter 6.24 - Initial write up of Picosun Atomic Layer deposition chapter (02/09).
Chapter 6.30 - Complete rewrite of the PQECR PECVD deposition tool chapter (12/09).
Chapter 7.12 - Initial write up of Centura-MET, metal etch chapter (01/09).

Updated Manual Chapters

Chapter 1.3 - MOD 1-14 were reviewed and updated (08/09)
Chapter 1.3 - MOD 35 was reviewed and updated (02/09)
Chapter 1.8 - Compatibility of tools to 4" and 6" substrates was updated (03/09)
Chapter 1.10 - Miscellaneous etchant; Aqua Regia added, KOH/TMAH sections (4/09)
Chapter 2.1 - General cleaning procedure chapter update (08/09).
Chapter 2.7 - Minor changes made to sink7 chapter (08/09).
Chapter 2.13 - Notes added to section 8.0 and 9.13 in the Tousimis 815 chapter (10/09).
Chapter 2.14 - Notes added to section 8.0 and 9.13 in the Tousimis 915B chapter (10/09).
Chapter 3.3 - Updated sections 8.4 (commands), section 9.14 of pattern generator (02/09).
Chapter 3.4 - Updated sections 6.0, 9.14, 9.1.5, 9.2.5 of APT emulsion mask chapter (11/09).
Chapter 3.5 - Updated sections 9.0, 9.2, 9.3.8 of APT chrome mask chapter (11/09).
Chapter 3.6 - Updated sections 3.0, 9.1.4, 9.2, 9.2.5 of iron oxide mask chapter (11/09).
Chapter 4.12 - Updated sections 8.1 of GCA 8500 Wafers stepper chapter (11/09).
Chapter 4.14 - Updated sections 9.6.5 of Karl Suss MA6 mask aligner chapter (07/09).
Chapter 4.15 - Added focus setting and wafer disk size to Canon mask aligner chapter (09/09).
Chapter 4.16 - Updated with notes and added figures to Quintel mask aligner chapter (04/09).
Chapter 4.25 - Reviewed and updated svgdev chapter (11/09).
Chapter 4.26 - Updated Table3, and PEB programs in SVGDEV6 chapter 05/09).
Chapter 4.27 - Reviewed and made minor update of UVbake chapter (08/09).
Chapter 4.29 - Reviewed and performed minor editing of the HMDS chapter (02/09).
Chapter 5.0 - Reviewed and made minor revisions to furnace overall chapter (09/09).
Chapter 5.2 - Minor revision to sections 8.4, 9.2.1.3, and 9.5.11 of Tystar2 chapter (02/09).
Chapter 5.3 - Minor revision to sections 8.4, 9.2.1.3, and 9.5.11 of Tystar3 chapter (02/09).
Chapter 5.4 - Minor revision in 8.3, 8.8- 8.11, 9.2.1.3 and 9.5.11 of Tystar4 chapter (02/09).
Chapter 5.5 - Minor revision to Tystar5 (10/09).
Chapter 5.6 - Minor revision to Tysta6(10/09).
Chapter 5.7 - Minor revision to Tysta7(10/09).
Chapter 5.10 - Minor revision to sections 5.8, 7.1, 9.1 and 9.2.4 of Tystar10 chapter (02/09).
Chapter 5.12 - Minor revision to sections 5.12, 7.1, 9.1 and 9.2.4 of Tystar12chapter (02/09).
Chapter 5.14 - Minor revision to section 8.7 of Tystar14 chapter (10/09).
Chapter 5.15 - Added Methyl silane and H2 to available gases in Tystar15 chapter (10/09).
Chapter 5.19 - Major changes in various sections of the Tystar19 chapter (02/09).
Chapter 5.33 - Added sections 8.4 added notes for TC and EPR to Heatpulse3 (03/09).
Chapter 5.34 - Added sections 8.4 and temp calibration to Heatpulse4 chapter (02/09).
Chapter 5.35 - Modified section 8.11 of the Nanox furnace chapter (09/09).
Chapter 5.36 - Updated idle temperature in YES prime oven chapter (03/09).
Chapter 6.01 - Updated and reformatted numbering of Hummer chapter (03/09).
Chapter 6.02 - Added paragraph 9.1.3 to Novellus m2i chapter (07/09).
Chapter 6.03 - Removed pd from target list of Randex chapter (04/09).
Chapter 6.04 - Moved sputter reference to appendix, minor changes to CPA chapter (04/09).

Chapter 6.07 - instruction added for new clamp down ring to Edwards sputter chapter (06/09).
Chapter 6.08 - Updated operational instructions and rules for AMS, AlN chapter (03/09).
Chapter 6.11 - Added Appendix sections 12.2 and 12.3 to NRC chapter (03/09).
Chapter 6.22 - Added Safety procedure and pictures to parylene chapter (7/09).
Chapter 6.23 - Updated section 8 and parameters in appendix in AMST MVD chapter (03/09).
Chapter 6.28 - Updated and added section 9.3.6 to AMAT P5000 chapter (07/09).
Chapter 7.2 - Minor changes made to Lam2 chapter (06/09).
Chapter 7.3 - Minor changes made to Lam3 chapter (06/09).
Chapter 7.4 - Minor changes made to Lam4 chapter (06/09).
Chapter 7.5 - Minor changes made to Lam5chapter (06/09).
Chapter 7.6 - New endpoint detection guideline was added to Centura Mxp+ chapter (01/09).
Chapter 7.7 - Modified Centura DPS chapter and new chamber configuration added (07/09).
Chapter 7.8 - Major update and modification to STS chapter was made (02/09).
Chapter 7.9 - Modified section 8.0 & added oxide, nitride recipes to Ptherm chapter (02/09).
Chapter 7.11 - Minor text edit to Technics-c chapter (09/09).
Chapter 7.13 - Added section 10.6 in troubleshooting guidelines for XeF2 chapter (04/09).
Chapter 8.05 - Updated hardware & wafers set up in Electroglass Auto Probe chapter (01/09).
Chapter 8.23 - Minor text changed made to UVscope chapter (07/09).
Chapter 8.24 - Added section 10.2 to MEMSscope chapter (01/09).
Chapter 8.32 - Added the Appendix section to Ellipsometer chapter (03/09).
Chapter 8.42 - Review and minor editing throughout the text (08/09).
Chapter 9.2 - Edited 9.1.2, 9.1.4, 9.2.1, 9.4.5, 9.5.5 and 9.5.10 of KS-SB6 chapter (07/09).
Chapter 10.1 - Modified sections 9.7, 9.8 and 9.9, Min. down force in CMP chapter (07/09).

Process Monitoring, Equipment Training, Member Qualification, & Test Grading

Last year our student helpers continued their excellent service and support of the Microlab by preparing dummy wafers at different stations, cleaning boats in furnaces, and running test monitors on our baseline tools in a very timely manner. Jimmy has directly managed their activities in the lab, also provided support/training for the new student hire, whenever it was needed.

A large number of equipment qualification were performed this past year, written test (graded), and oral tests were given by staff for a number of tools. The BSAC and baseline engineers, also provided great support in the DRIE etch, metrology, and CAD layout/ mask making areas. I assigned superusers on various tools and helped administration staff reinstate some of our members on their expired equipment qualification.

V. PROCESS STAFF SUPERVISION, TRAINING & OTHER SERVICES

Staff Supervision & The New Job Definition

I continued my supervision of Process/MEMS-Exchange Engineers, one baseline assistant specialist, as well as one graduate student researcher (GSR 25%), and two undergraduate assistants working in the process group. Process staff yearly appraisals were submitted on time, before the September 1st deadline. I also revised our job titles to see them through acceptance by the HR department/University. All engineers in my group have successfully been mapped to their respected categories (accepted!).

Promotion & Awards

This year Marilyn and her student lab assistant, Greg Michael, were both recognized for their efforts, service and support of the Microlab by receiving ERSO's "SPOT" award. I was also honored by becoming one of the recipients of the "Excellent in Management Award" on Campus, nominated by colleagues and selected by the Berkeley Staff Assembly (BSA). The theme for this year award was "Embracing the Inevitable…Change".

High School Interns

The Microlab was able to continue its 8 year old summer internship program with three new high school students; Anjana Bala and Sarah Ip, our two interns in the process group and Christopher McNally in the equipment engineering group. Jimmy Chang (senior process engineer) and Daniel Queen (PhD candidate) provided mentorship, also helped our interns conduct their aluminum deposition experiments on various tools in the Microlab. The result of their work was presented to the Microlab staff and guests at the conclusion of their summer internship, now available at the following link:

http://microlab.berkeley.edu/text/participants.html

Microlab, EE143 (UCB)

Process staff continued their service/support of the EE143 lab and by ordering new furnace boats, supplying the class with their chemical needs, and helping TAs with their poly/oxide runs.

Member Advising, Help/Support of Other Universities, Institutions

- Helped one of our BLMA engineers with a special application job to read off the position of printed PM marks within each flash field (Grid on his wafer) on the ASML. This required changing the layout design to include PM marks in all exposure fields, as well as a special application job to first print and then read the position of PM marks as a measure of local alignment and rotation offsets within each exposure field, and finally plot the vector results.
- Helped a colleague at Stanford with her request to etch PM marks on 15 wafers (5 groups of 3 each targeting different etch depth: 1200 Å, 2400 Å, 3600 Å, 4800 Å, and 6000 Å).
- Helped one the graduate student at Stanford looking for a good conformal PECVD oxide, a better alternative to their STS machine. We processed his samples in our Oxford2 and in return, he shared his data/results with us. It was concluded that the Berkeley and Stanford PECVD oxide processes were somewhat identical, an artifact of the type of tools available at these sites, hence, could not offer any advantage/s in performing his run/s here.

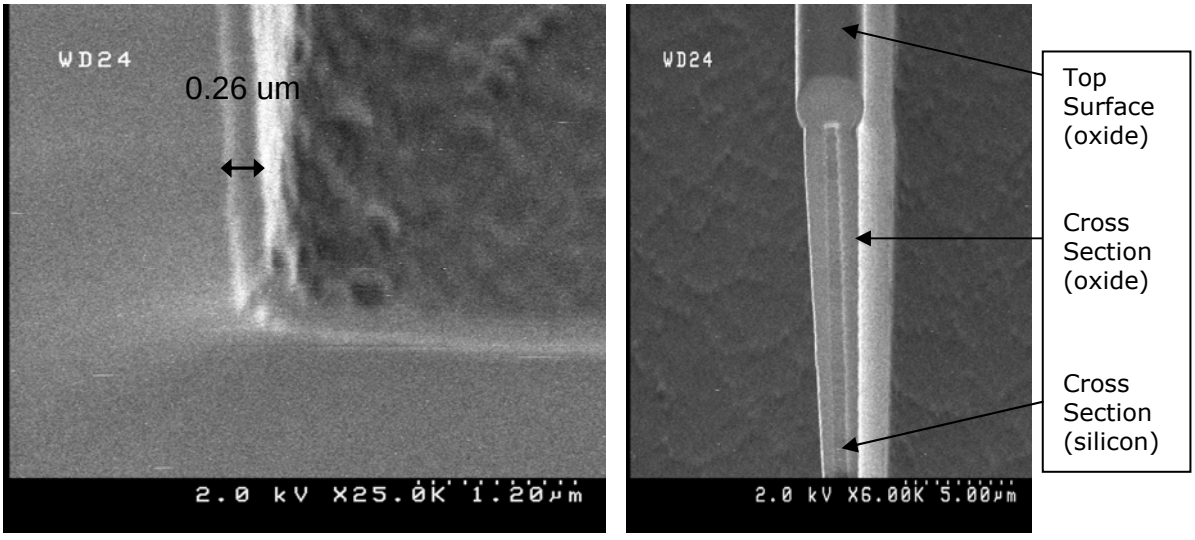


Figure 3 - SEM Cross-Section of a Structure Covered by Oxford2 PECVD Oxide (45º tilt)

- Sent a copy of our GCA stepper manual to Prof. Jackson at Penn State University.
- Processed EE146A wafers from University of California at Davis, and deposited 6KÅ of undoped poly, part of the process used for their fabrication of MOS devices in their class.
- Held weekly meetings with process staff, discussed Microlab issues, projects, new lab agenda; tool support and process implementation on the new and relocated tools.

VI. SEMICONDUCTOR PROCESSING & SPECIAL SERVICES

ETR Services

Last year process staff completed 13 engineering test requests (ETRs) generating $19,763 in revenue for the Microlab. In addition to the standard processing normally offered in the litho, etch and diffusion areas, we performed non-baseline processes such as ALN deposition on Molybdenum (provided rocking curves), ITO deposition on glass samples cleaned by O2 plasma, as well as amorphous silicon + aluminum deposition on glass substrates + ITO dots.

MEMS-Exchange Process Services

Last year we wound down our services/support of the MEMS-Exchange program, with one local MEMS-Exchange (MX) engineer, half time at our site.

Mask Making Services

A total of 643 new masks were processed on the pattern generator for internal (UCB researchers and BMLA), as well as external customers (other Universities) in 2009.

Special Requests/ other Services

Staff supplied the Microlab office with pocket wafers, poly-Si control wafers for general use and two sets of 25 pocket wafers that were fabricated in February and September of 2009. Also, we made several show wafers as presents for College of Engineering distinguished visitors.

VI. CMOS BASELINE ACTIVITIES

Baseline Run (0.35 µm Process)

Laszlo Petho our baseline engineer completed the latest 0.35 µm CMOS baseline run (5th six-inch run). Table 3 below shows average value for some of the device parameters measured on transistors, and circuits in this run, which also yielded nicely with 0.3 µm P-channel and N-channel devices (below intended design rules) in Figure 4. Threshold voltage on these devices had tight distribution, shown in Figure 5. Hot aluminum process was tried out on one group of wafers at metal1 deposition step, which yielded better than the standard aluminum process group, also for the first time enabled functional circuits at our more aggressive designs/layouts with submicron contact sizes (0.7 µm contact never worked before on our previous runs!). Figure 6 shows oscilloscope measurement of operating frequency for one of the fastest ring oscillators ever on baseline runs (f = 309 MHz), and Figure 7 an image of CMOS-192 test chip.

No.	Parameters	Units	NMOS	PMOS
1	Vt	V	0.46	-0.48
2	Sub Threshold Slope	mV/decade	95	85
3	Ring oscillator frequency (31 stages, 1.0 µm gate, 3.3V)	MHz	70.8	
4	Ring oscillator frequency, fastest (31 stages, 0.35 µm gate, 3.3V)	MHZ	309.1	

Table 3 - Device Parameters for CMOS192 (W = 2.5 µm and L = 0.3 µm)

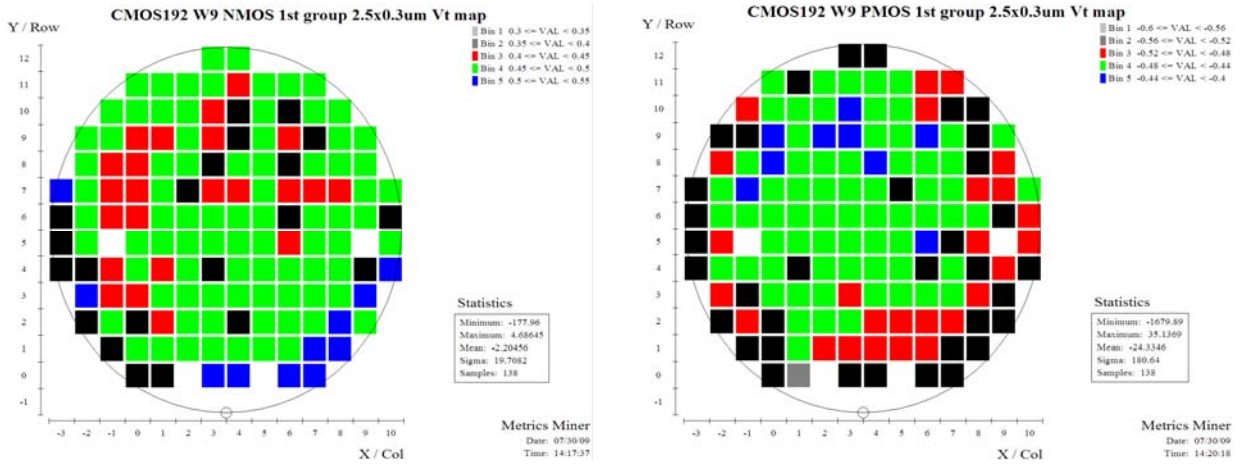


Figure 4 - VT Distribution Map of N and P MOSFETs on a Wafer (W = 2.5 µm and L = 0.3 µm)

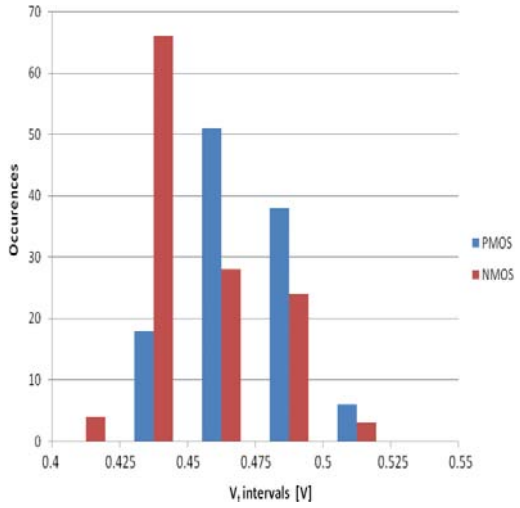


Figure 5 - Pareto Chart of N and P Channel VT (W = 2.5 µm and L = 0.3 µm)

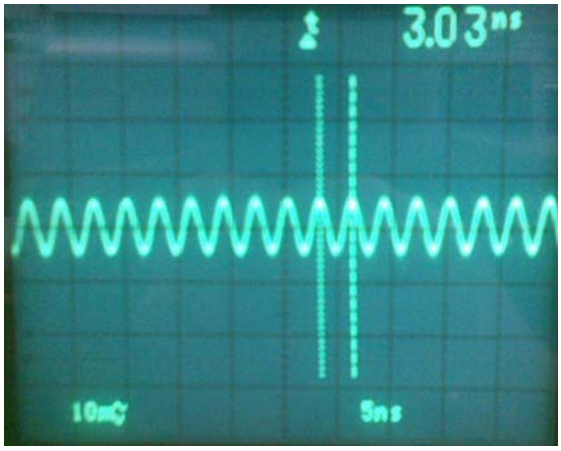


Figure 6 - One of the Faster Ring Oscillators on the Test Chip (W = 2.5 µm and L = 0.3 µm)

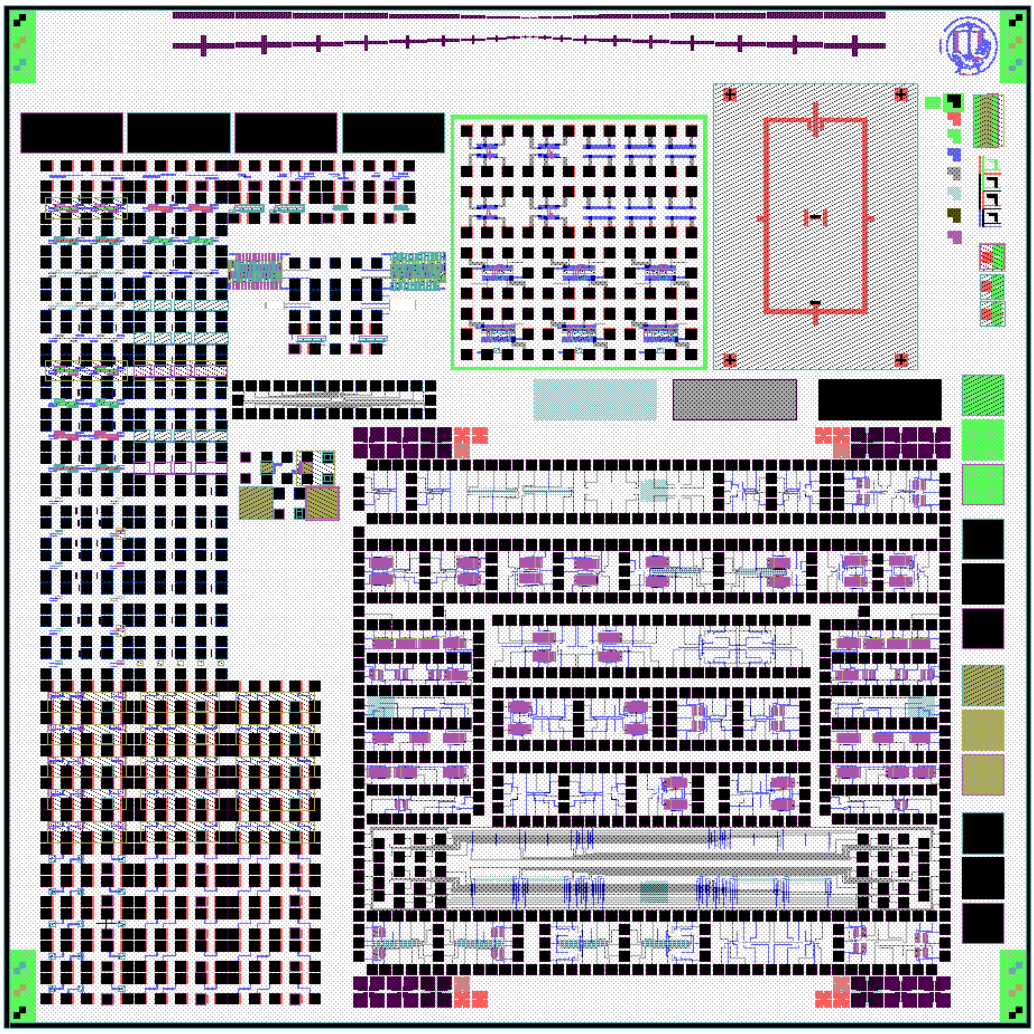


Figure 7 - Baseline CMOS192 Test Chip

A copy of CMOS-192 report is currently available online at the following link:
http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-163.html

VII. REPORTS, PUBLICATIONS & SEMINARS

- A new ITO process report from Daniel Queen was added to process related section of our website: http://microlab.berkeley.edu/text/processreports/ITO.pdf
- Lam5 evaluation - system performance and baseline data was compiled on a Memorandum, which was submitted to Operation Manager and PIs on 04/22/2009.
- The latest 0.35 µm baseline report (CMOS-192) was submitted by Laszlo Petho (12/2009).
- Process staff attended BSAC IAB seminars In March and September of 2009 (1/2 day).
- Process staff attended the Semicon West exhibition in July 2009.
- Process staff attended the Solid State Technology and Devices Seminars on Fridays.