Future Chip Technology Scaling for Big Data and Cloud Computing

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Abstract

CMOS scaling enables smaller, faster, cheaper and more energy efficient chip technology for computing. Conventional planar CMOS scaling approaches limit due to leakage issue from short channel effects. FinFET enables new robust low-Vdd design. In this talk, we discuss several FinFET development efforts at IBM such as multiple Vt strategy, parasitic R/C, variability. We will then introduce the research on new materials and device architectures such as Si Nanowire, III-V channel, SiGe channel and Carbon Nanotubes. The talk will also discuss neuromorphic computing and quantum computing that could enable extremely power-efficient and fast computation system for the future.

Biography

Dr. Chung-Hsun Lin received his Ph.D. degree in Electrical Engineering from the University of California, Berkeley in 2007. His Ph.D. work on FinFET compact modeling with colleagues at UC Berkeley led to the world first and only industrial standard FinFET SPICE model – BSIM-CMG. After graduation, he joined IBM T.J. Watson Research Center. He currently manages both Exploratory Device Research group and 14nm SOI FinFET development device group. Dr. Lin has authored or coauthored more than 60 technical papers and holds more than 43 US patents. He was elected IBM Master Inventor in 2012 for outstanding contribution to corporate IP portfolio.