L-shaped TFET for High Current Drivability and Low Subthreshold Swing

Sang Wan Kim

Department of electrical engineering and computer sciences, University of California at Berkeley

Abstract:

A tunnel field-effect transistor (TFET) has been regarded as one of the promising alternatives for a metal-oxide-semiconductor FET (MOSFET) for extremely-low-power applications. Theoretically, TFET can achieve sub-60 mV/dec subthreshold swing (*S*) at room temperature and maintain on-off current ratio while scaling down supply voltage. However, most of experimental results have shown worse current drivability and *S* than predicted. Thus, several novel strategies should be investigated.

In this talk, an L-shaped TFET which features band-to-band tunneling (BTBT) perpendicular to the channel direction will be demonstrated. It is different from other vertical-BTBT-based TFETs in that it maintains high scalability with the help of mesa structure. It shows ~10x higher on-current than that of conventional TFETs. It is attributed to more abrupt on-off transition and larger tunnel junction area. Because the proposed device structure and epitaxy-based process flow are compatible with heterojunction structure, further on-current boosting is feasible if narrow band gap materials such as SiGe, Ge and compound semiconductors are used.

Biography:

Sang Wan Kim is a postdoctoral scholar at the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, since Aug. 2014. He received his B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 2006, 2008, and 2014, respectively. He had been a Research Assistant of process integration and a Teaching Assistant of oxidation and diffusion processes at the Inter-University Semiconductor Research Center (ISRC), SNU, from 2010 and 2008 to 2014, respectively. He is an inventor of 8 patents and author or coauthor of more than 90 research papers for journals and conferences. His current research interests include the design, fabrication, measurement, characterization, and modeling of nanoscale CMOS/CMOS compatible devices, nanoelectromechanical (NEM) devices, negative capacitance FETs, thin-film transistors, and neuromorphic systems.