Title: Negative capacitance for ultra-low power beyond CMOS devices

Speaker:
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Abstract:
Fundamental physical limits of the transistor operation have put the electronics industry into a power dissipation bottleneck, which led to an industry-wide call for "reinventing the transistor." In this talk, I will discuss a fundamentally new device, the negative capacitance field-effect-transistor (NCFET), in which a gain mechanism introduced by a ferroelectric gate oxide can lower the power dissipation below the physical limit set by the Boltzmann distribution. Despite the strong interest, experimental realization of ferroelectric negative capacitance has remained challenging and elusive-thanks to the non-equilibrium nature of the negative capacitance. In the first part, I will describe our recent experiment, which led to the first direct measurement of negative capacitance in an isolated thin, epitaxial ferroelectric film at the room temperature. In a series combination of a resistor and a ferroelectric capacitor, we observed that upon the application of voltage pulse, the voltage across the ferroelectric decreases for an increasing charge–in exactly the opposite direction to which voltage for a regular positive capacitor should change. Using similar examples, I will motivate the idea that such circuit theoretic approaches present unprecedented insights into some of the most important and unresolved questions in ferroelectrics/multiferroics and strongly correlated materials and are vital for rapid identification and prototyping of negative capacitance materials.

In the second part of the talk, I will discuss recent advances in and challenges for NCFET design, heterogeneous integration of complex oxide ferroelectrics with semiconductors and fabrication of negative capacitance transistors on the CMOS platform. I will also give a brief overview of the overall landscape of negative capacitance research worldwide. I will end the talk with a general guideline for finding negative capacitance in alternative non-ferroelectric materials and nanoscale systems.

Biography:
Asif Khan is a PhD candidate in Electrical Engineering at UC Berkeley working in the Laboratory for Emerging & Exploratory Devices (LEED) advised by Prof. Sayeef Salahuddin. He is also a member of the research groups led by Prof. Ramamoorthy Ramesh and Prof. Chenming Hu. His current research focuses on ferroelectricity & nano-ferroelectronics for ultra low power beyond CMOS electronics. The work led by him in the LEED group resulted the first experimental proof-of-concept demonstration of ferroelectric negative capacitance in nanoscale crystalline heterostructures, a novel physical effect proposed in 2008 that can help to beat the "Boltzmann Limit" of 60 mV/dec subthreshold swing in nanoscale CMOS transistors. His research interests lies in combining techniques from engineering, physics,

material science and neurosciences for new frontiers in computing.

Prior to Berkeley, Asif received his BS in Electrical & Electronic Engineering from Bangladesh University of Engineering & Technology (BUET) in 2007. He was awarded the Qualcomm Innovation Fellowship 2012, the Silver prize at the 5th TSMC Outstanding Student Research Award in 2011, the University Gold medal (class of 2007) from BUET by the Hon'b President of Bangladesh in 2011, Kintarul Haque Gold Medal (class of 2007) from BUET in 2011, Select Delegate Award to represent Bangladesh at the 58th Lindau Meeting of Physics Nobel Laureates in 2008, the 1st prize in IEEE R-10 Student Paper Contest in 2006 and the 2nd prize in the IEEE History Student Paper Contest in 2004.