

## Technology Inflection Points: Planar to FinFET to Nanowire

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### Abstract:

Analysis of transistor architecture, material engineering, and library cell design for 7nm and 5nm technology nodes. Mechanical stability of tall and narrow fins is an increasing issue that drives transistor architecture choices and suggests transition from FinFETs to gate-all-around nanowires at 5nm node. Comparative analysis of group IV and III-V FinFETs for High Performance, Standard Performance, and Low Power technology options shows that non-Si channels can beat Si by ~2x for HP, but are too leaky for LP. The Middle-of-Line parasitic RC dominates ring oscillator performance and prompts investment into interconnect material engineering and gate-all around nanowires. Holistic library cell design (mechanics + transistor on/off + parasitic RC + circuit performance) is introduced. Benchmarking two-input NAND library cells based on quadruple patterning Si 7nm FinFETs, Ge SOI 7nm FinFETs, and EUV+DSA Si 5nm vertical nanowires exhibits 4x performance advantage of the 5nm vertical nanowire technology with simultaneous 5x dynamic power reduction.

### Bio:

Dr. Victor Moroz is a Synopsys Scientist, engaged in a variety of projects on modeling FinFETs, gate-all-around nano-wires, stress engineering, 3D ICs, transistor scaling, Middle-Of-Line and Back-End-Of-Line RC, solar cell design, innovative patterning, random and systematic variability, junction leakage, non-Si transistors, and atomistic effects in layer growth and doping. Several facets of this activity are reflected in three book chapters and over 100 technical papers, invited presentations, and patents. Has been involved in technical committees at ITRS, IEDM, SISPAD, DFM&Y, ECS, IRPS, and ESSDERC.