

Title: Wafer Inspection

Abstract: Integrated circuit (IC) devices are an integral part of today's life, and the demand for better, lower cost IC devices continue to grow. Wafer inspection is an important step which semi-conductor fabrication plants adopt to uncover design or process problems to ensure IC devices meet high performance design and yield targets. Today, wafer inspection steps are injected in both R&D and high volume production phases in the development cycle. As design node shrinks, the size of defects causing IC devices to fail also shrinks. This leads to higher sensitivity requirement for wafer inspector node after node. The sensitivity target for current generation is aimed at finding defects on the order of 10nm. Not only is sensitivity a key, wafer inspector must also complete inspection in tight time frame so the development process can be monitored in real time. In this presentation, we will discuss the challenges wafer inspectors face and the technologies enabling successful wafer inspection.

Bio: Grace Chen is a Sr. Director of System Engineering at KLA-Tencor. She leads the R&D development at KLA-Tencor, focusing on wafer inspection. Prior to KLA-Tencor, Grace lead the numerical simulation development for phase-shift mask at Numerical Technologies and developed innovative methods to automatically identify small objects from panoramic images obtained from satellites at Innovative Imaging Systems. Grace came to US from Taiwan to become a concert pianist but switch to study physics later. She received her Ph.D. in Physics from MIT.