There's Plenty of Room at the Bottom - and at the Top

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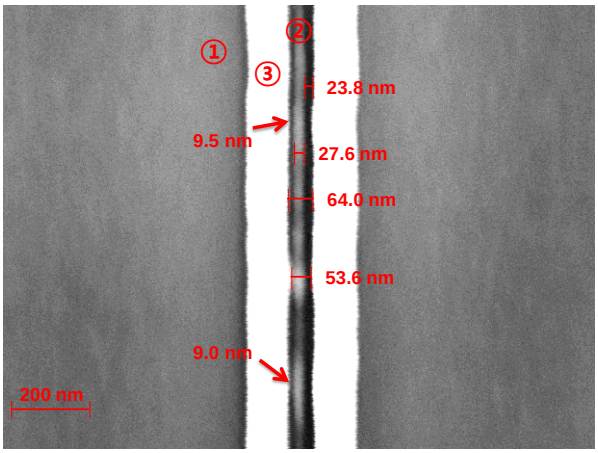
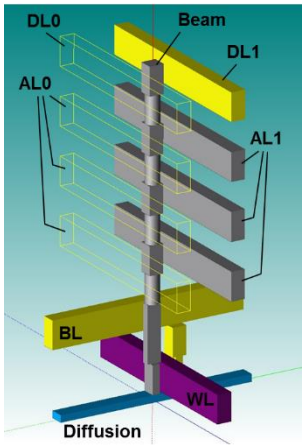
December 2, 2016

Abstract

The virtuous cycle of integrated-circuit (IC) technology advancement has been sustained for over 50 years, resulting in the proliferation of information and communication technology with dramatic economic and social impact. Industry experts predict that the pace of increasing transistor density will slow down dramatically within the next 5 years, however, due to fundamental limits of the conventional photolithographic patterning process. Scaling of IC feature sizes beyond the resolution limit of lithography has been enabled by multiple-patterning techniques, but at significant incremental cost. In the first part of this seminar, I will describe a more cost-efficient approach for defining sub-lithographic features, to help extend the era of Moore's Law.



Beyond Moore's Law, the proliferation of mobile electronic devices and the emergence of applications such as wireless sensor networks and the Internet of Things have brought energy consumption to the fore of challenges for future information-processing devices. The energy efficiency of a digital logic integrated circuit is fundamentally limited by non-zero transistor off-state leakage current. Mechanical switches have zero leakage current and potentially can overcome this fundamental limit. In the second part of this seminar, I will describe recent progress toward realizing the promise of ultra-low-power mechanical computing.



Biography:

Tsu-Jae King Liu received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University. From 1992 to 1996 she was a Member of Research Staff at the Xerox Palo Alto Research Center (Palo Alto, CA). In August 1996 she joined the faculty of the University of California, Berkeley, where she currently holds the TSMC Distinguished Professorship in Microelectronics in the Department of Electrical Engineering and Computer Sciences and serves as Associate Dean for Academic Planning and Development in the College of Engineering.

Dr. Liu's research awards include the DARPA Significant Technical Achievement Award (2000) for development of the FinFET, the IEEE Kiyo Tomiyasu Award (2010) for contributions to nanoscale MOS transistors, memory devices, and MEMs devices, the Intel Outstanding Researcher in Nanotechnology Award (2012), and the Semiconductor Industry Association Outstanding Research Award (2014). She has authored or co-authored 500 publications and holds over 90 U.S. patents, and is a Fellow of the IEEE. Her research activities are presently in advanced materials, process technology and devices for energy-efficient electronics.