Title: Forget about SoCs – Let's talk about SoWs (System on Wafer)

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Abstract:

Silicon features have scaled by over 1500X for over five decades, and with the adoption of innovative materials delivered better power-performance, density and till recently, cost per function, almost every generation. This has spawned a vibrant system-on-chip (SoC) approach, where progressively more function has been integrated on a single die. The integration of multiple dies on packages and boards has, however, scaled only modestly by a factor of three to five times. However, as SoC's have become bigger and more complex, the Non-Recurring Engineering Charge and time to market have both ballooned out of control leading to ever increasing market consolidation. At UCLA CHIPS, we are trying to address this problem through novel methods of system Integration. We show that with the apparent slowing down of semiconductor scaling and the advent of the Internet of Things, there is a focus on heterogeneous integration and system-level scaling. Packaging is undergoing a transformation that focuses on overall system performance through integration rather than on packaging individual components. We propose ways in which this transformation can evolve to provide a significant value at the system level while providing a significantly lower barrier to entry compared with a chip-based SoC approach that is currently used. More importantly it will allow us to re-architect systems in a very significant way. This transformation is already under way with 3-D stacking of dies and will evolve to make heterogeneous integration the backbone of a new SoC methodology, extending so we can integrate entire Systems on Wafers (SoWs). We will describe the technology we use and the results to-date. This has implications in redefining the memory hierarchy in conventional systems and in neuromorphic systems. Additionally, we will look at anew at conventional devices and explore new ways to use them in in memories, neuromorphic computing, fault-tolerance and repair applications in the CHIPS context. We extend these concepts to flexible and biocompatible electronics.