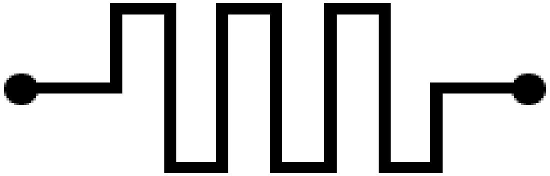
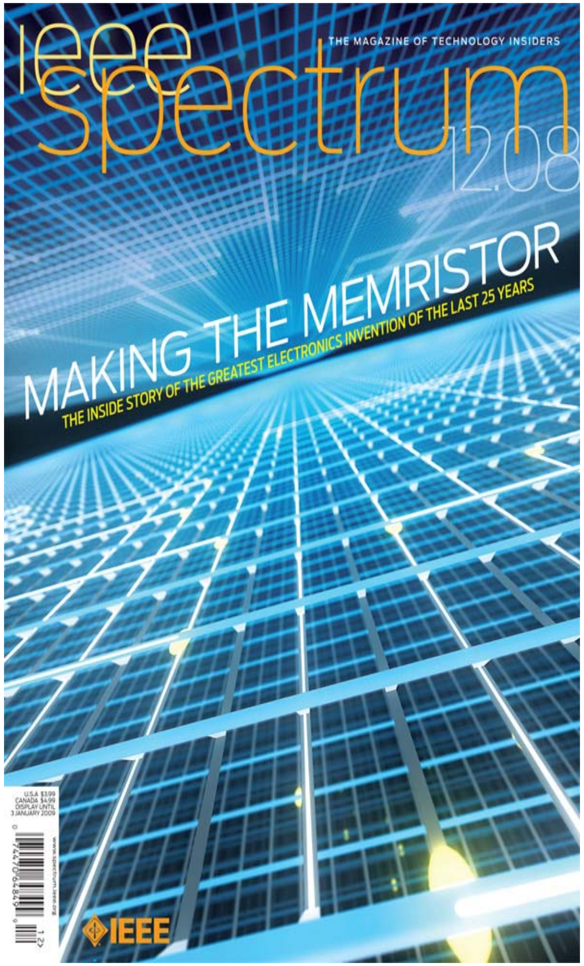
Resistive RAM: Technology and Market Opportunities



Deepak C. Sekar
MonolithIC 3D Inc.

RRAMs/Memristors have excited many people…



IEEE Spectum:

“The greatest electronics invention of the last 25 years”

Time Magazine:

“One of the best inventions of 2008”

This presentation:

- Explains RRAM Technology and Applications
- Are IEEE Spectrum and Time right to be excited?

  After this talk, you judge!

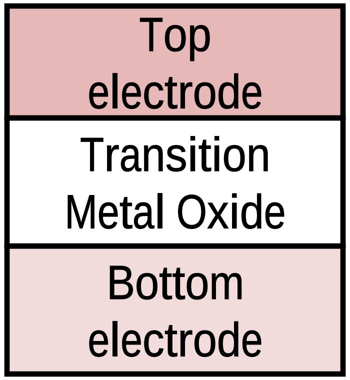
Outline

- Introduction
- Mechanism
- Switching Optimization
- Array Architectures and Commercial Potential
- Risks and Challenges
- Conclusions

Outline

- Introduction

Device Structure


Top electrode

Transition Metal Oxide

Bottom electrode

	Examples
Top electrode	Pt, TiN/Ti, TiN, Ru, Ni …
Transition Metal Oxide	TiO_x, NiO_x, HfO_x, WO_x, TaO_x, VO_x, CuO_x , …
Bottom Electrode	TiN, TaN, W, Pt, …

- Many types of RRAM exist
- Transition Metal Oxide RRAM (above) seems most popular → focus of this talk

RRAM compared with other switching materials

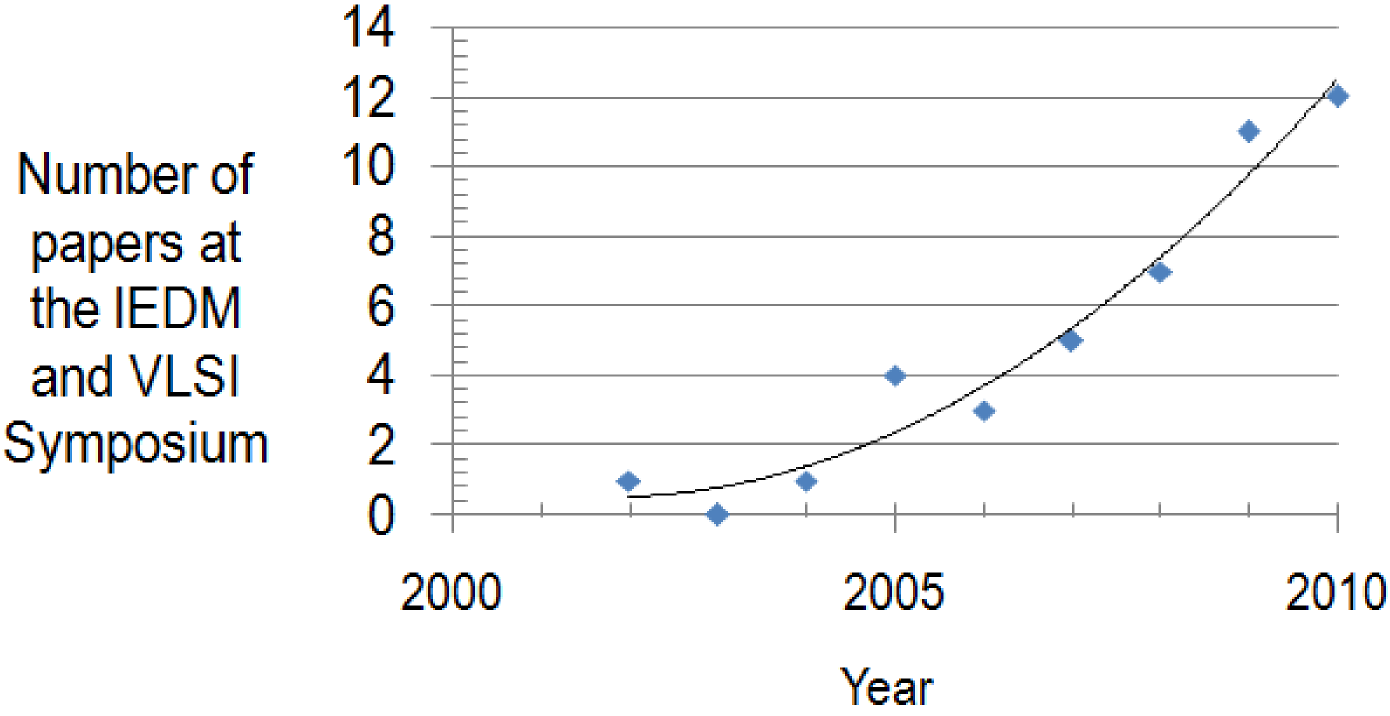
Single cell @ 45nm node	Phase Change Memory	STT-MRAM	RRAM
Materials	TiN/GeSbTe/TiN	Ta/PtMn/CoFe/Ru/CoFeB/MgO/CoFeB/Ta	TiN/Ti/HfO_x/TiN
Write Power	300uW	60uW	50uW
Switching Time	100ns	4ns	5ns
Endurance	10^{12}	$>10^{14}$	10^6, 10^{10} reported in IEDM 2010 abstract
Retention	10 years, 85°C	10 years, 85°C	10 years, 85°C

Ref: PCM – Numonyx @ IEDM'09, MRAM: Literature from 2008-2010, RRAM – ITRI @ IEDM 2008, 2009

Simple materials, low switching power, high-speed, endurance, retention:

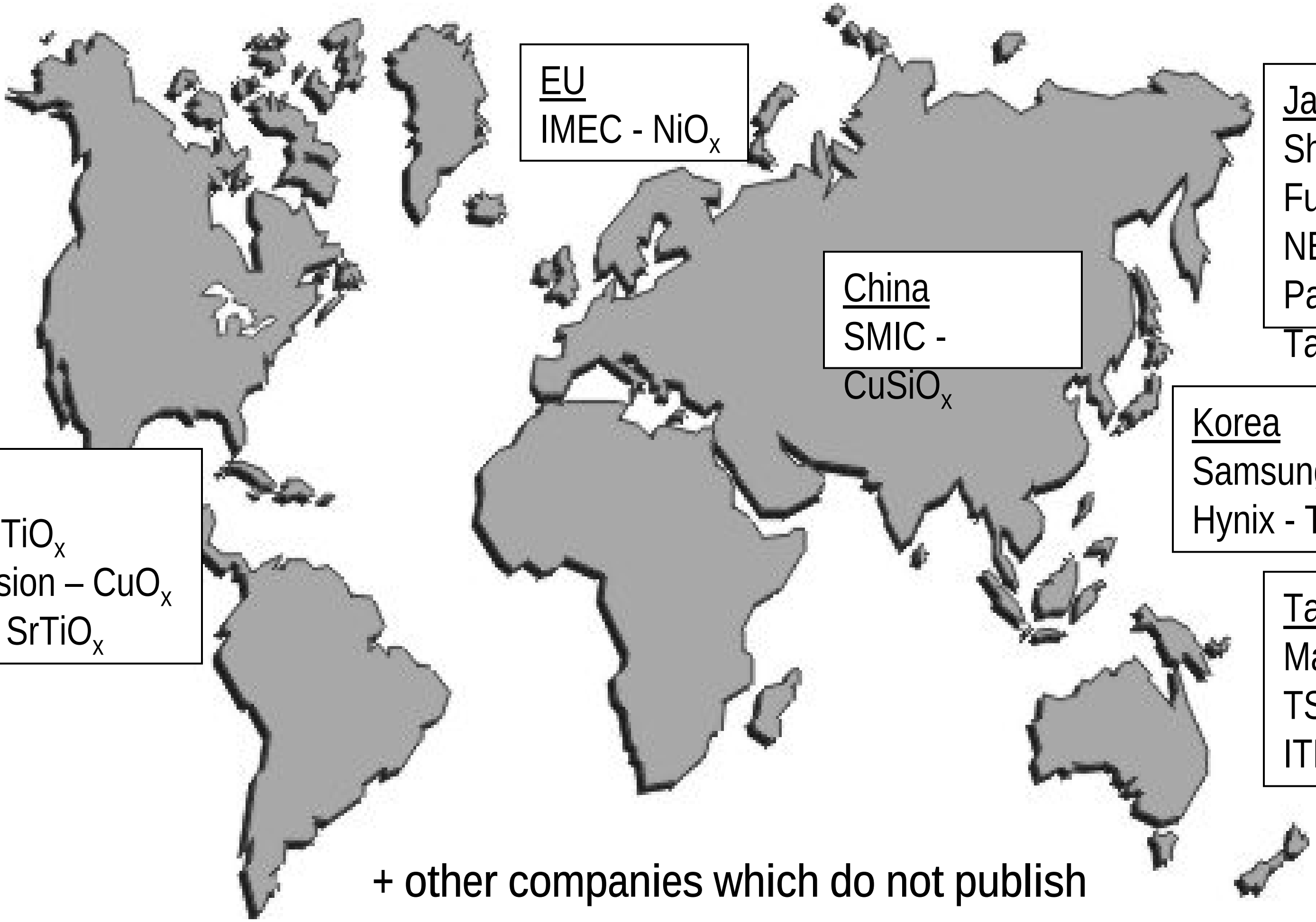
RRAM could have them all. One key reason for the excitement…

RRAM in the research community



Steadily increasing interest

Industry players developing transition metal oxide RRAM



US
HP – TiO_x
Spansion – CuO_x
IBM - $SrTiO_x$

EU
IMEC - NiO_x

China
SMIC - $CuSiO_x$

Japan
Sharp - TiON
Fujitsu – NiO_x
NEC - TaO_x
Panasonic – TaO_x

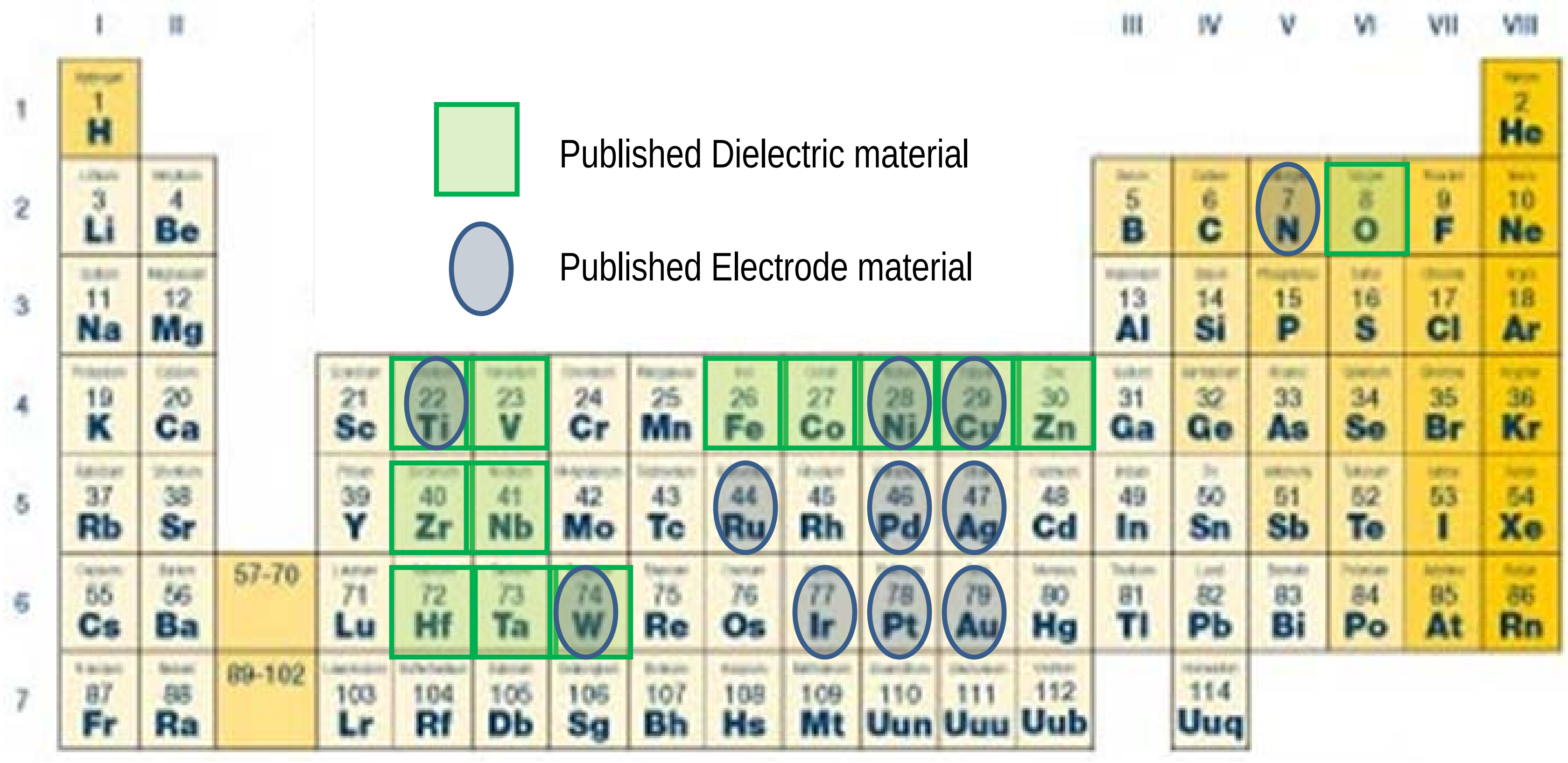
Korea
Samsung - NiO_x
Hynix - TiO_x

Taiwan
Macronix - WO_x
TSMC – TiON
ITRI - HfO_x

+ other companies which do not publish

Based on published data and publicly available info

The periodic table → a playground for RRAM developers



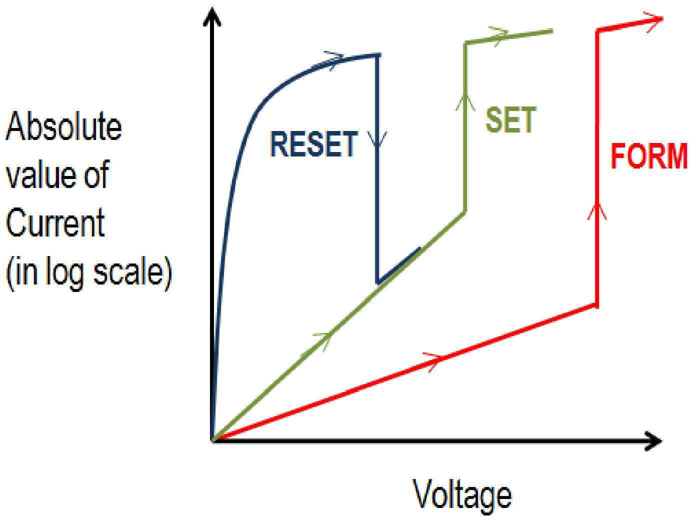
Which materials switch better? Can hopefully answer at the end of this talk…

Outline

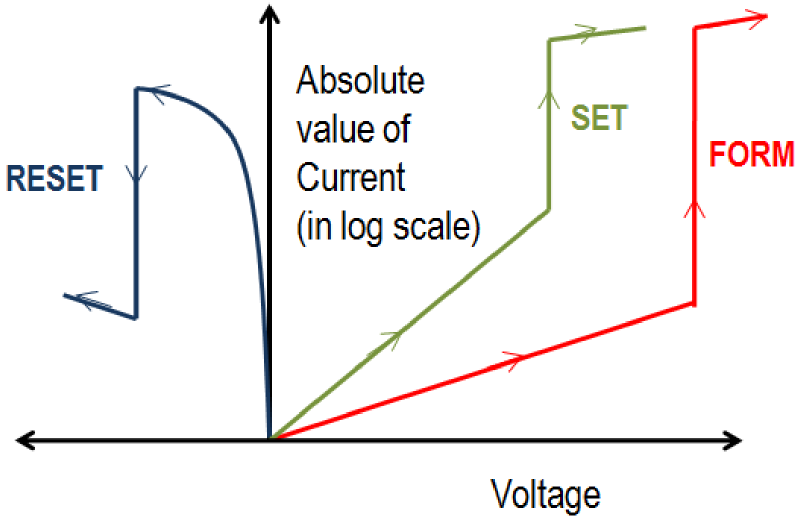
- Mechanism

RRAM Switching

- FORM: Very Hi Z → Lo Z. Highest Voltage, Done just once at the beginning.
- RESET: Lo Z → Hi Z, SET: Hi Z → Lo Z



Unipolar switching:
All operations same polarity



Bipolar switching:
RESET opposite polarity to SET and FORM

Switching Mechanism

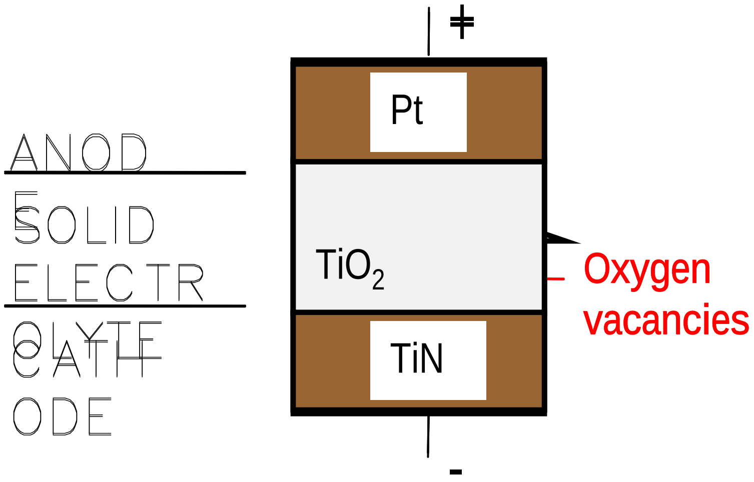
- RRAM switching mechanism not yet fully understood

- In next few slides, will present best understanding so far (with evidence) for

1) FORM
2) RESET
3) SET

for oxygen ion conduction RRAMs

Understanding FORM



BEFORE FORM
DURING FORM
AFTER FORM

On applying forming voltage,

@Cathode: $TiO_2 + 2xe^- \rightarrow TiO_{2-x} + xO^{2-}$

@Anode: $2O^{2-} \rightarrow O_2 + 4e^-$

Background information:

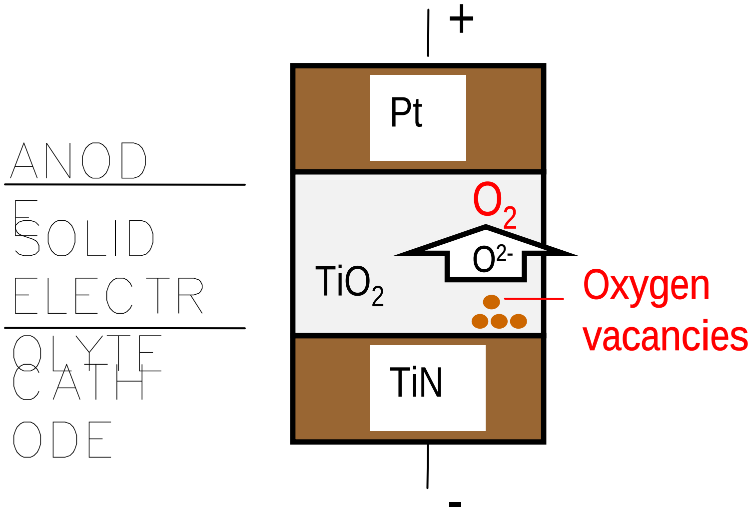
- Ti, a transition metal, exists as TiO_2, Ti_4O_7, Ti_5O_9, Ti_2O_3, TiO. Multiple oxidation states → +2, +3, +4, etc
- Transition metal oxides good ionic conductors. Used in fuel cells for that reason.

Two key phenomena → next few slides give evidence:

- Oxygen formed at the anode
- Conductive filament with oxygen vacancies from cathode

Ref: [1] G. Dearnaley, et al., 1970 *Rep. Prog. Phys.* [2] S. Muraoka, et al., IEDM 2007, [3] J. Yang, et al., Nature Nanotechnology, 2008.

Evidence for oxygen at anode

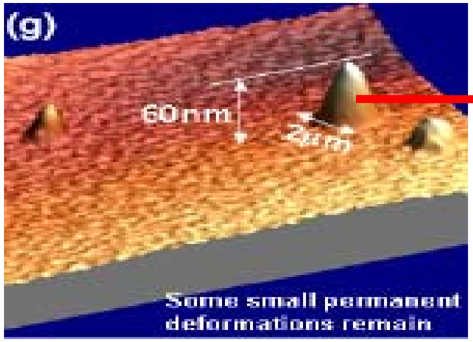


DURING FORM

On applying forming voltage,

@Cathode: $TiO_2 + 2xe^- \rightarrow TiO_{2-x} + xO^{2-}$

@Anode: $2O^{2-} \rightarrow O_2 + 4e^-$

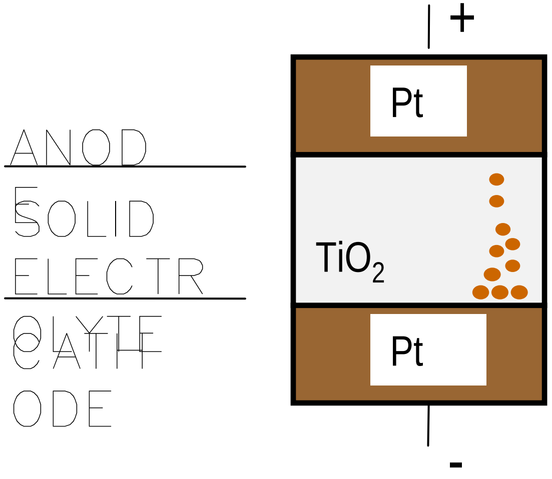


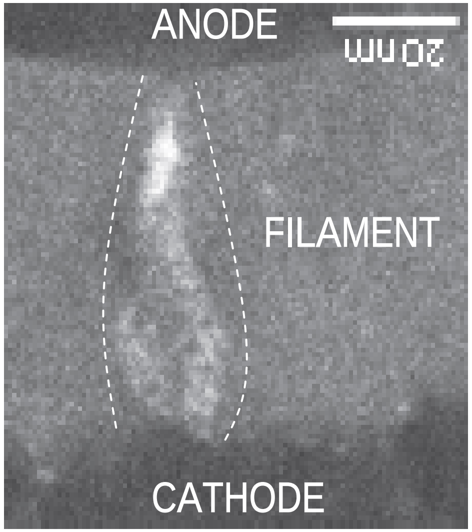
AFM image detecting oxygen bubbles for big devices

Click to view

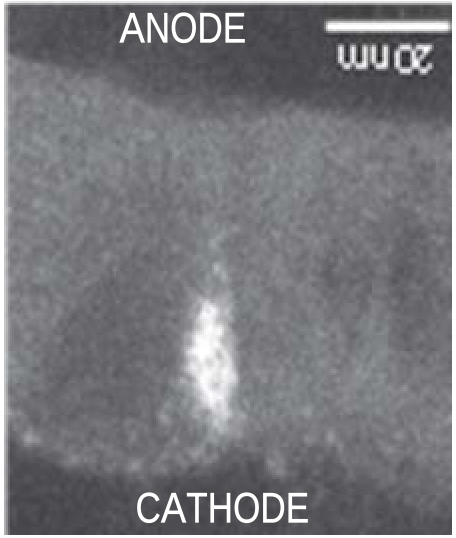
Ref: J. Yang, et al., Nature Nanotechnology, 2008.

Evidence for conducting filament of oxygen vacancies (1/2)





Fully-formed filament



Partially-formed filament

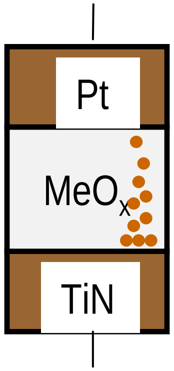
- Filament observed in TEM after forming
- Starts at cathode, many filaments present, most are partial filaments. Filament wider on cathode side.
- Electron diffraction studies + other experiments reveal filaments are Magneli phase compounds (Ti_4O_7 or Ti_5O_9, essentially TiO_{2-x}). These Magneli phase compounds conductive at room temperatures.

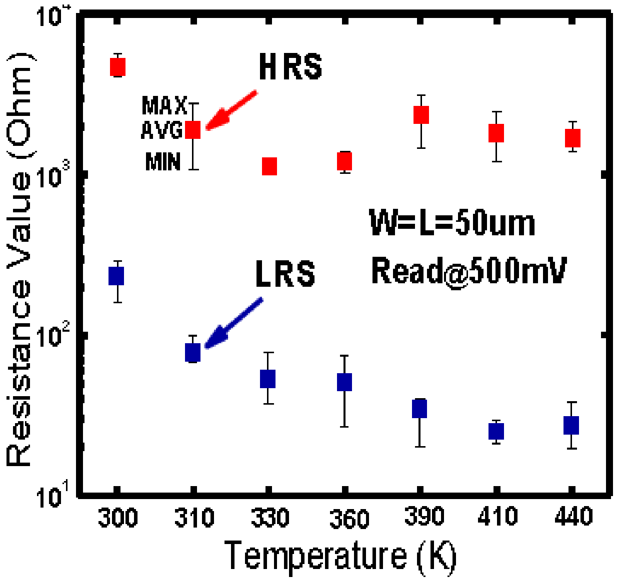
Ref: D-H. Kwon, et al., Nature Nanotechnology, 2010.

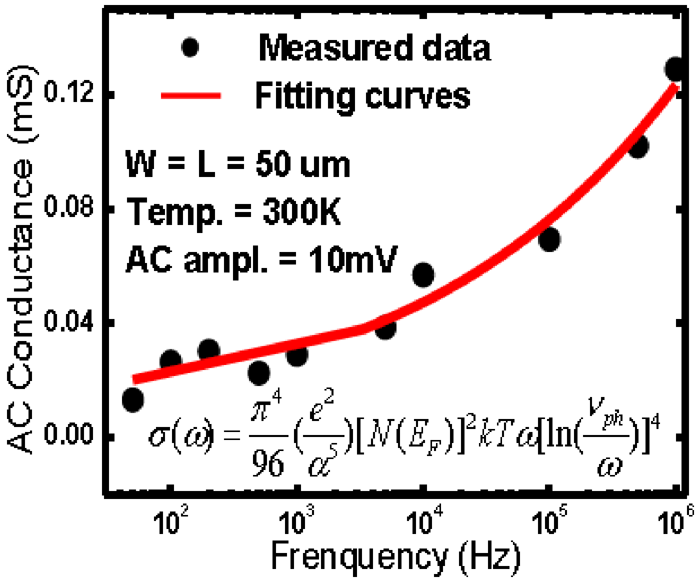
Evidence for conducting filament of oxygen vacancies (2/2)

Why should a filament of oxygen vacancies conduct?

A: Conduction by electron hopping from one oxygen vacancy to another.





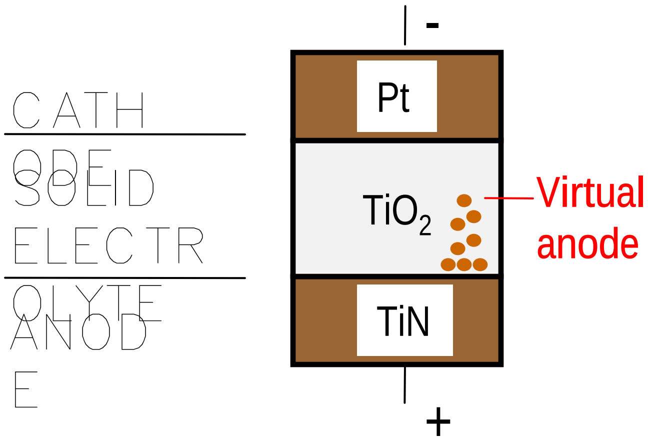


Curves fit Mott’s electron hopping theory

Ref: N. Xu, et al., Symp. on VLSI Technology, 2008.

Understanding RESET

Phenomenon 1: Filament breaks close to Top Electrode - MeO_x interface



Bipolar mode:

@Virtual Anode: $TiO_{2-x} + xO^{2-} \rightarrow TiO_2 + 2xe^-$

Heat-assisted electrochemical reaction, since 25uA reset current thro' 3nm filament → Current density of 3×10^8 A/cm^2… High temperatures!!!!

Unipolar mode:

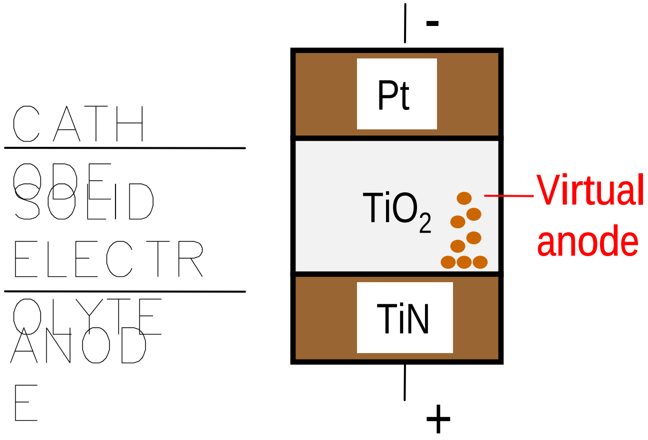
Solely heat driven

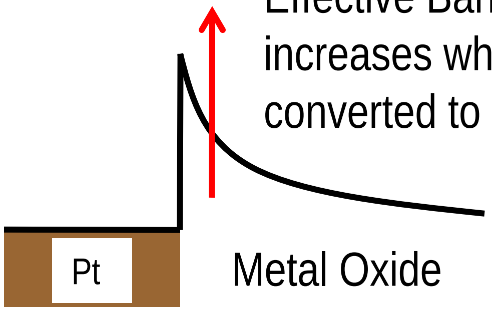
Ref: [1] S. Muraoka, et al., IEDM 2007, [2] J. Yang, et al., Nature Nanotechnology, 2008.

Understanding RESET

Phenomenon 2:

Filament breaks → Schottky barrier height at interface changes → Big change in resistance





Effective Barrier height increases when TiO_{2-x} converted to TiO_2

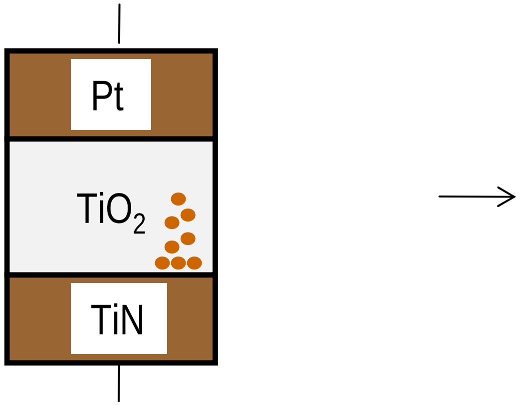
Oxygen vacancies @ interface reduce effective barrier height.

Similar theory to Fermi level pinning in CMOS high k/metal gate.

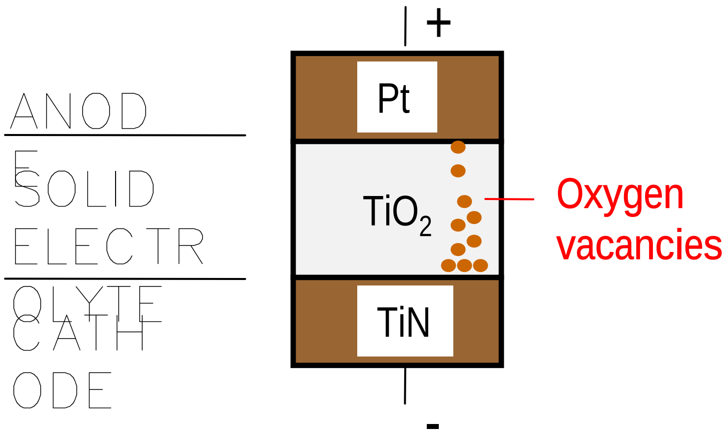
Ref: [1] S. Muraoka, et al., IEDM 2007, [2] J. Yang, et al., Nature Nanotechnology, 2008, [3] J. Robertson, et al., APL 2007.

Understanding SET

SET similar to FORM, but filament length to be bridged shorter → Lower voltages



Cell before SET



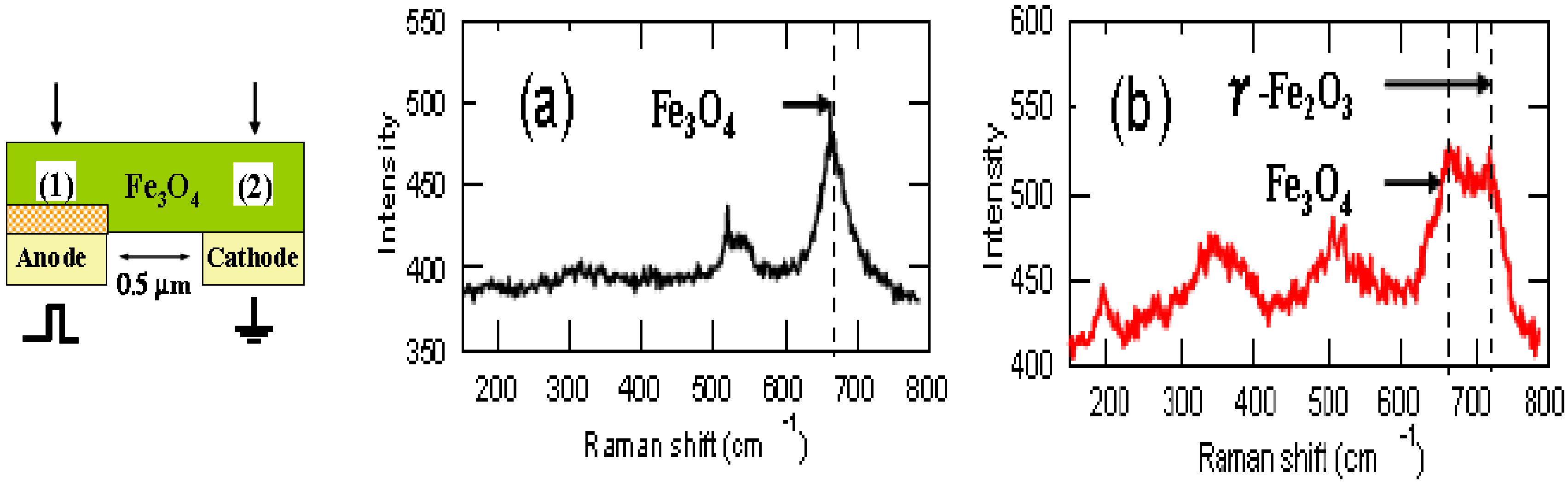
On applying set voltage,

@Cathode: $TiO_2 + 2xe^- \rightarrow TiO_{2-x} + xO^{2-}$

@Anode: $2O^{2-} \rightarrow O_2 + 4e^-$

Ref: [1] S. Muraoka, et al., IEDM 2007, [2] J. Yang, et al., Nature Nanotechnology, 2008.

Evidence for oxidation state change during switching



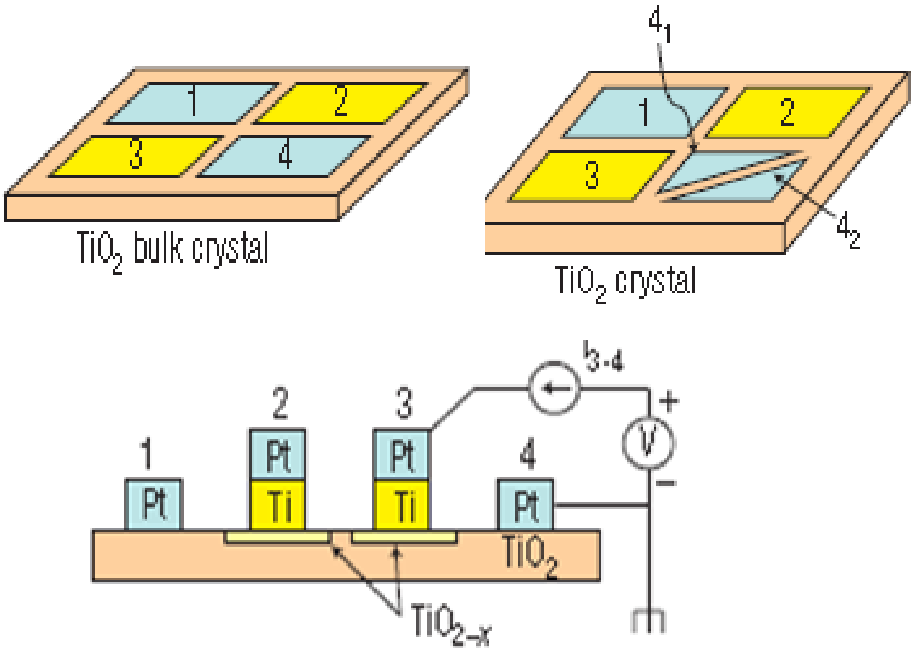
(a) Raman spectrum at (1) before switching and (2) before and after switching

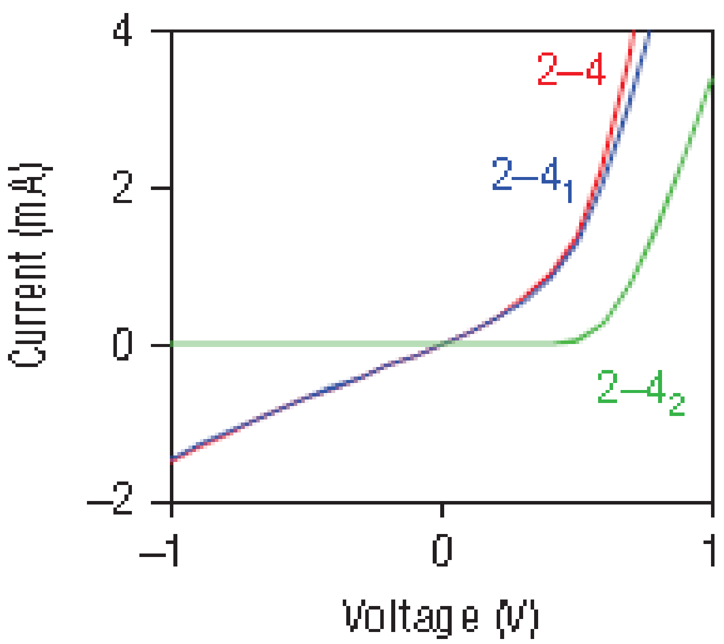
(b) Raman spectrum at (1) after switching

→ Switching occurs at interface (1) and involves oxidation state change

Ref: S. Muraoka, et al., IEDM 2007.

Evidence for switching at Top Electrode/MeO$_x$ interface





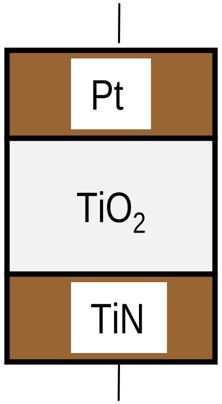
- SET voltage between pad 2 and pad 4 (denoted 2-4).
- Then, pad 4 broken into two. One broken part (denoted 2-4$_1$) had nearly the same I-V curve as previously! The other (denoted 2-4$_2$) OFF, almost ideal rectifier

→ Filamentary conduction, and interface between Pt/TiO$_2$ switching.

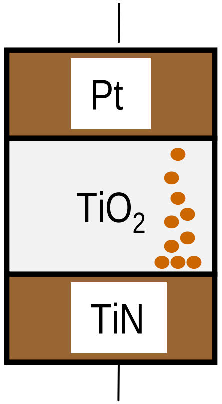
Ref: J. Yang, et al., Nature Nanotechnology, 2008.

To summarize today’s understanding of RRAM,

Before FORM

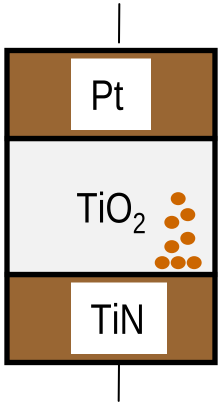


After FORM



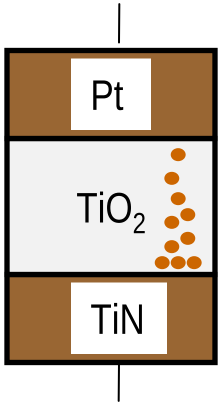
$TiO_2 + 2xe^- \rightarrow TiO_{2-x} + xO^{2-}$

After RESET



$TiO_{2-x} + xO^{2-}$
$\rightarrow TiO_2 + 2xe^-$

After SET



$TiO_2 + 2xe^-$
$\rightarrow TiO_{2-x} + xO^{2-}$

Filamentary switching with oxygen vacancies.

Barrier height at Top electrode/MeO_x interface plays a key role in ON/OFF I-V curves.

Outline

- Switching Optimization

Techniques to optimize RRAM switching

- Optimized Top Electrode
- Optimized Transition Metal Oxide
- Control of Cell Current during SET

Techniques to optimize RRAM switching

- Optimized Top Electrode

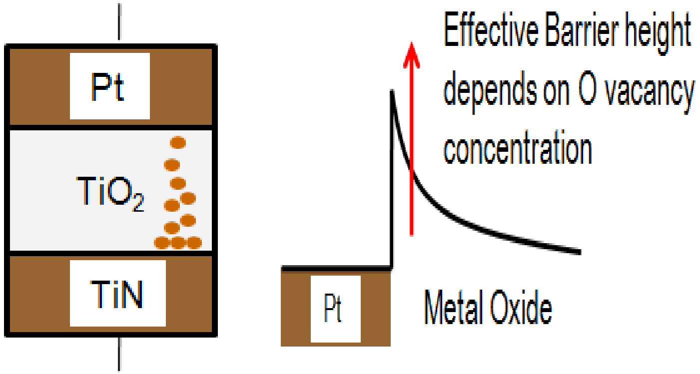
Based on switching model, RRAM's top electrode needs

Fab-friendly material

Excellent oxidation resistance → even for high T and oxygen rich ambients

SET: $TiO_2 + 2xe^- \rightarrow TiO_{2-x} + xO^{2-}$

RESET: $TiO_{2-x} + xO^{2-} \rightarrow TiO_2 + 2xe^-$

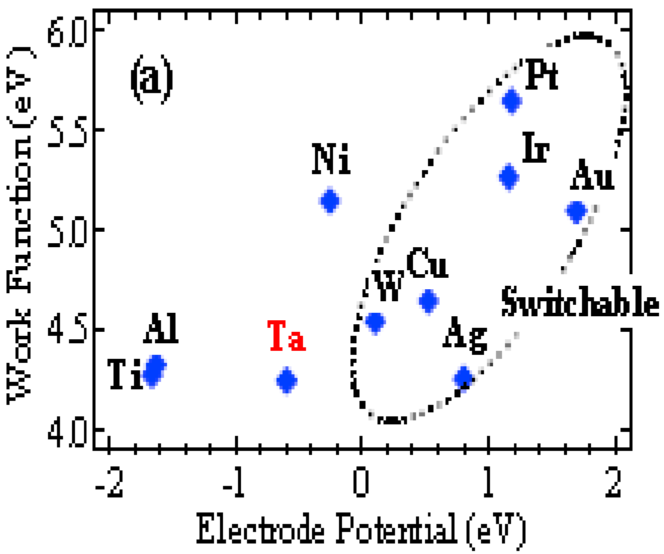


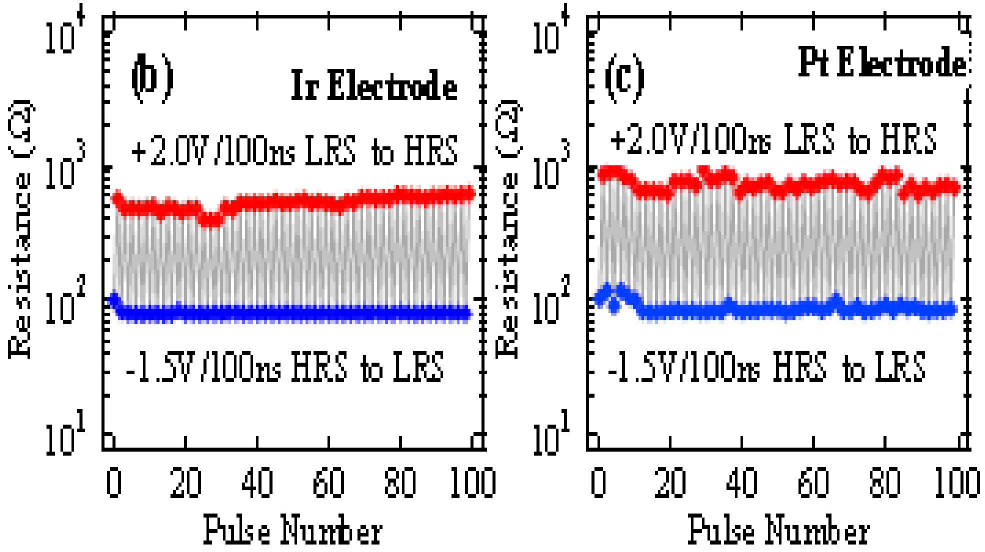
High work function → High Schottky barrier height → Lower current levels

Pt → excellent oxidation resistance, high work function → used in RRAMs. But not fab-friendly ☹

Ref: Z. Wei, et al., IEDM 2008

Top electrode candidates for RRAM





By definition, higher electrode potential

→ More difficult to oxidize

Best switching seen when both electrode potential

and work function are high

pMOS gate in high k/metal gate logic transistors → high work function, good oxidation resistance

→ Can use those electrodes (eg. TiAlN) for RRAM as well.

Ref: [1] Z. Wei, et al., IEDM'08 [2] D. Sekar, et al., US Patent Applications 20100117069/20100117053 , filed Feb.'09, published by USPTO '10

Techniques to optimize RRAM switching

- Optimized Transition Metal Oxide

Based on switching model, RRAM's Metal Oxide Material needs

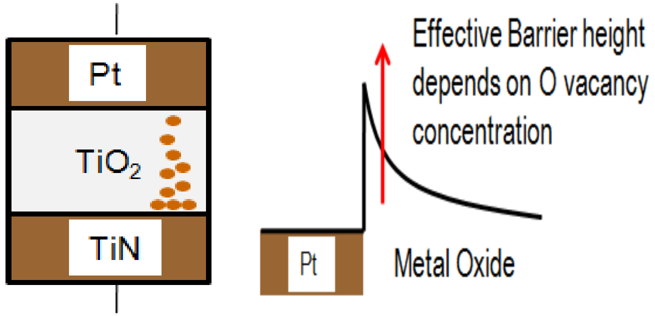
High ionic conductivity → helps ions move at lower fields and temperature

Multiple stable oxidation states, low energy needed for conversion

Simple fab-friendly material (Key)

SET: $TiO_2 + 2xe^- \rightarrow TiO_{2-x} + xO^{2-}$

RESET: $TiO_{2-x} + xO^{2-} \rightarrow TiO_2 + 2xe^-$



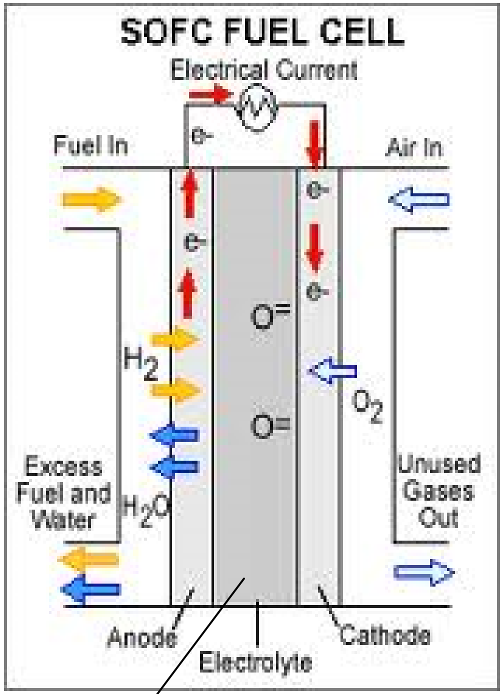
Low electron affinity → High Schottky barrier height → Lower current levels. Can possibly avoid use of Pt.

Work reliably at high temperatures encountered during RRAM operation

Multiple materials fit these criteria, and many drop off our candidate list due to these too…

Ref: D. Sekar, et al., US Patent Applications 20100117069/20100117053 , filed Feb.'09, published by USPTO '10.

Stabilized Zirconium Oxide: a good candidate for RRAM



Electrolyte typically Zirconium Oxide with Y doping

RRAM need	Stabilized ZrO_x properties	Comment
High Ionic conductivity	40S/cm @ 800ºC	One of the highest known, Fluorite structure
Multiple stable oxidation states	Stable +2, +3, +4 oxidation states	
Fab-friendliness	Well-known material	Due to high k work
Low electron affinity	Low, ~2.4eV	TiO_x and TaO_x RRAM have 3.9eV and 3.3eV
Withstand high T reliably	Yes	Fuel cells operate at 800ºC for long times, reliable

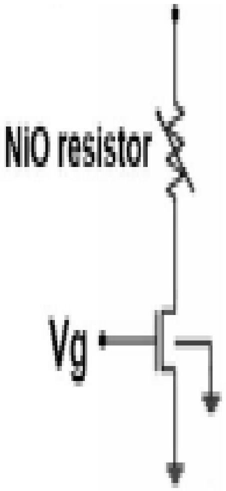
Hafnium oxide similar to Zirconium Oxide, has many of these advantages. Also used for fuel cells.

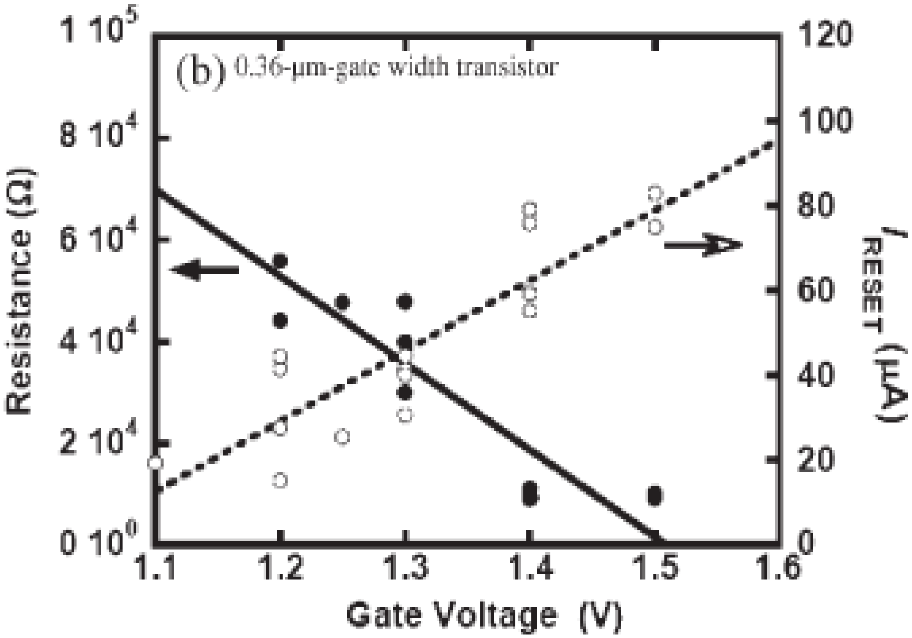
Ref: D. Sekar, et al., US Patent Applications 20100117069/20100117053 , filed Feb.'09, published by USPTO '10.

Techniques to optimize RRAM switching

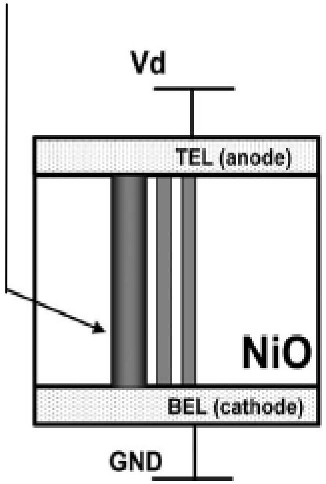
- Control of Cell Current during SET

RESET Current determined by SET Current Compliance





Filament size determined by SET current compliance



- Fatter filament if higher SET current → Harder to break → Higher RESET current
- Careful transient current control for SET important, for both RRAM device development and array architecture. Keep parasitic capacitances in your test setup in mind while measuring!!!!!

Ref: [1] Y. Sato, et al., TED 2008, [2] F. Nardi, et al, IMW 2010.

Outline

- Array Architectures and Commercial Potential

RRAM Device Specs from the Literature

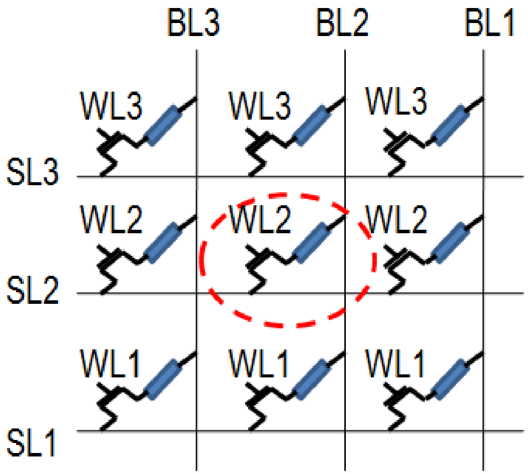
	ITRI, IEDM 2008	NEC, VLSI 2010	Panasonic, IEDM 2008	Univ. + IMEC, IMW 2010	Fujitsu, IEDM 2007
Device	TiN/Ti/HfO_x/TiN	Ru/TiO_x/TaO_x/Ru	Pt/TaO_x/Pt	Au/NiO_x/TiN	Pt/Ti-doped NiO/Pt
Test chip	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R
Polarity	Bipolar	Unipolar	Bipolar	Unipolar	Unipolar
Reset	2V, 25uA	0.65V, 200uA	1.5V, 100uA	0.5V DC, 9.5uA	1.9V, 100uA
Set	2.3V	2.8V	2V	2.7V DC	2.8V
Form Voltage	3V	?	?	3.7V DC	3V
Switching Time	<10ns	<1us	<100ns	NA	10ns
On/off ratio	~100x	100x	10x	5x-10x	90x
Endurance, Data Retention	10^6, 10 years	10^5, 10 years	10^9, 10 years	130 cycles, ?	100, 10 years
Comments	Typical data	Worst case data	Typical data	Typical data	Typical

For these device specs, what kind of selectors and array architectures work well?

Potential Array Architectures

- 1T-1R
- 3D Stacked 1D-1R
- 3D Stacked 1T-manyR
- 3D Stacked 1T-1R

1T-1R Array Architecture



1T-1R viable for embedded NVM, code storage if forming-free
USPs: Easily embeddable device, low switching energy

- Easy to embed into a logic process

  → ~3 extra masks vs. ~8 extra masks for flash

  → Lower voltages vs. flash

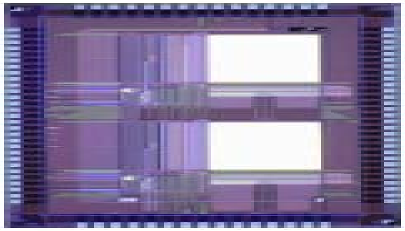
Key issues:

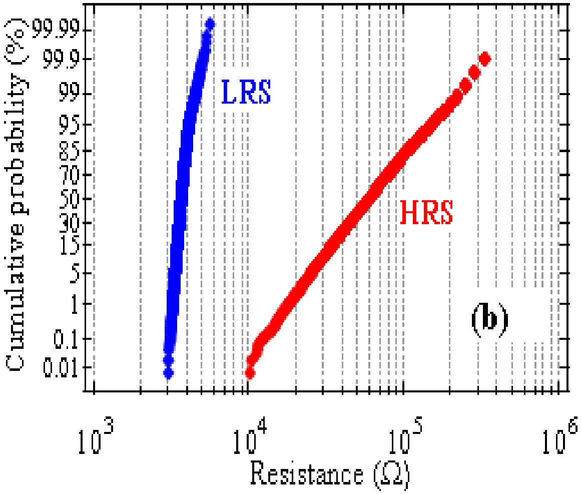
- Need forming-free operation:

  For 3V forming, standard MOSFET probably cannot scale below 130nm L_{eff}.

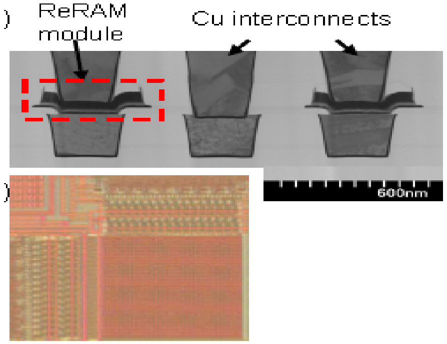
- If forming-free and SET/RESET voltage < 1-1.5V, density = $6F^2 – 8F^2$. Then, good for embedded NVM and code storage applications.

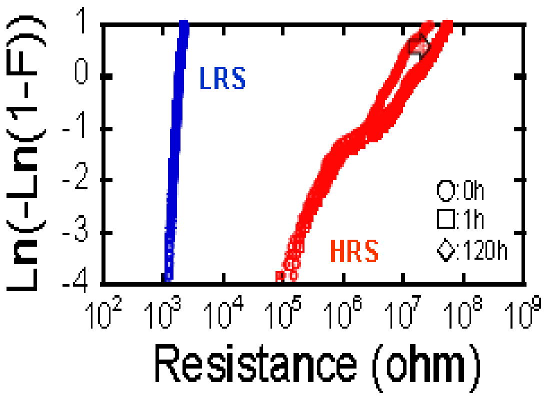
Array Demonstrations of 1T-1R RRAM



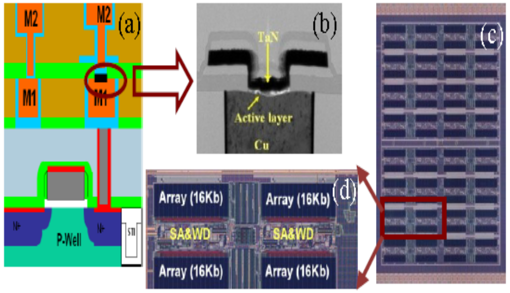


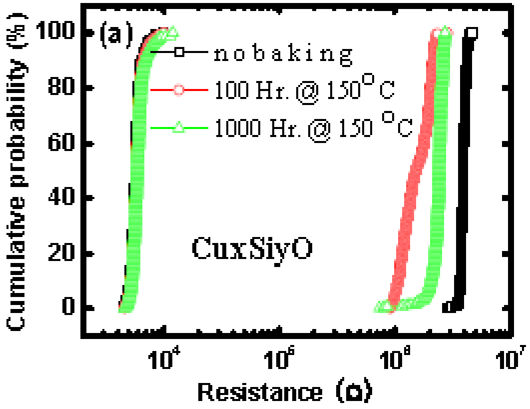
Pt/TaO$_x$/Pt
8kb bipolar array
Panasonic, IEDM 2008





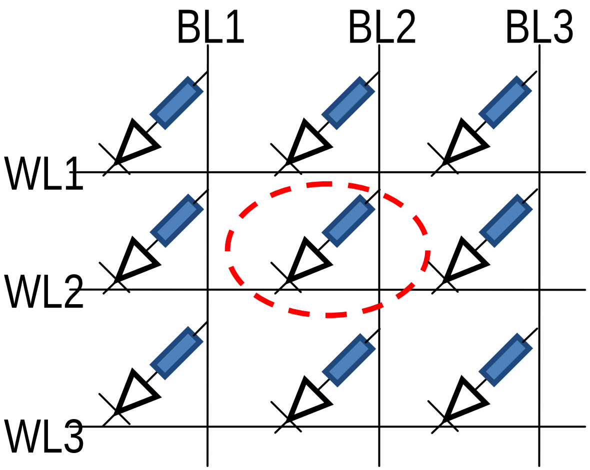
Ru/TiO$_x$/TaO$_x$/Ru
1kb unipolar array
NEC, VLSI 2010





TaN/CuSi$_x$O$_y$/Cu
1Mb bipolar array
SMIC, VLSI 2010

3D Stacked 1D-1R Architectures



- pn diodes → unipolar, or

  Punch-Through Diode, Ovonic Threshold Switch (OTS), others → bipolar
- 6 levels of memory → $4F^2/6 = 0.66F^2$. Very dense!!!

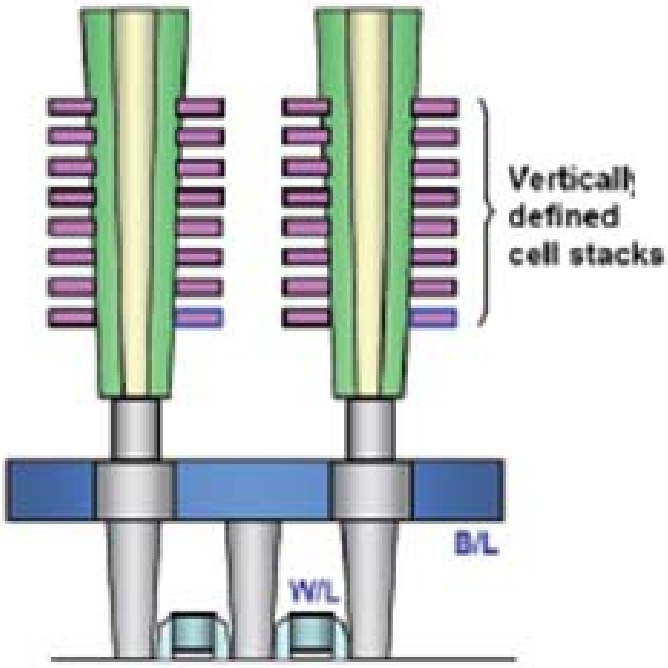
<u>Key issues:</u>

- 6 layers → 12 critical masks if 2 masks per layer. Cost competitive with NAND flash (4 critical masks)?
- Compete with NAND performance and power? 3D diode selectors not as good as transistor selectors.

USP: Dense. Targets data and code storage markets.

Ref: [1] E. Harari, SanDisk Investor Day, Aug. 2008 [2] D. Kau, et al., IEDM 2009 [3] A. Mihnea, D. Sekar, et al., US Patent Appln. 12/582,509 [4] W. Parkison, US Patent Appln. 20090207645 [5] S. Lai, IEDM 2008

3D Stacked 1T-manyR Architecture



USP: Dense + Low number of litho steps. Targets code and data storage markets.

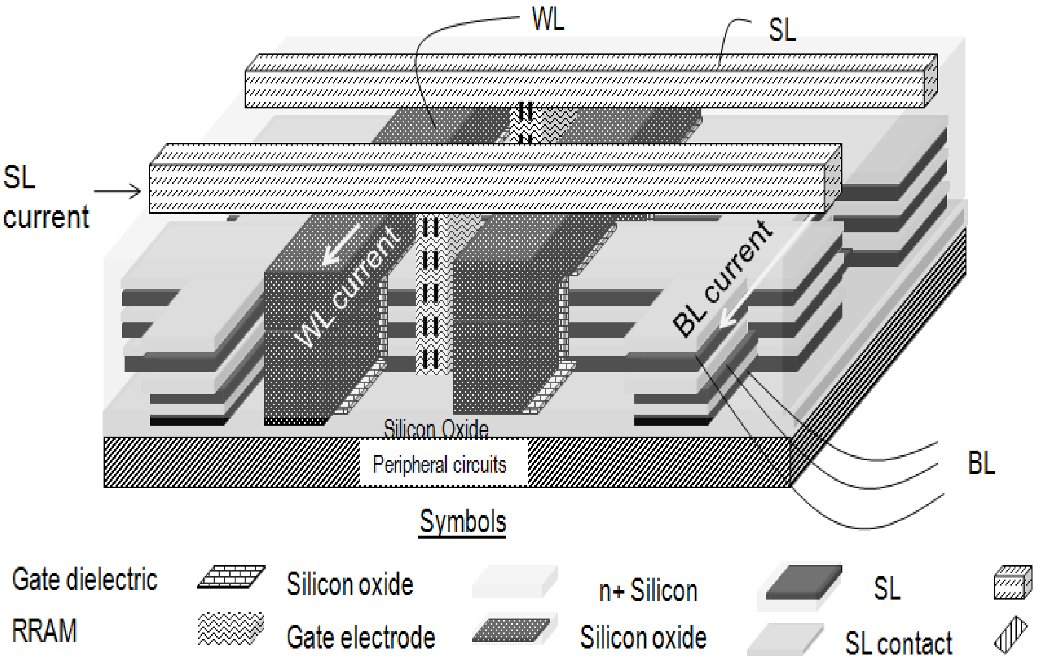
- Advantages of transistor selectors, but higher density than 1T-1R → More suited for storage.
- Low number of lithography steps

<u>Key Issues:</u>

- Sneak leakage. Reach high array efficiency and NAND-like cost per bit?
- Performance and power consumption competitive with NAND flash?

Ref: H. S. Yoon, et al., VLSI 2009.

3D Stacked 1T-1R Architecture



USP: Dense + Low number of litho steps + Excellent selector. Targets code and data storage markets.

- c-Si Junction-Less Transistor selector with ion-cut (JLT ok for this appln).
- No sneak leakage, so excellent performance/power.
- Shared litho steps

<u>Key Issues:</u>

- Ion-cut cost might need some optimization to get to $60 per layer

Market Opportunities

Data Storage

Market (2010): $22B
Applications: Cell-phones, tablets, computers
USP vs. incumbent: Endurance, Performance

3D Stacked 1T-1R, 3D Stacked 1D-1R, 3D Stacked 1T-manyR

Code Storage

Market (2010): $5.5B
Applications: Computers, Cell-phones
USP vs. incumbent: Density, Scalability

3D Stacked 1D-1R, 1T-1R,
3D Stacked 1T-manyR, 3D Stacked 1T-1R

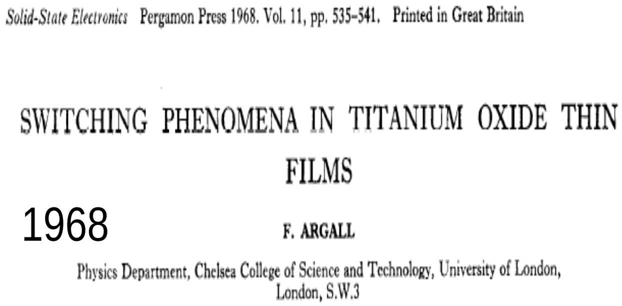
Embedded NVM

Market (2010): $4.5B
Applications: Microcontrollers, FPGAs, others
USP vs. incumbent: Easy to embed

1T-1R

Intellectual Property

1960s: Switching observed



Solid-State Electronics Pergamon Press 1968. Vol. 11, pp. 535–541. Printed in Great Britain

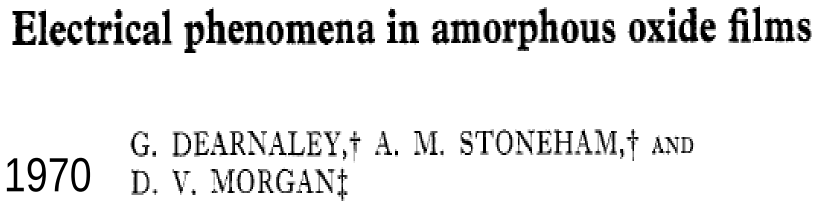
SWITCHING PHENOMENA IN TITANIUM OXIDE THIN FILMS

1968

F. ARGALL

Physics Department, Chelsea College of Science and Technology, University of London,
London, S.W.3

Late 1960s-early 1970s: Forming, filamentary model, switching summary of 10 different transition MeO_x where Me is Ti, Ta, Zr, V, Ni, etc



Electrical phenomena in amorphous oxide films

1970

G. DEARNALEY,† A. M. STONEHAM,† AND
D. V. MORGAN‡

- Patents, if any, on *basic switching concepts,* have expired ☺.
- Good patents on more advanced concepts exist (eg) Pt-replacement approaches, array architectures, doping, etc. Can engineer around many of these.
- IP scenario for RRAM a key advantage. Other resistive memories have gate-keepers (eg) Basic patents on PCM, CB-RAM, STT-MRAM from Ovonyx, Axon Technologies, Grandis.

Outline

- Risks and Challenges

Risks and Challenges

Business risk:

Competing with *high-volume* flash memory technologies.

Technology risks:

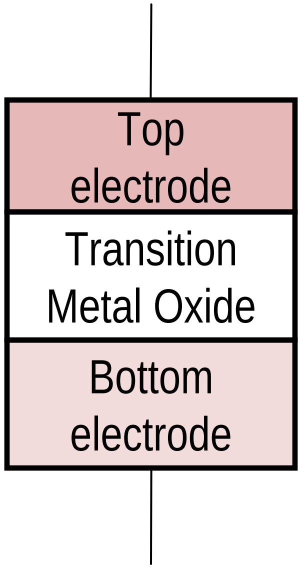
- RESET current scaling a function of current compliance, not device area.

  How low can it go with acceptable retention?
- Array architecture
- Forming

Outline

- Conclusions

Conclusions



Top electrode

Transition Metal Oxide

Bottom electrode

- Simple materials. Excellent switching + good retention possible.
- Mechanism: Oxygen vacancy filaments
- Many techniques to optimize switching such as materials engg. of top electrode and RRAM, transient current control
- Markets:

  - Data storage ($22B) → 3D stacked 1T-1R, 1D-1R and 1T-manyR

  - Code storage ($5.5B) → 3D stacked architectures, 1T-1R

  - Embedded NVM ($4.5B) → 1T-1R attractive if no forming

My take:
Exciting and interesting technology. But will RRAM change the world? Too early to say…

PS:

What’s all this “Memristor” stuff the press is going gaga about?

Analogy: The RRAM as a Memristor

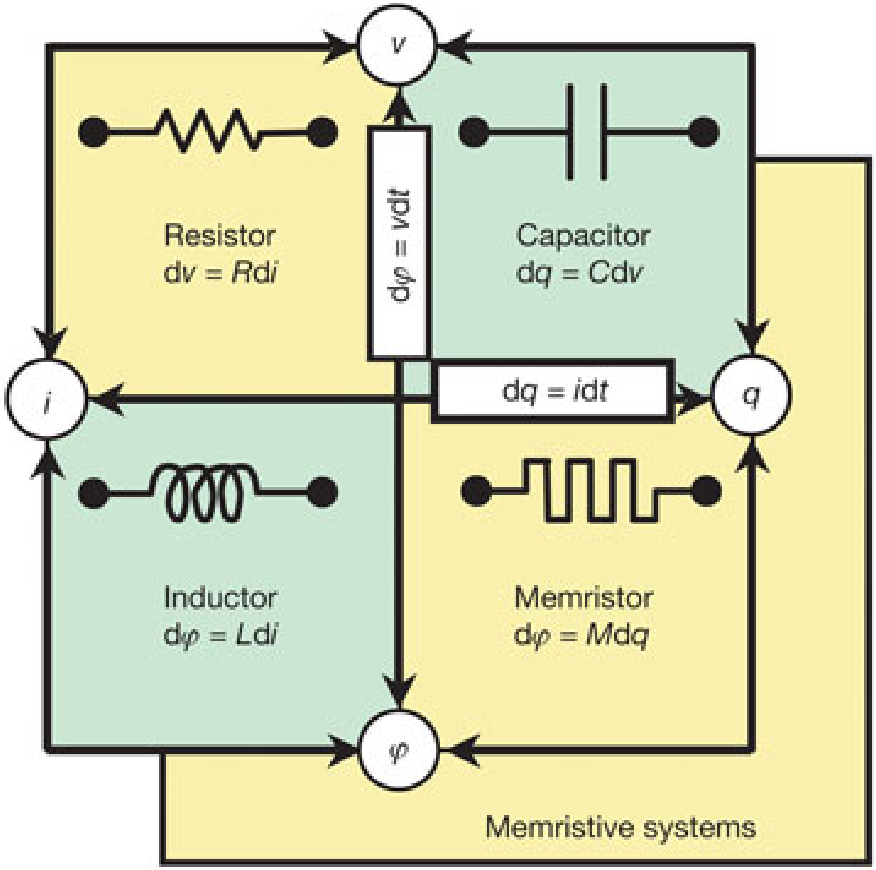
- $V(t) = M(q(t))\, I(t)$

↓

Resistance value of RRAM = function of charge that has flown through it

- $M(q(t)) = \dfrac{V(t)}{I(t)}$

$$= \frac{d(\text{Flux})/dt}{dq/dt} = \frac{d(\text{Flux})}{dq}$$

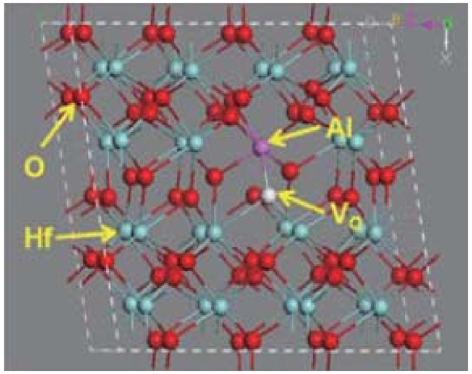


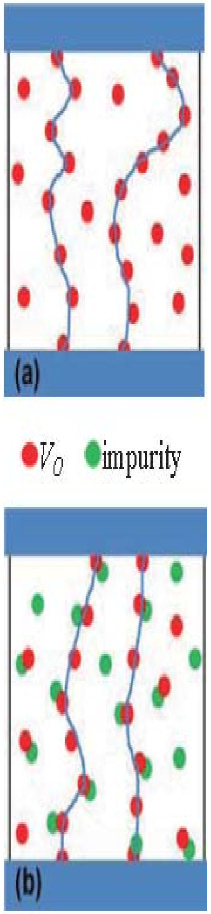
Ref: J. Yang, et al., Nature Nanotechnology, 2008.

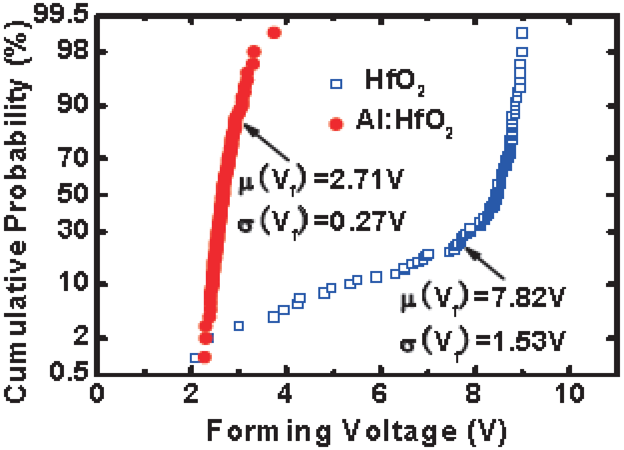
Thank you for your attention!

Backup Slides

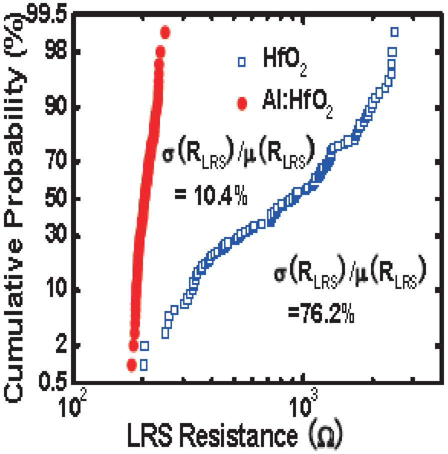
Doping elements with +3 oxidation state into metal oxides with +4 oxidation state

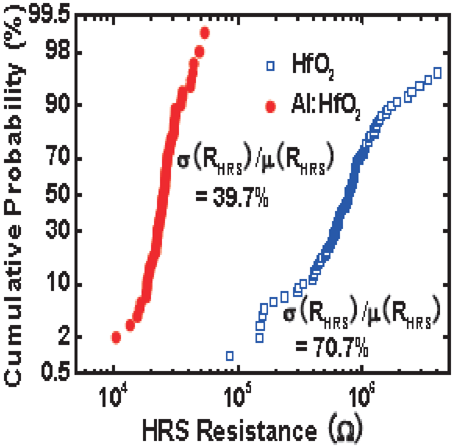






- Al in HfO_2 → Al replaces Hf in lattice, oxygen vacancies produced
- More oxygen vacancies → supposedly *uniform* conductive filaments



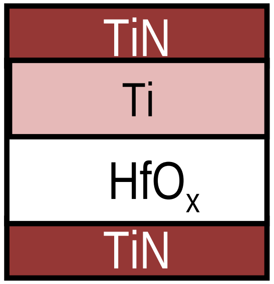


Ref: B. Gao, et al., Symp. on VLSI Technology, 2009.

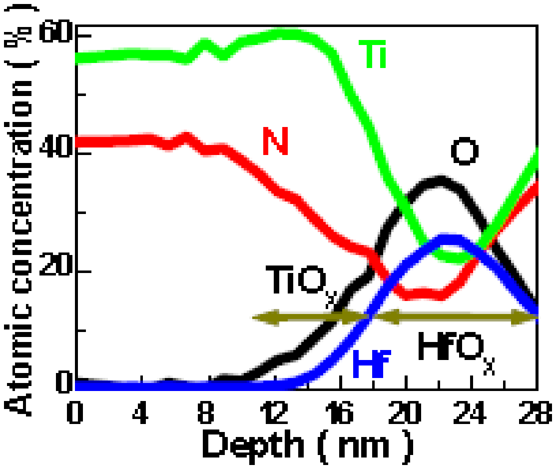
Impact of interface layers

- Ti interface layer in HfO_2 RRAM.
- Ti → getters oxygen → vacancies in HfO_2. Forms $TiN/TiO_x/HfO_{1.4}/TiN$ device.
- Vacancies → reduce forming voltage and improve switching yield.

Some of the best switching characteristics reported to date for RRAM.



As constructed



On XPS analysis

Parameter	Results
FORM	3V
SET/RESET voltages	<2V
RESET current	25uA possible
Switching time	10ns
Endurance	$>10^6$ cycles
Retention at 85°C	10 years

Ref: H. Y. Lee, et al., IEDM 2008