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CONFIDENTIAL

INVENTIVE

DfM: What, Why, When & How

Nickhil Jakatdar

Overview:

- What is DfM?
- Why DfM?
  - The realities below 130nm
  - Yield / Cost Analysis
  - Rules and Models
- When is it going to be needed?
  - Examples in CMP, Lithography, and CAA
- How is it going to be solved?
  - Novel approaches in design implementation
- Observations and Predictions

What is Design for Manufacturing (DfM)?

- Various definitions of DfM include
  - Anything and everything relating to a more mfg. aware design of a chip
  - RET/OPC
  - Lithography/CMP Process Checks
  - Critical Area Analysis
  - Statistical Static Timing Analysis (SSTA)
  - Manufacturing Aware Routers
  - Design for Marketing
  - Design for Money
  - Anything that allows a start-up to raise a round of funding

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Why Design must care about Manufacturing…

- Below 130nm, “What you draw is not what you get”
- The further you go below 130 nm, the less a rule-based approach is effective
- This leads to designs that behave very differently in reality vs. simulation ➔ little to no predictability

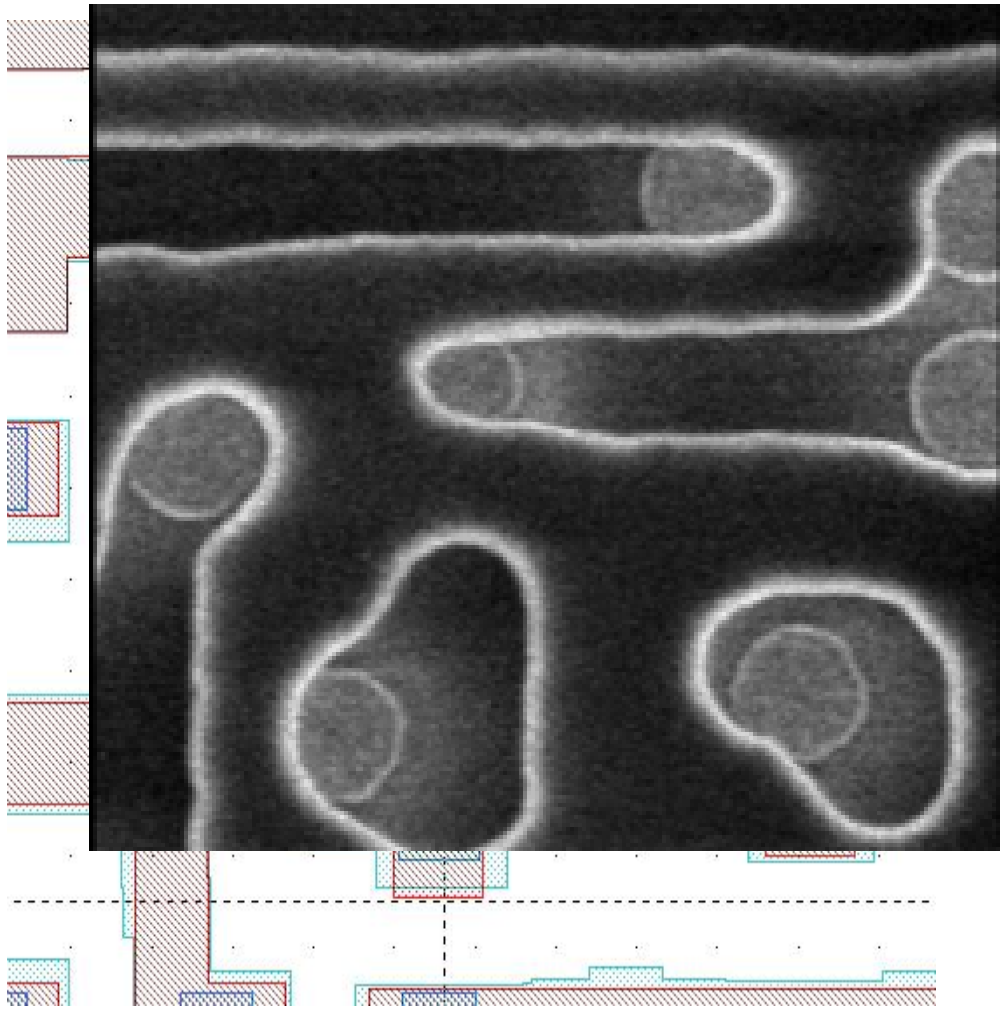

Illustration and photomicrograph courtesy of Texas Instruments.

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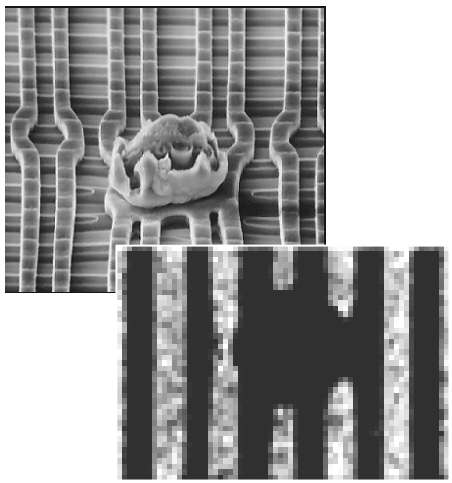
More and more Manufacturing Effects cannot be Modeled with Rules

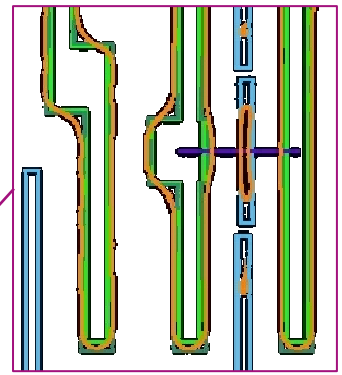
130nm

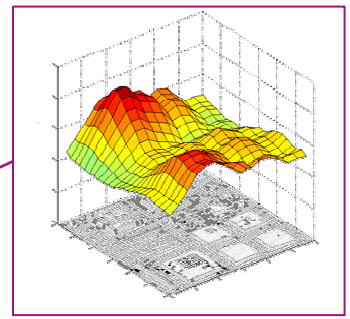
- Via Failure
- Particle Defects

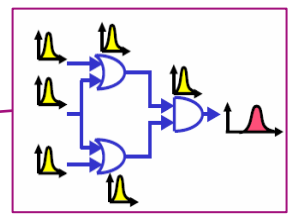


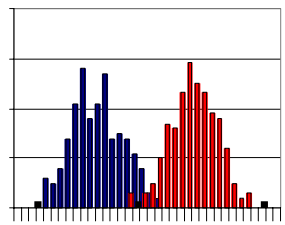
65nm/45nm

- Via Failure
- Particle Defects
- Litho Effects
- CMP Effects
- Timing, Power Variation









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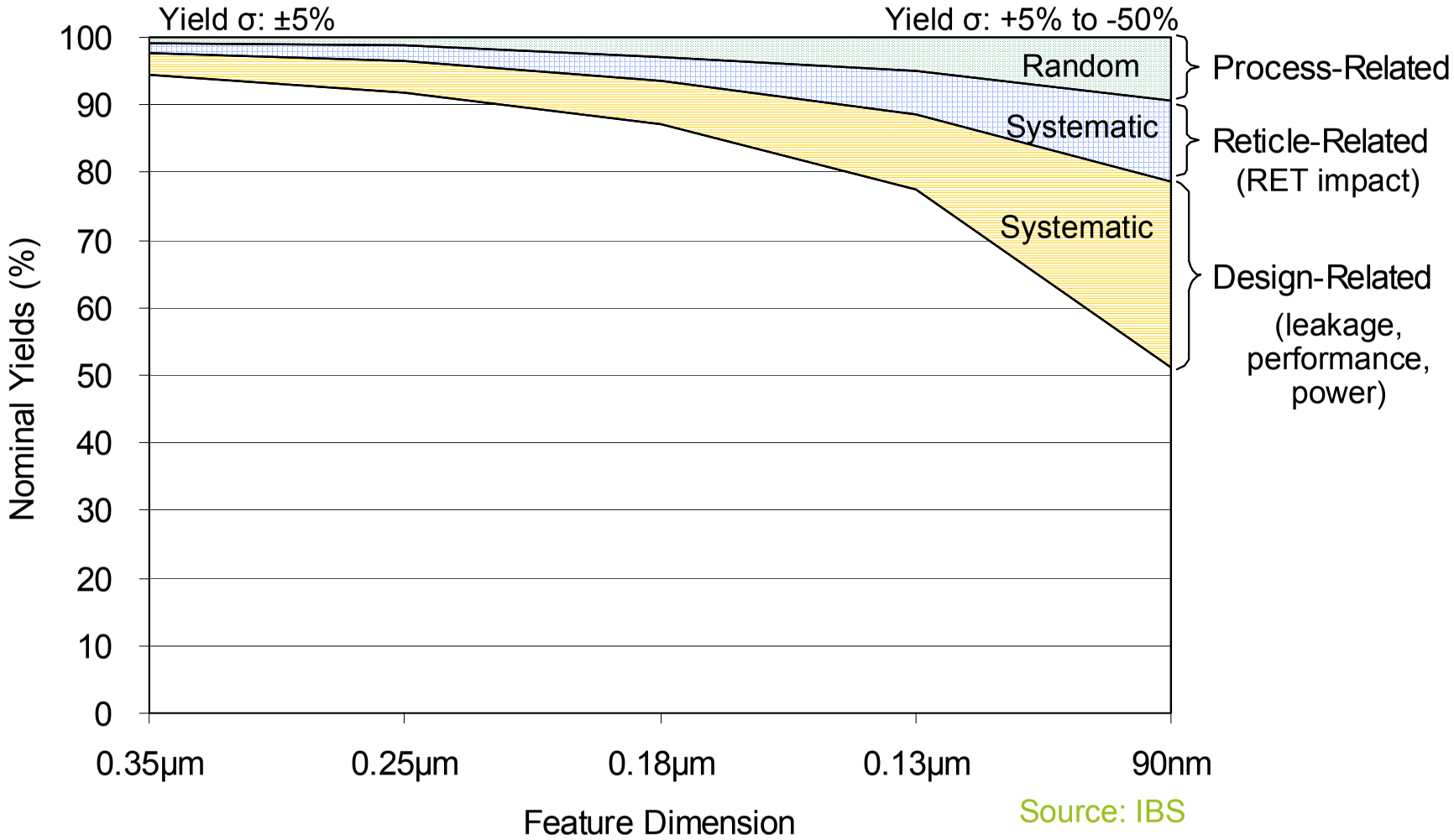
Impact of DfM on Yield

Increasing with each new process generation



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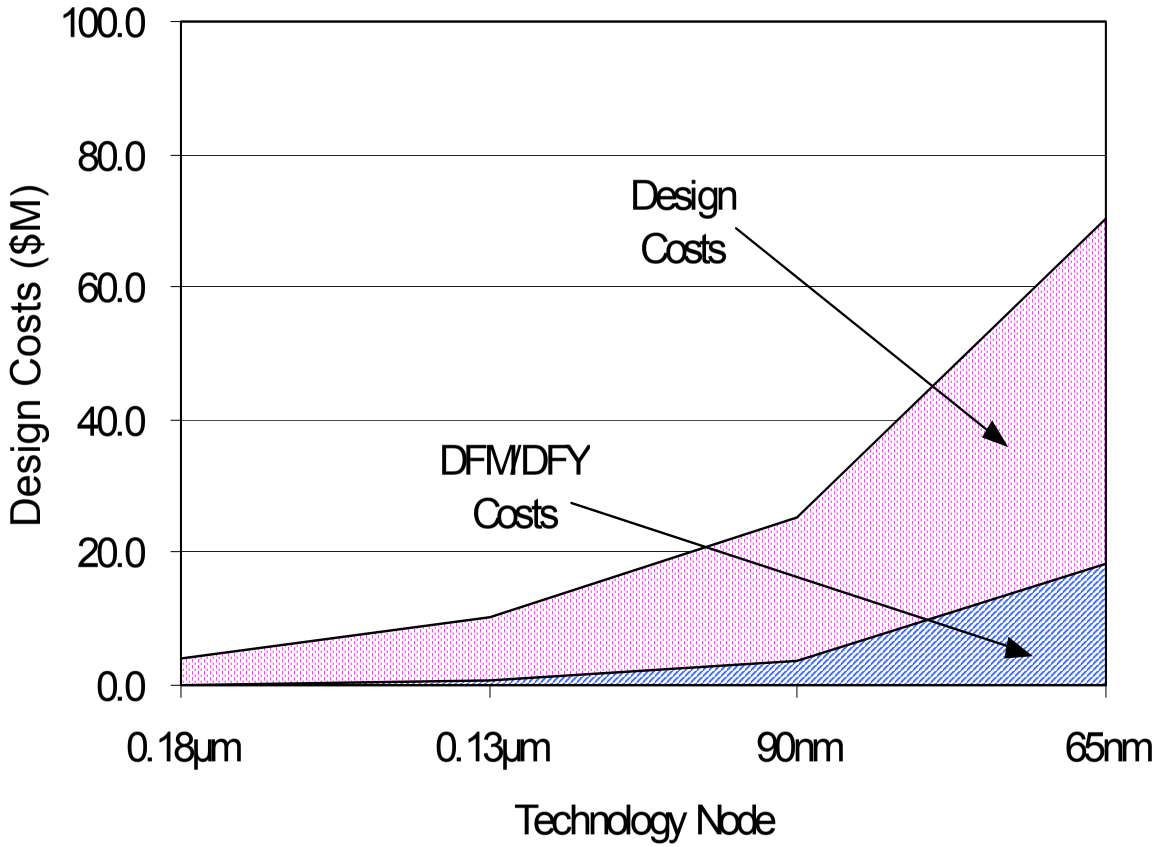
Impact of DfM on Design Costs



Observations:

- Design-specific yield related problems are growing
- Caused by interaction of design & materials/process
- Increasing cross-process interactions difficult to model with rules
- Most solutions lie beyond the domain of Traditional DFM (e.g. post design processing)

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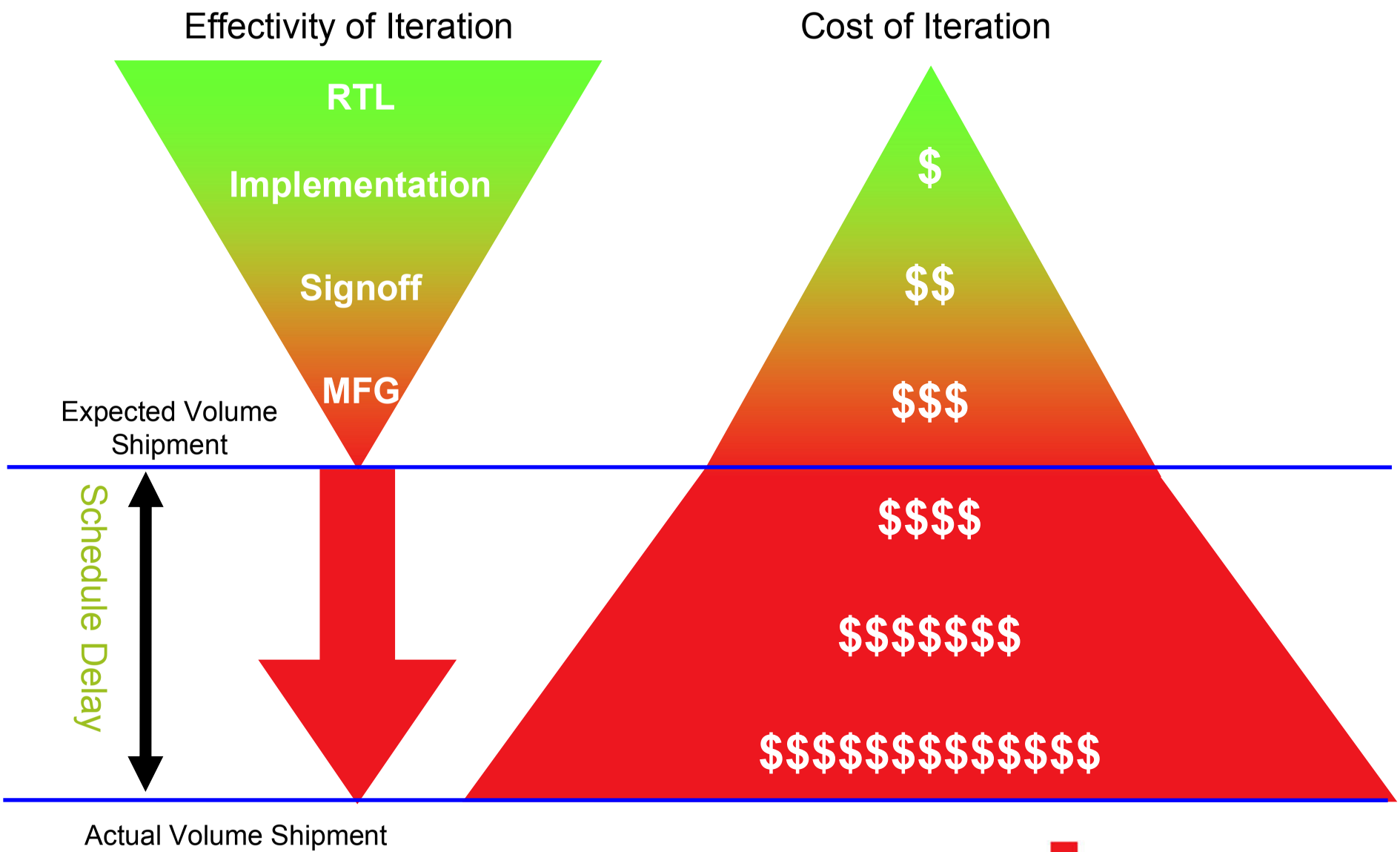
Impact of DfM on Time to Market



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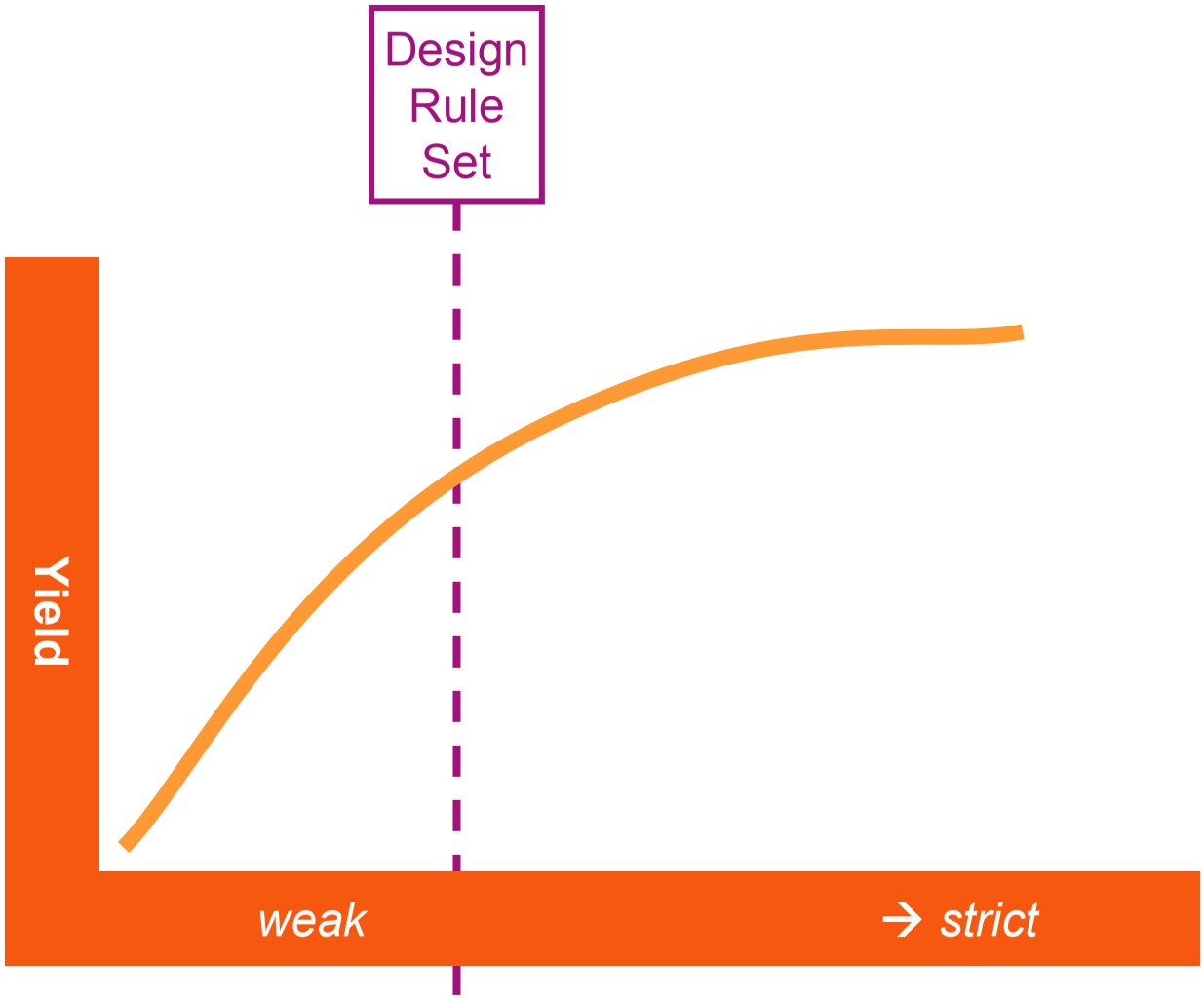
Traditional rule-based approach to minimize failures in design

- Add rules
  → Rule deck size and complexity are exploding
- Make rules more strict
  → Highly conservative rules prevent benefits of advanced processes
- Add margin
  → Compounding effect of margin + margin + margin
- Drawbacks
  - Sacrifice performance
  - Increase area +/or power
  - Lengthen design cycle
  - Miss unanticipated interactions between effects

Design rules are a tradeoff



Speed vs. effectiveness

- To make rules execute fast, keep them simple
- To make simple rules effective, be conservative and add margin

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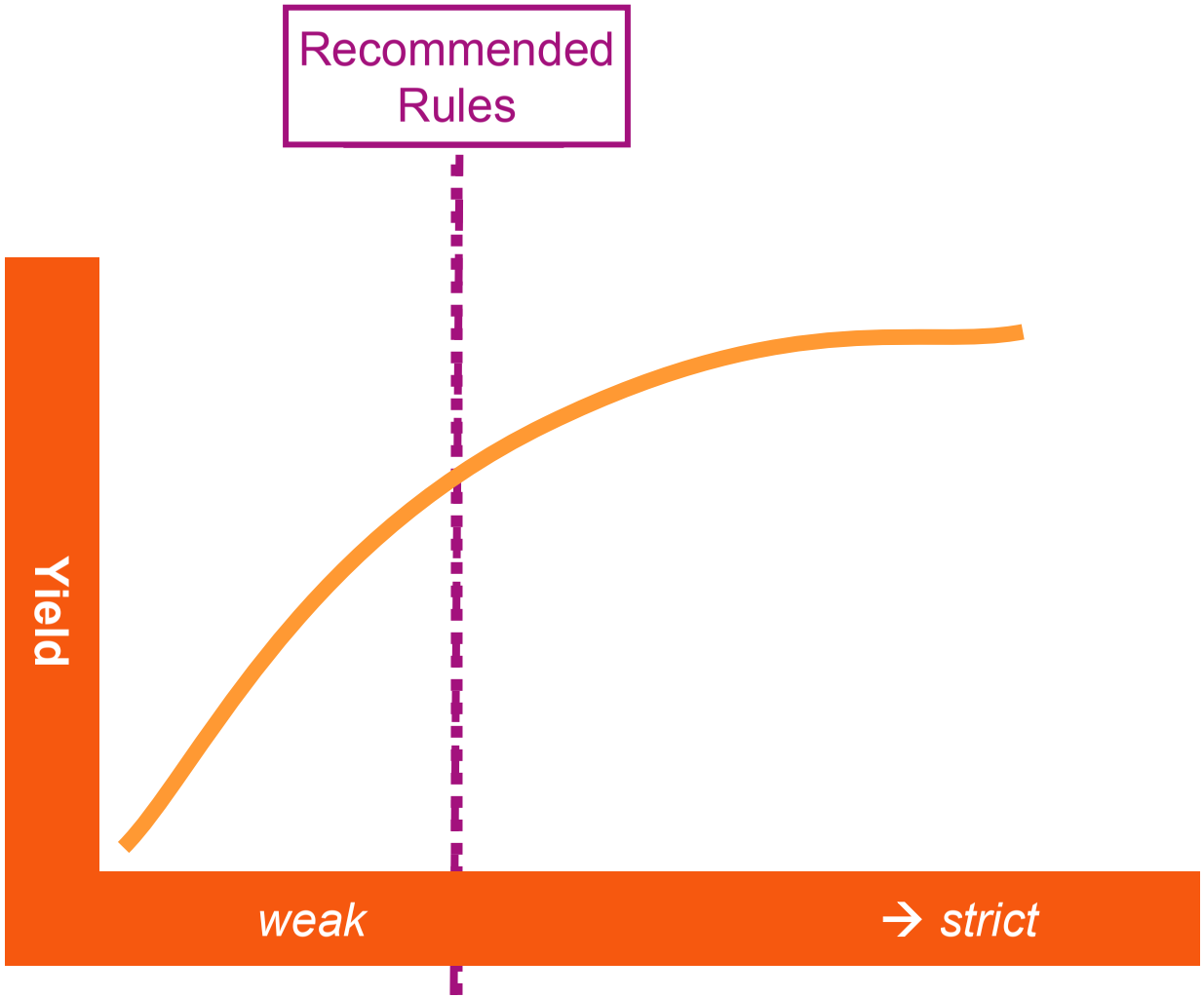
Current approach: recommended rules



Recommended rules are:

- More strict
- More complex
- More run time
- Optional

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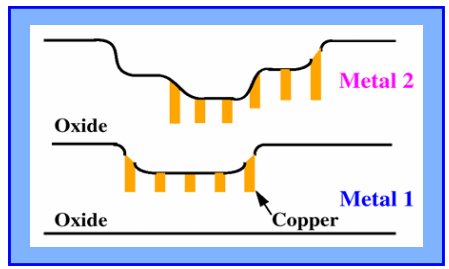
More Rules – Recommended Rules – Don't Solve the Problems

- Still have too many rules, too-strict rules, too much margin
- Rules don't handle interaction of effects – multivariate correlations
  - Litho stepper shallow depth of focus ↔ uneven chip surface from CMP
  - OPC on adjacent DRC-clean shapes produces artifacts (extra shapes)
  - Multiple DRC-clean layers stack up to allow soft spot for CMP erosion
- Rules always compromise between Type I and Type II errors
  - Type I: missed a true problem
  - Type II: highlight a false alarm
- Rules don't enable intelligent risk/benefit tradeoff



Bottom-Line: Required Rules vs. Recommended Rules Drive Designers Crazy!!

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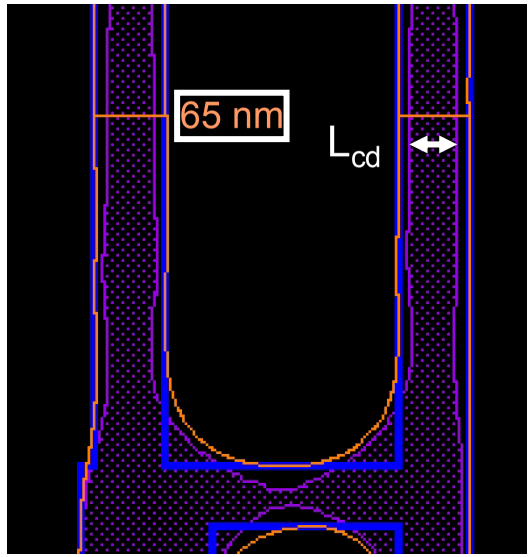
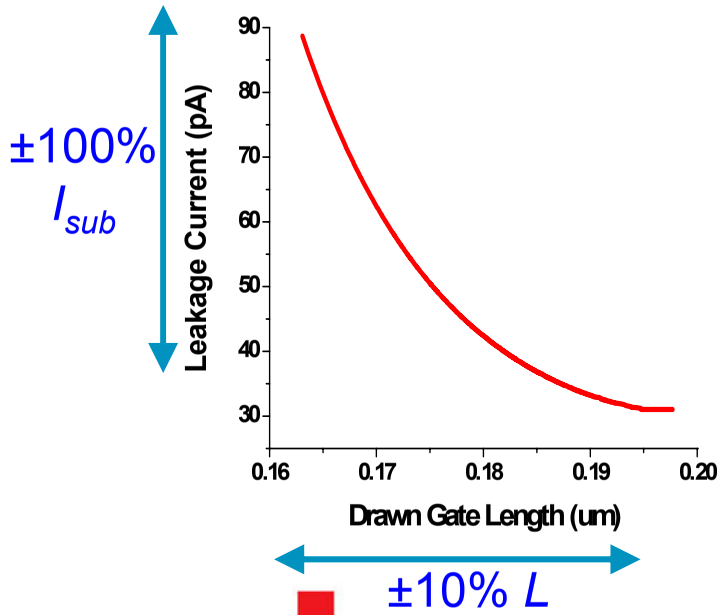
Parametric Yield Very Sensitive to Litho Process Variations

- For a 2-input NAND Gate: a change in Poly Gate Length of 10%
  - ➔ 20% in delay variations (65 NM)
  - ➔ 100% in leakage (90 NM).
- Width and length variation can be predicted by using Model Based Lithography Analysis:
  - At the Library Design level
  - At the chip level

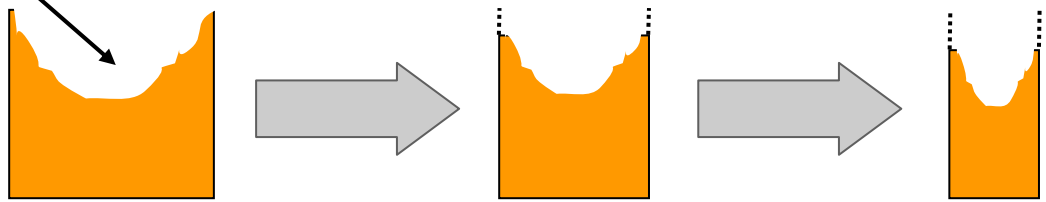




Interconnect Variations – The Z axis

Cu loss due to dishing (or erosion)

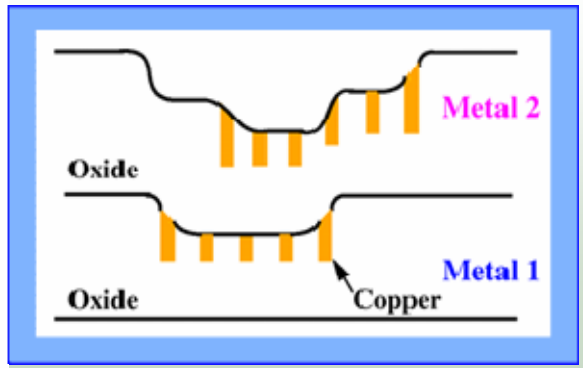
130nm > 90nm > 65nm



Decreasing Cross-Sectional Area of Line

Narrower Lines Mean Larger Impact on Electrical Parameters

Additional Metal Layers Compound the Topographical Impact



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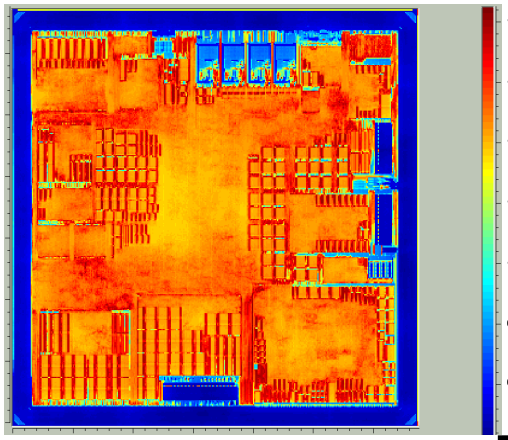
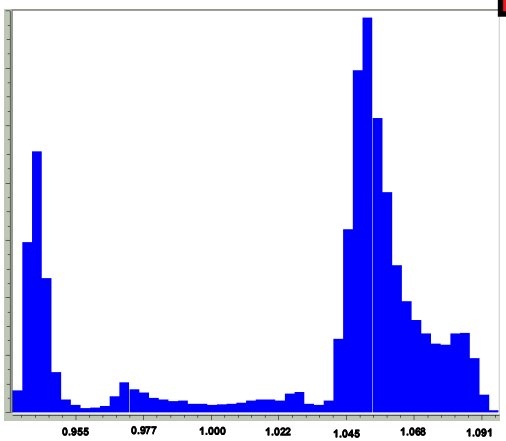
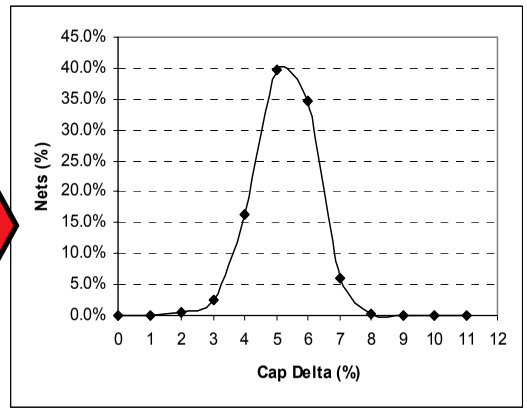
Parametric Yield Very Sensitive to CMP Process Variations

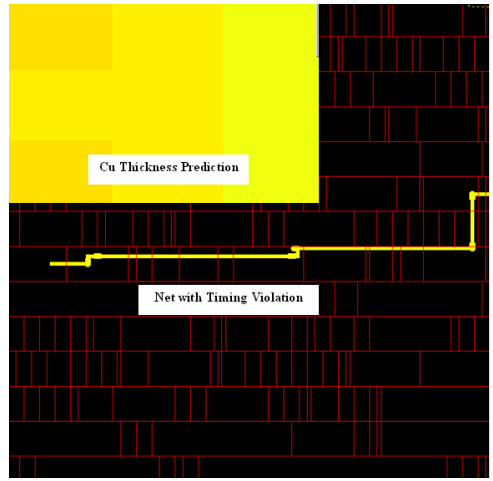




Thickness Variation



RC Variation



	Setup		Hold	
	Rule	Model	Rule	Model
Path1	OK	8ps worse		
Path2	OK	15ps worse		
Path3			Minor	OK
Path4			Minor	5ps better

Timing Variation

Joint paper "**Incorporation of CMP Modeling in RC Extraction and Timing Flow**" by H. Liao, L. Song, N. Jakatdar, R. Radojcic) submitted to DAC

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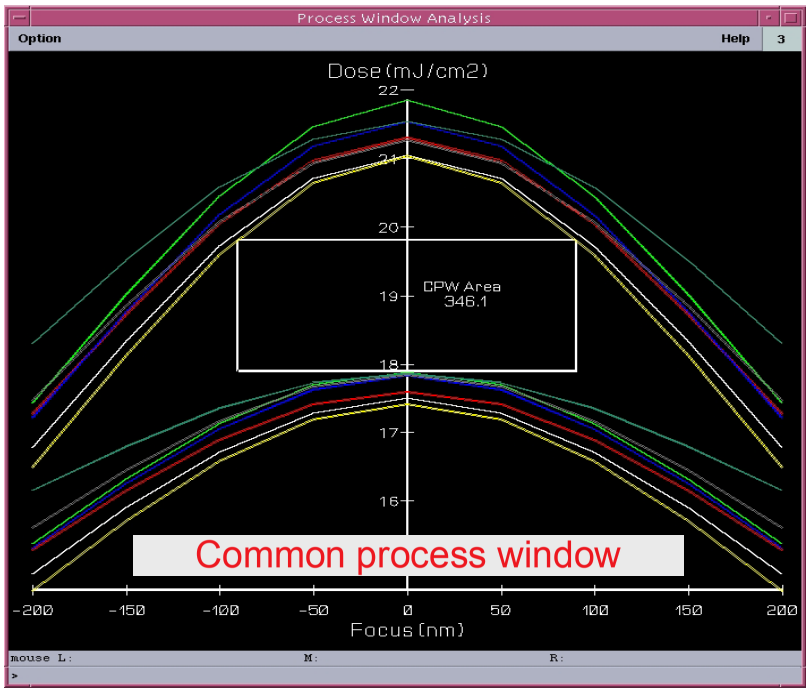
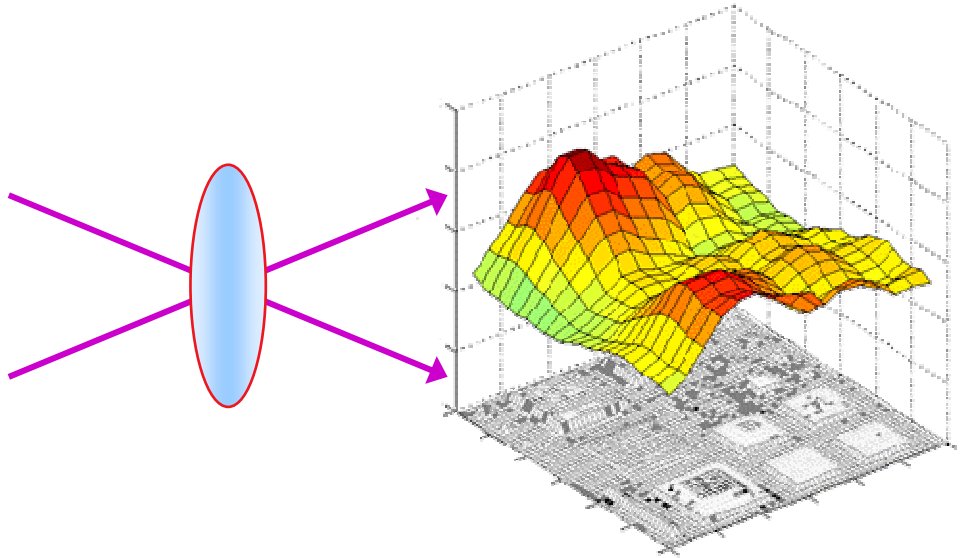
Manufacturing effects interact (2)

CMP produces big variations in surface height



DoF: +/- 100nm



Litho effect + CMP effect
= distorted / missing feature
➔ yield failure

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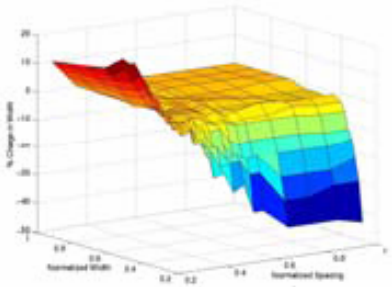
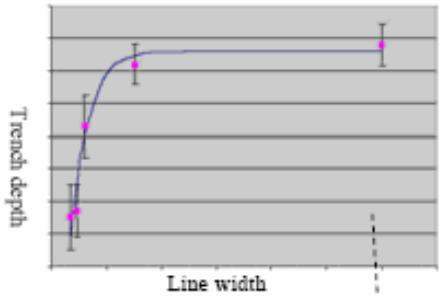
Impact of Systematic Interconnect Variations @ 65nm

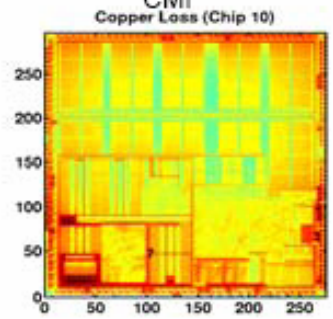
Selective Process Bias



Trench copper thickness (Etch)



CMP



Cell	Drive Strength	Pitch	Fanout	Interconnect length (um)	% Change in Frequency: SPB Width	Etch Bot thickness	CMP top thickness
INV	1x	1x	FO=1	4.7	-0.25%	1.26%	1.01%
NAND2	1x	1x	FO=1	4.7	-0.21%	1.08%	0.86%
NOR2	1x	1x	FO=1	4.7	-0.21%	1.07%	0.86%
MUX2	1x	1x	FO=1	4.7	-0.08%	0.37%	0.29%
INV	1x	1x	FO=3	4.7	-0.15%	0.78%	0.62%
NAND2	1x	1x	FO=3	4.7	-0.14%	0.71%	0.57%
NOR2	1x	1x	FO=3	4.7	-0.14%	0.71%	0.57%
NAND2	1x	1x	FO=1	10.8	-0.39%	1.98%	1.56%
INV	10x	1x	FO=1	500	0.34%	-0.96%	-1.85%
INV	20x	1x	FO=1	500	1.01%	-3.90%	-4.58%
INV	10x	2x	FO=1	500	0.02%	2.37%	-0.24%
INV	20x	2x	FO=1	500	-0.09%	0.04%	-2.04%

For short routes, metal width and thickness reduction improves speed

For long routes, metal width and thickness reduction hurts speed

10% variation assumed for etch/CMP effects

DAC-2006 DFM Tutorial

Nagaraj NS/nsnr@ti.com

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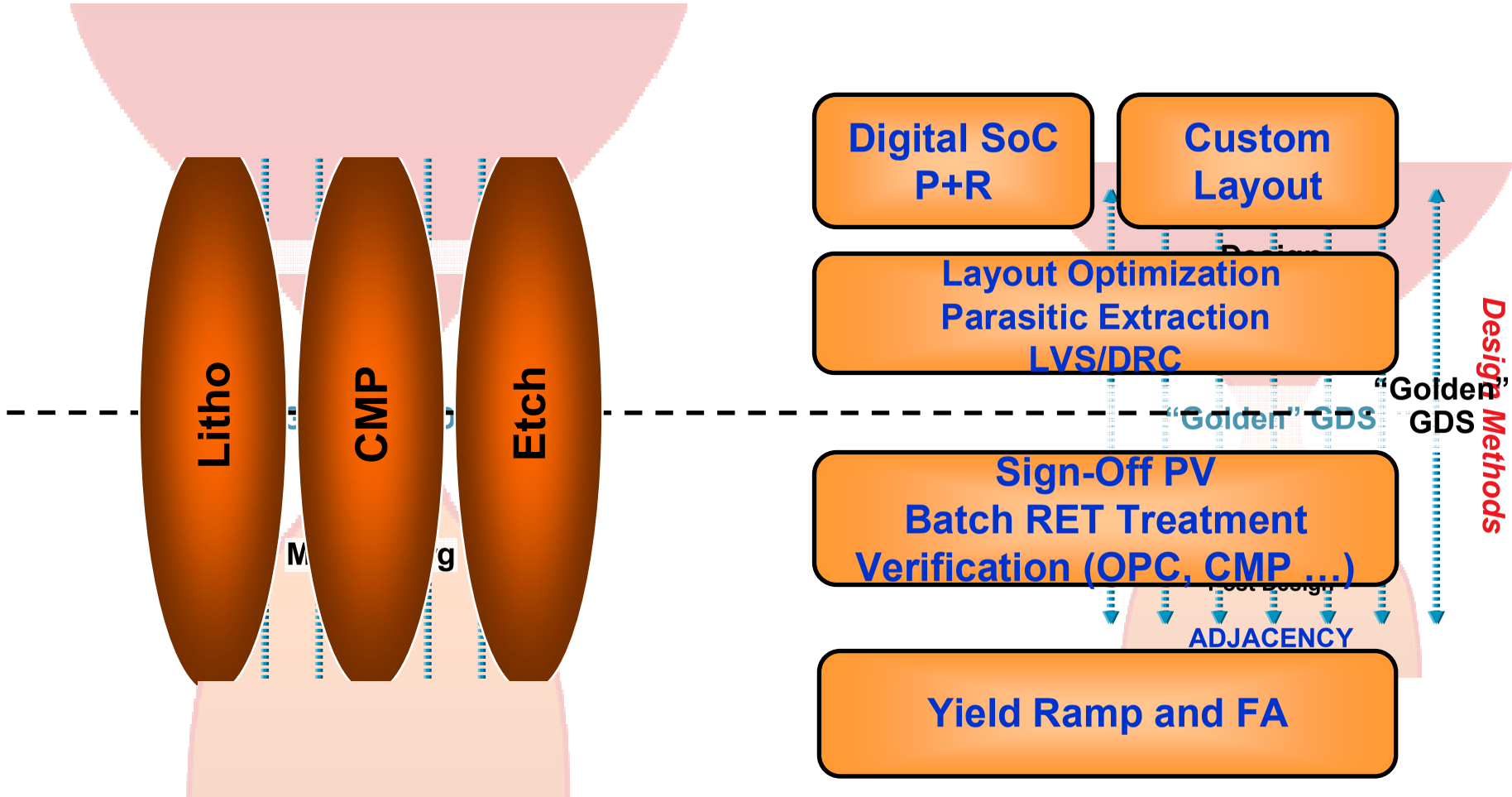
Physical Effects Connect Core to Adjacency



Industry Structure

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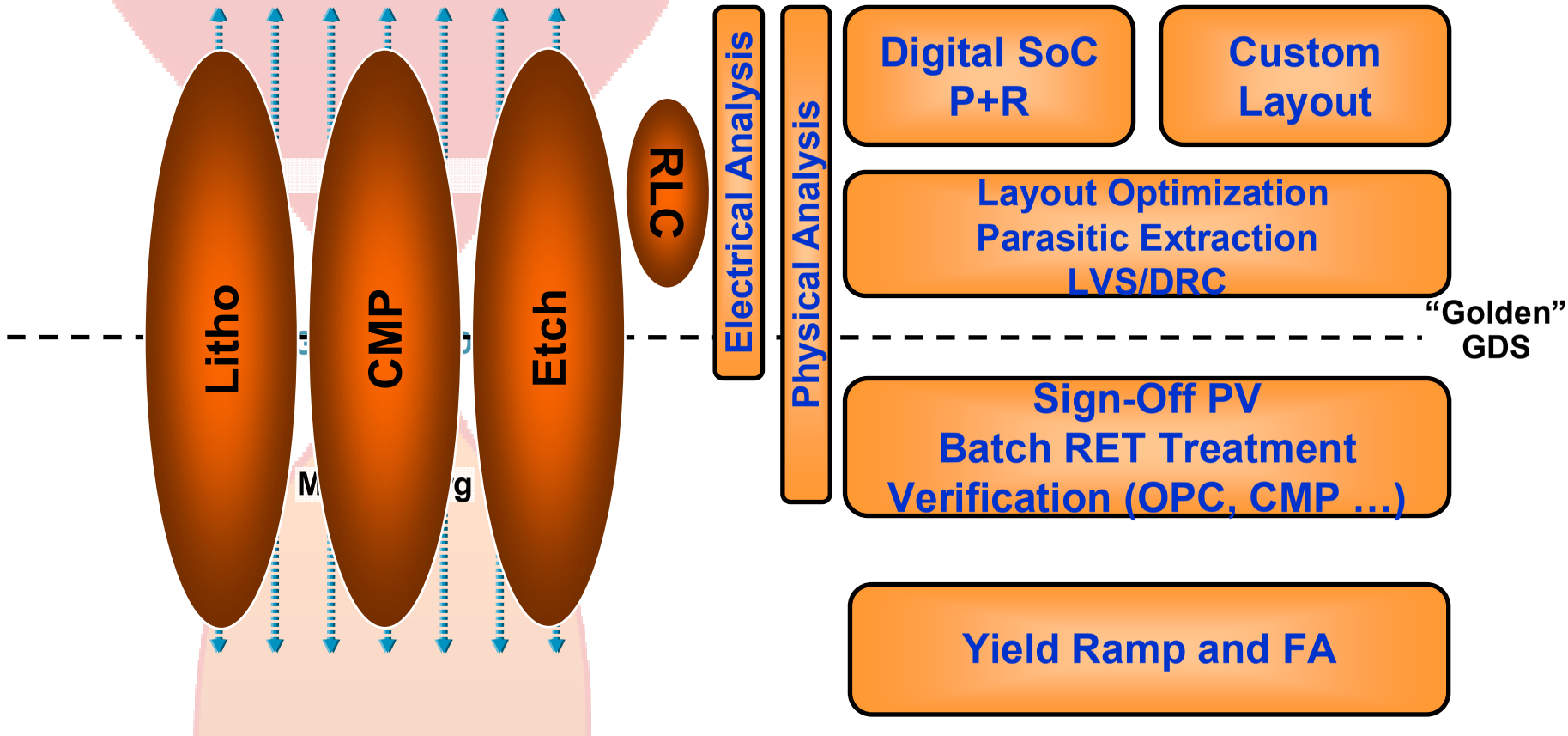
Model Based Design & Abstraction Links Implementation to Manufacturing



Industry Structure

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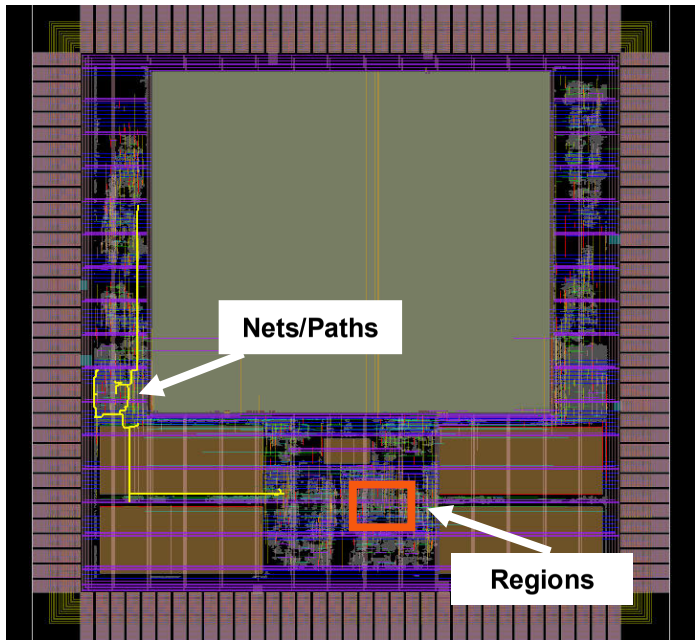
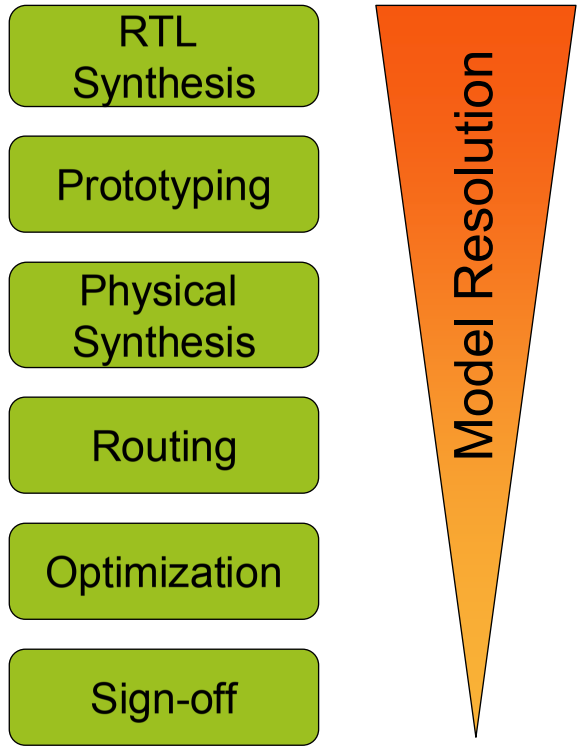
Context-based, Adaptive Model Resolution

- In the Design
  - Increased model resolution for optimizing critical and sensitive paths



- In the Flow
  - Adaptive model resolution and speed-accuracy trade-off to match abstraction level



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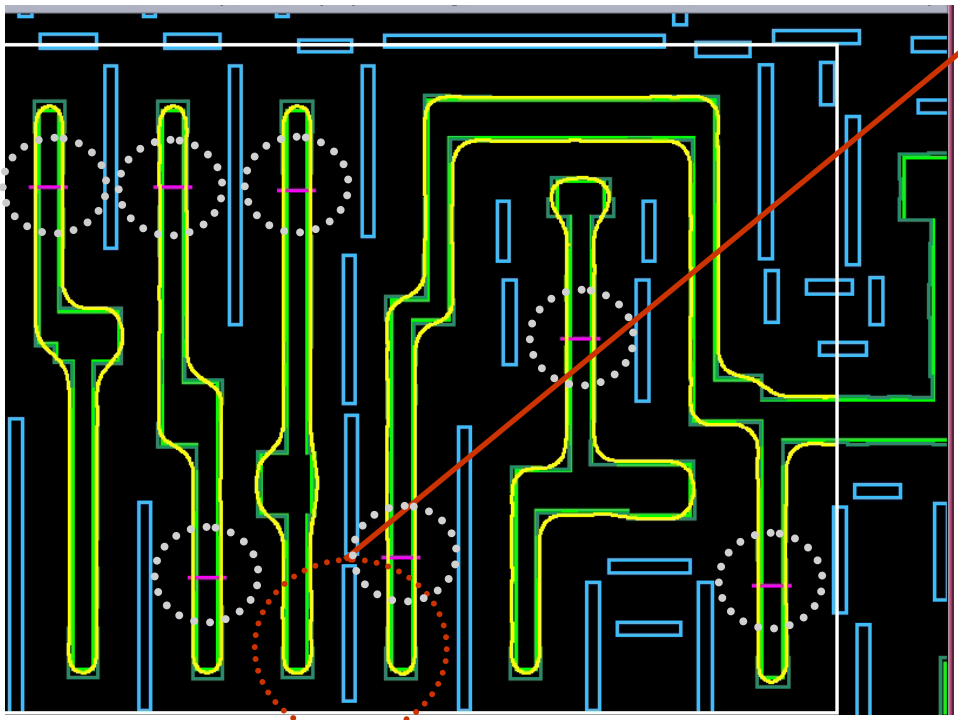
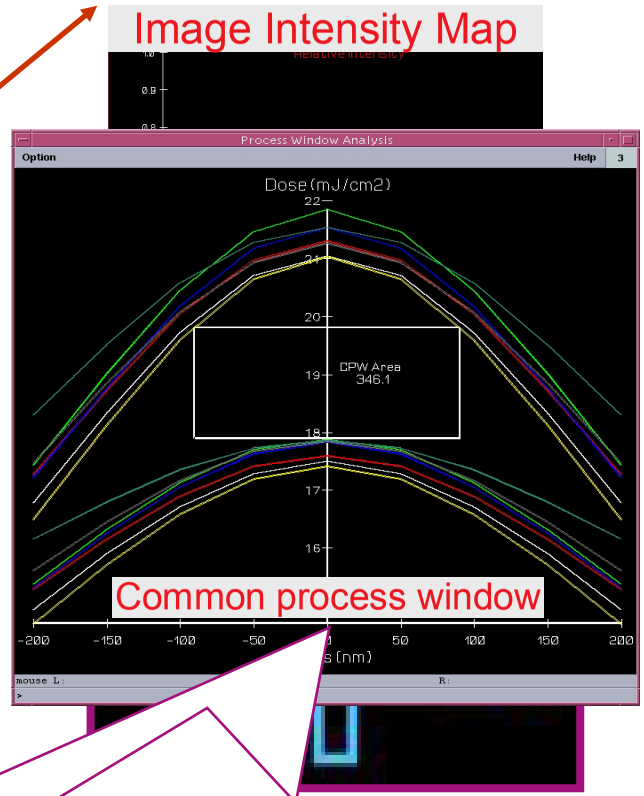
Custom Design Methods Evolution





Determine **Silicon image** of multiple post **treatment** layouts analyzed to determine sensitivity of **original** design layout with image intensity map

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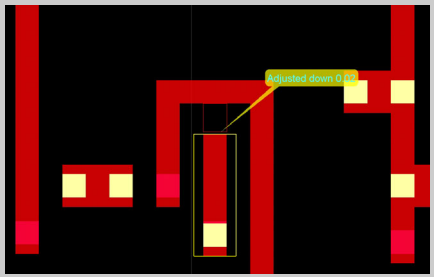
During Implementation

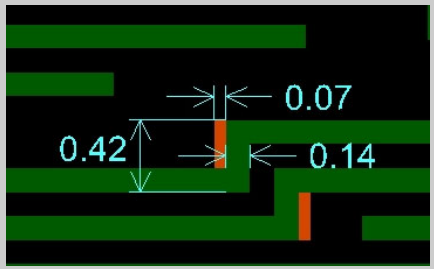
Interconnect Optimization/Litho Repair

Chip Optimizer Examples

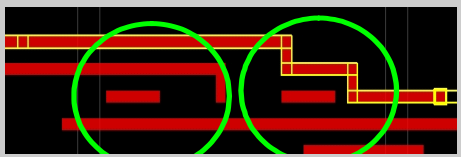
Case 1: Slide via down or move wire - 20nm



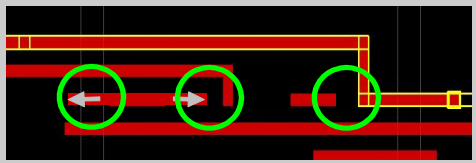
Case 2: Widen jogs



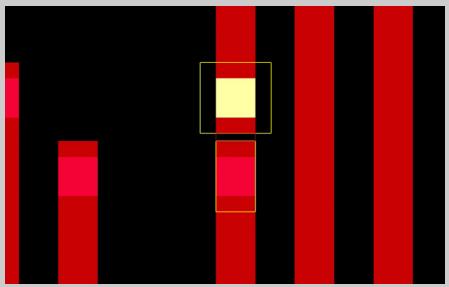
Case 3: Before



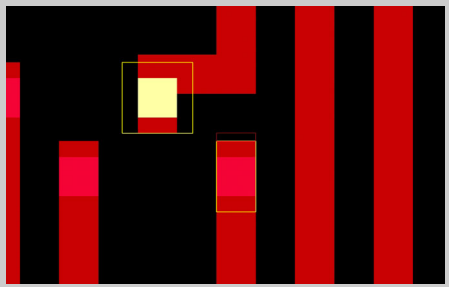
After (bend/topo optimization)



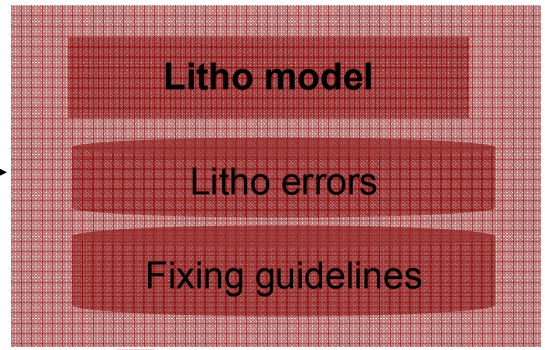
Case 4: Before



After (wire/via move)



- Low perturbation with controllable electrical characteristics
- Fast and precise with high fix rates
- Incremental timing analysis



Cadence Chip Optimizer

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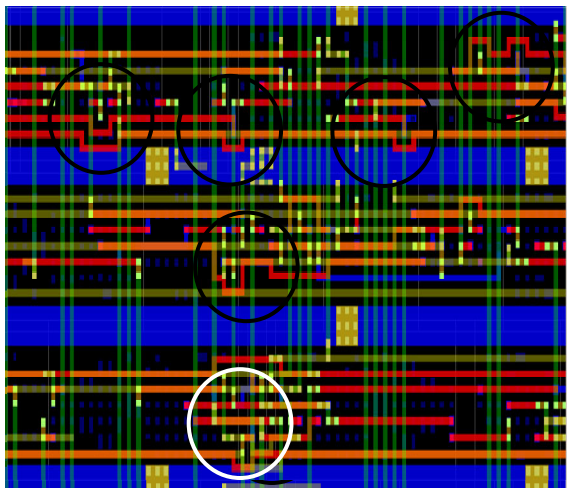
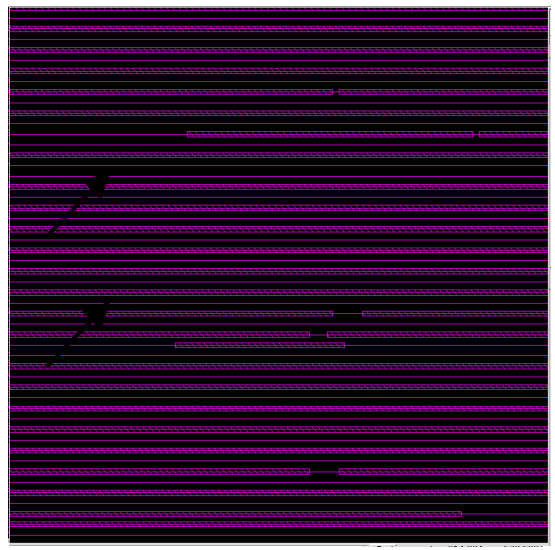
Smart routing prevents yield problems

- New layout rules and guidelines
- Redundant vias and reduced via count
- Wire spreading

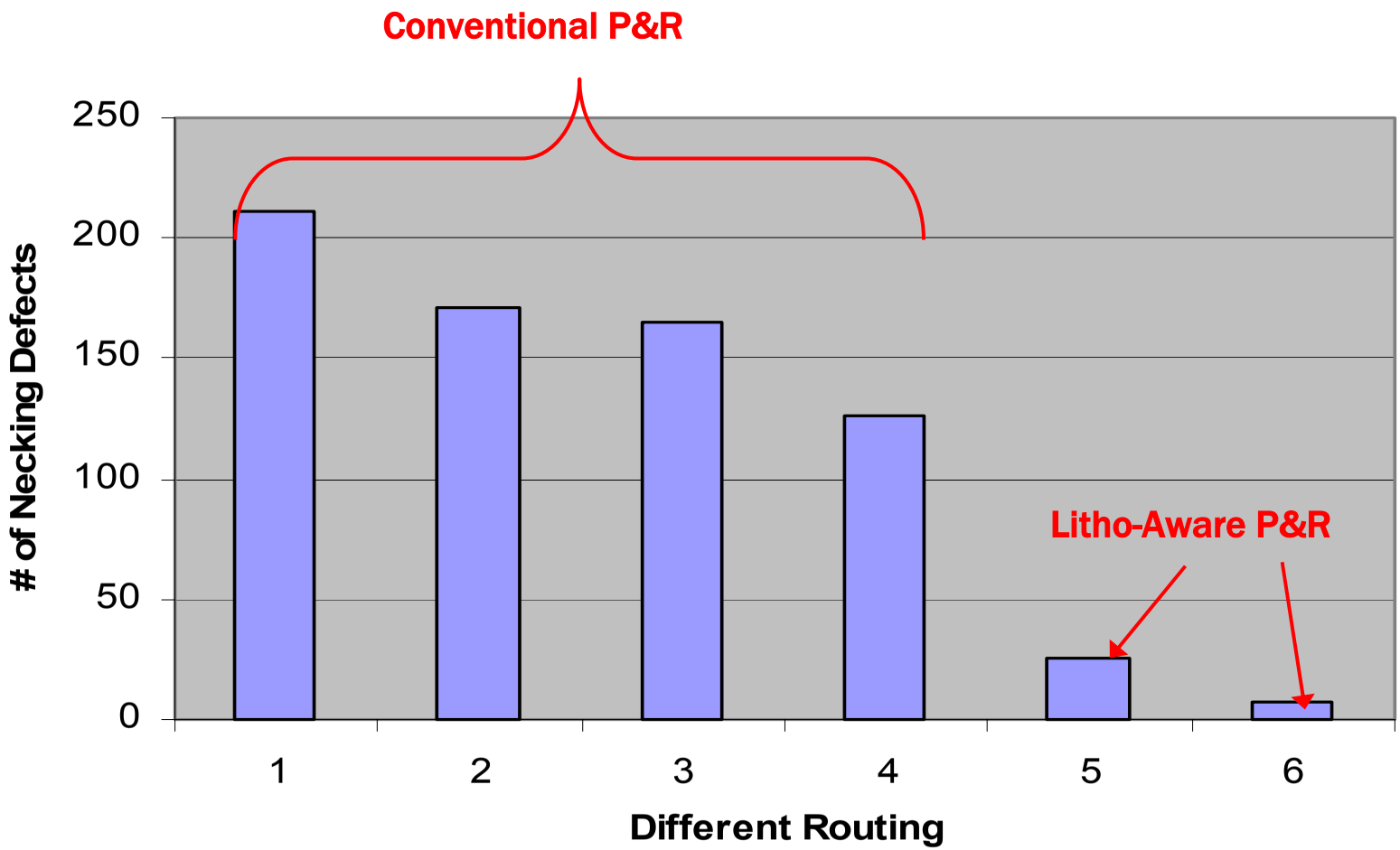


Via optimization



Wire spreading

During Implementation
Litho Aware Routing



SoC Encounter

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DfM Implementation: Key Take-Aways

- Models are required to reduce guard band by improved modeling of systematic effects
- A platform for concurrent analysis and optimization of effects is required for convergence
- Incremental analysis is required for optimization
- Margin driven model accuracy is needed to focus computational resources


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