Research of Germanium on Insulator

Haiyan Jin, visiting scholar

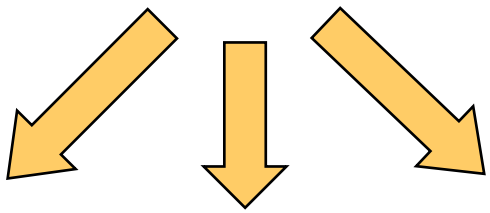
Collaborators: Eric Liu and Prof.Nathan Cheung
EECS, UC Berkeley

The work is supported by the UC Discovery
FLCC and IMPACT programs

Seminar

Institute of Microelectronics

Peking University, Beijing, China



ULSI SOC MEMS

Wang Yangyuan
Professor and Director of
Institute of Microelectronics

Professors : 49

Undergraduate students : 60~80/year

Graduate students : 40~55/year

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National Key Micrometer/Nanometer Processing Lab

- Over 10-million USD process and analyzing equipment in a 900m² clean room.
- CMOS, Bipolar, especially MEMS baseline process.

OUTLINE

Part I State of the art on GeOI

- An introduction to GeOI
- Main approaches for GeOI fabrication

Part II Our research about GeOI

- Bulk and Epi Ge wafer are transferred on substrate
- A new method was presented to extract mobility
- Mobility and interface trap density are improved

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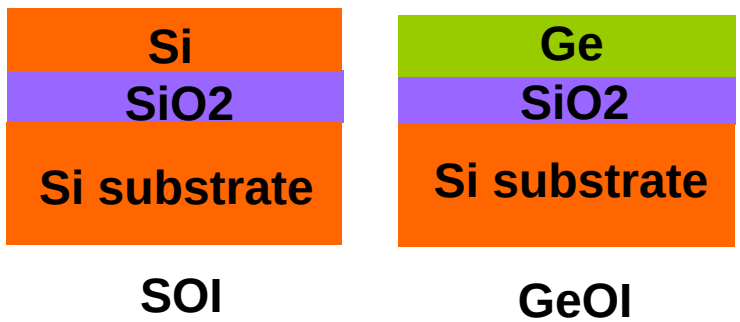
Part I State of the art on GeOI

- An introduction to GeOI

  What is GeOI ? GeOI = “Ge”+ “OI”



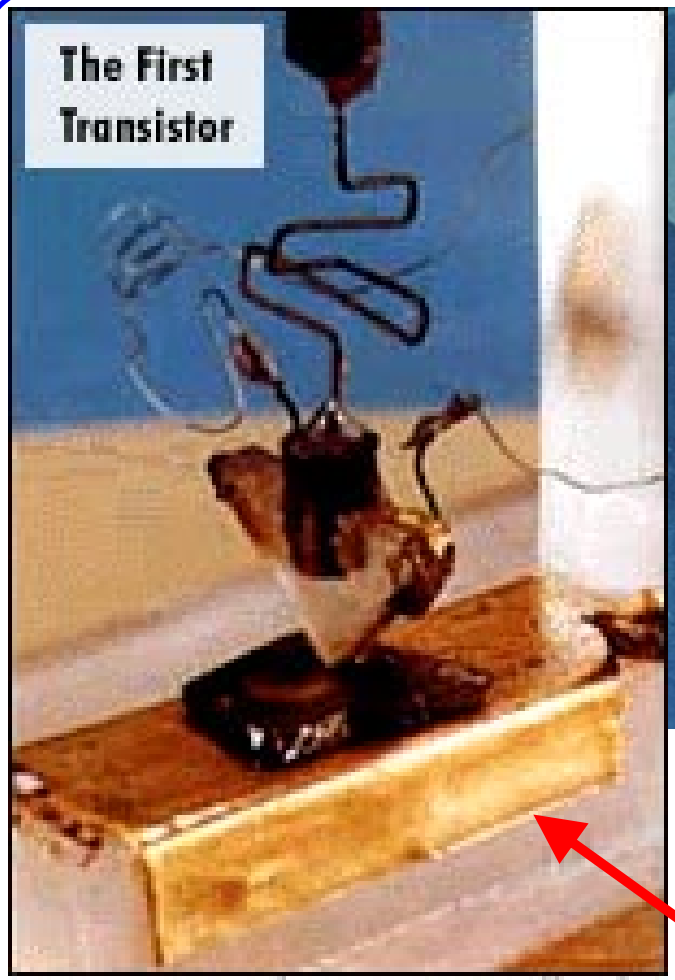
Why GeOI ?

Advantages of “Ge”

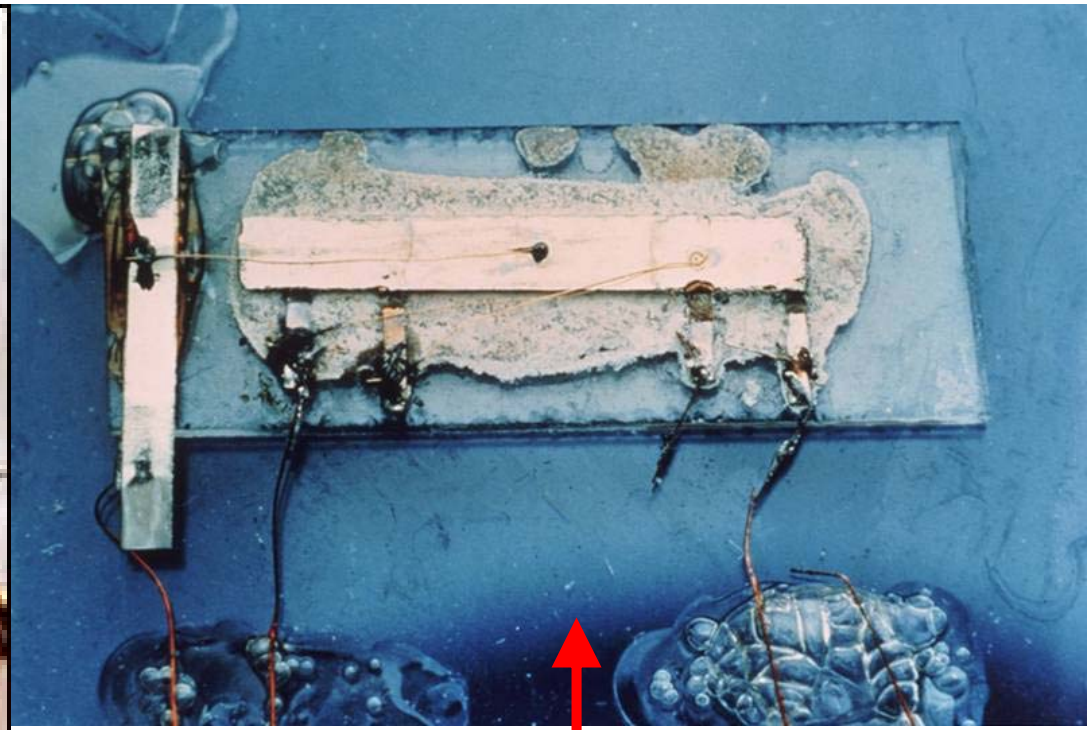
- Significantly higher bulk electron and hole mobilities
- Higher thermal injection velocity
- Lower Schottky barrier due to smaller Ge band-gap
- Allowing a smaller V_{DD}

Advantages of “on-Insulator”

- Partially overcoming the high leakage current
- Potential substrate for FinFET structures



copyright: Lucent / Bell Labs



- Texas Instruments' first IC made by Jack Kilby in 1958
- The first transistor was invented in 1947 by William Shockley, John Bardeen and Walter Brattain.

The first transistor and IC are all made of Germanium

The Myth: Si is the newer technology

Identified by Lavoisier in 1787

B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb

In 1886, Coca Cola was invented

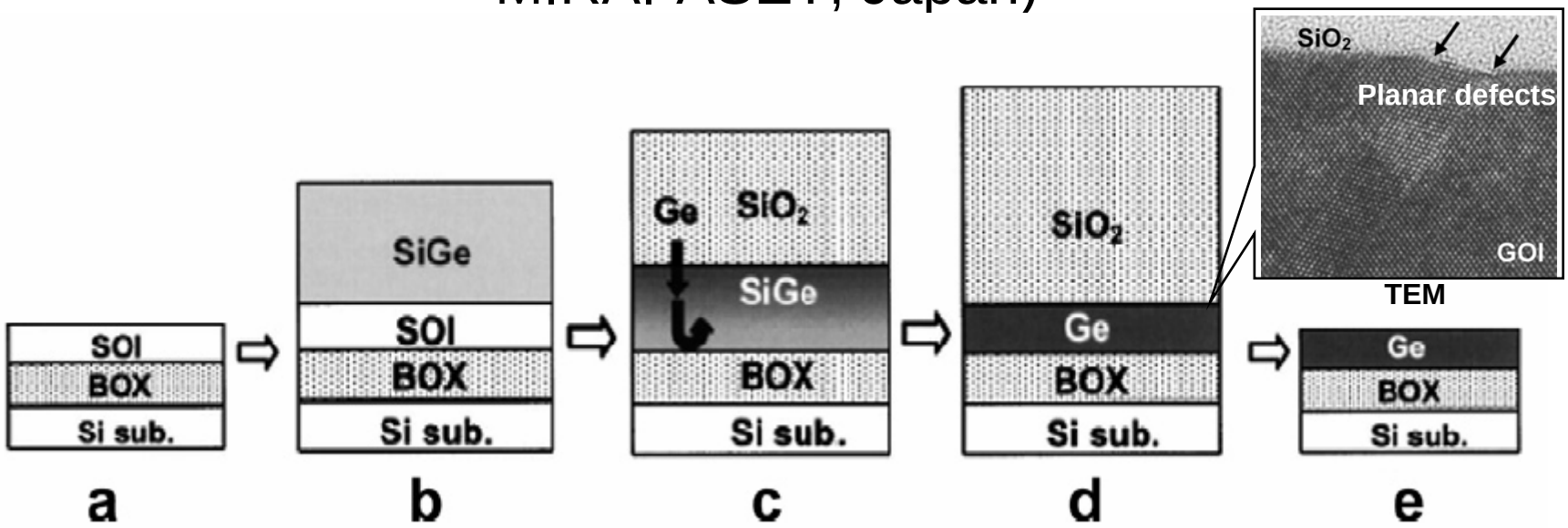
Identified in 1886

Part I State of the art on GeOI

- An introduction to GeOI
- Main approaches for GeOI fabrication
  - Ge condensation method
  - Rapid Melt Growth
  - Mechanical and Thermal Ion-Cut

Ge condensation method

(This method is first presented by S.Nakaharai, MIRAI-ASET, Japan)



• Ge condensation technique: (a) Commercial SOI wafer, (b) SiGe layer is grown epitaxially on an SOI wafer, (c) Oxidation of SGOI, (d) Complete Ge condensation and (e) GeOI wafer after removing surface oxide.

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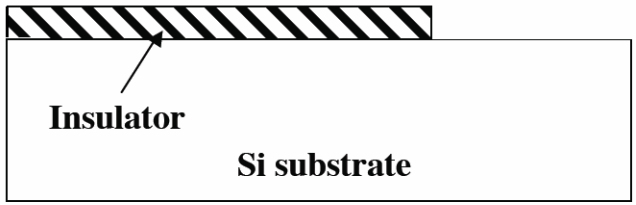
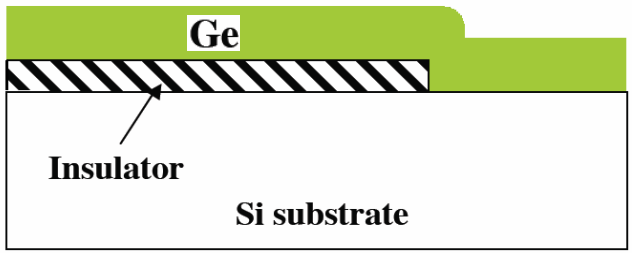
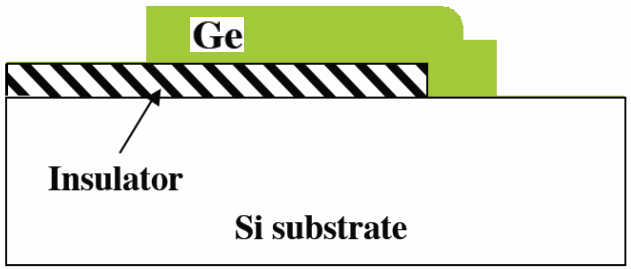
Rapid Melt Growth (RMG)



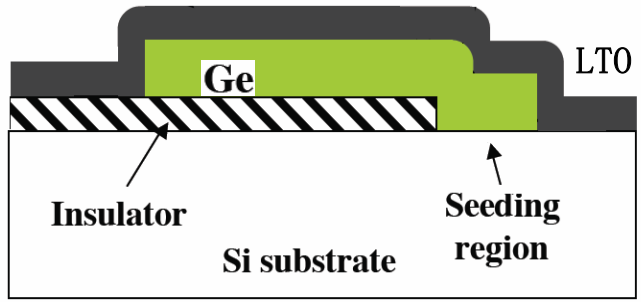
(a) Seed windows are etched



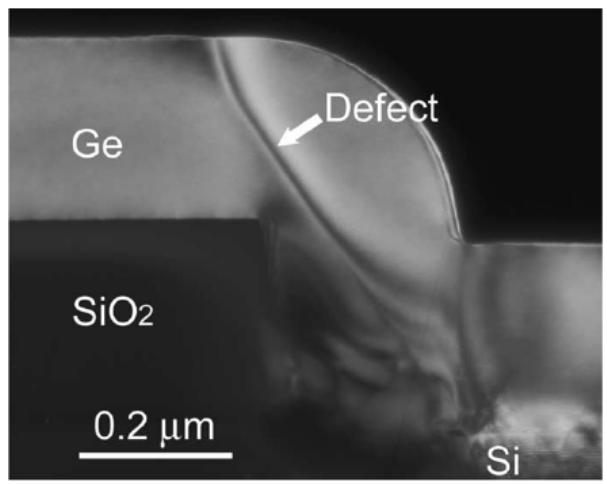
(b) Ge is deposited by CVD



(c) Ge film is patterned into stripes



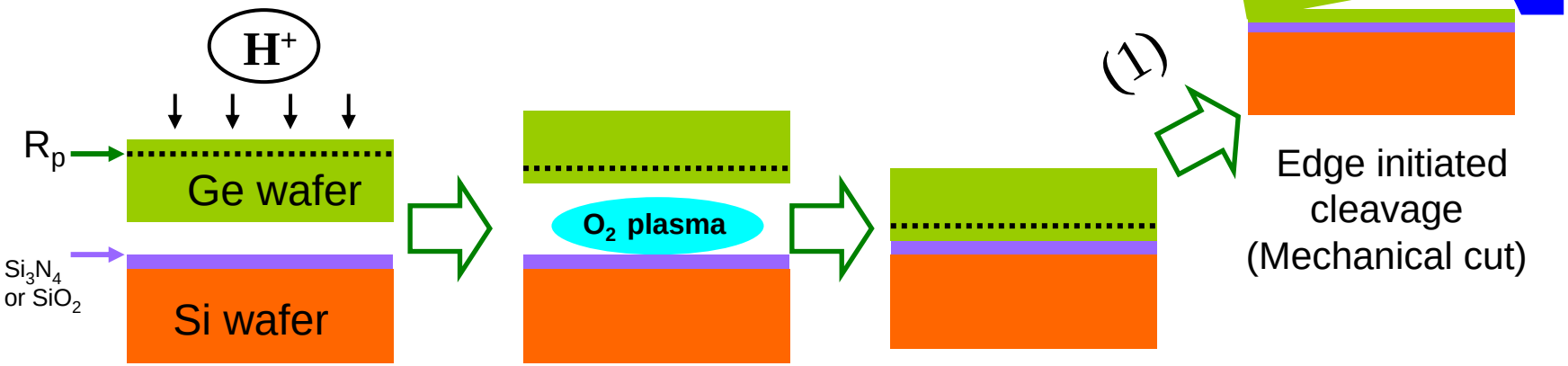
(d) Ge stripes is covered by LTO



TEM image of GeOI obtained by RMG

Y.Liu et al., Stanford University

Mechanical and Thermal Ion-Cut



(a) H+ implantation to Ge (dose:$6x10^{16}/cm^2$);
i) LPCVD Si_3N_4 on Si
ii)Thermal SiO_2 on Si

(b) Oxygen plasma activation for 15sec

(c) Ramp anneal at 200~250° C

A 200mm GeOI formed by thermal-cut method (Soitec, France)

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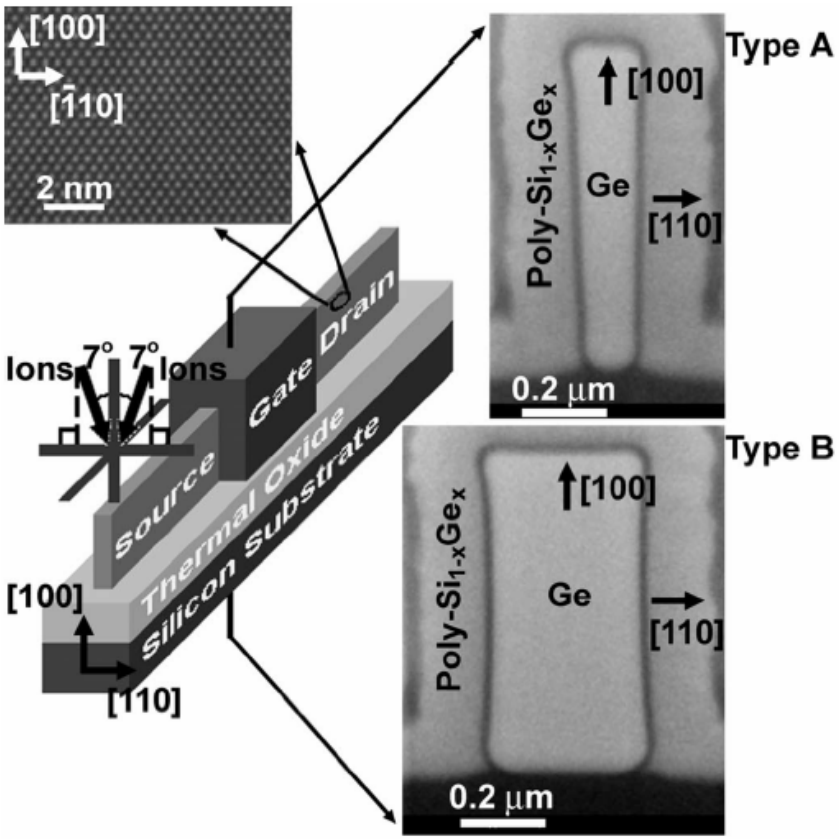
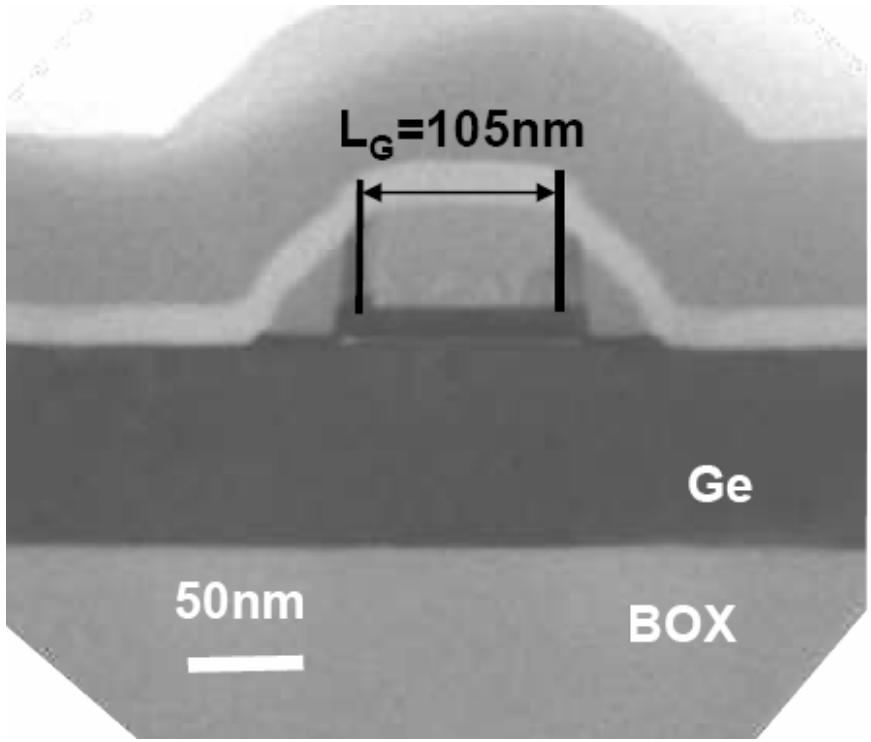
GeOI device



P-Channel Germanium FinFET
Based on RMG
Jia Feng, et al.(Stanford University), EDL, 2007



First Deep Sub-Micron GeOI PMOSFET
A.Pouydebasque, et al.
(CEA-LETI MINATEC, FRANCE)

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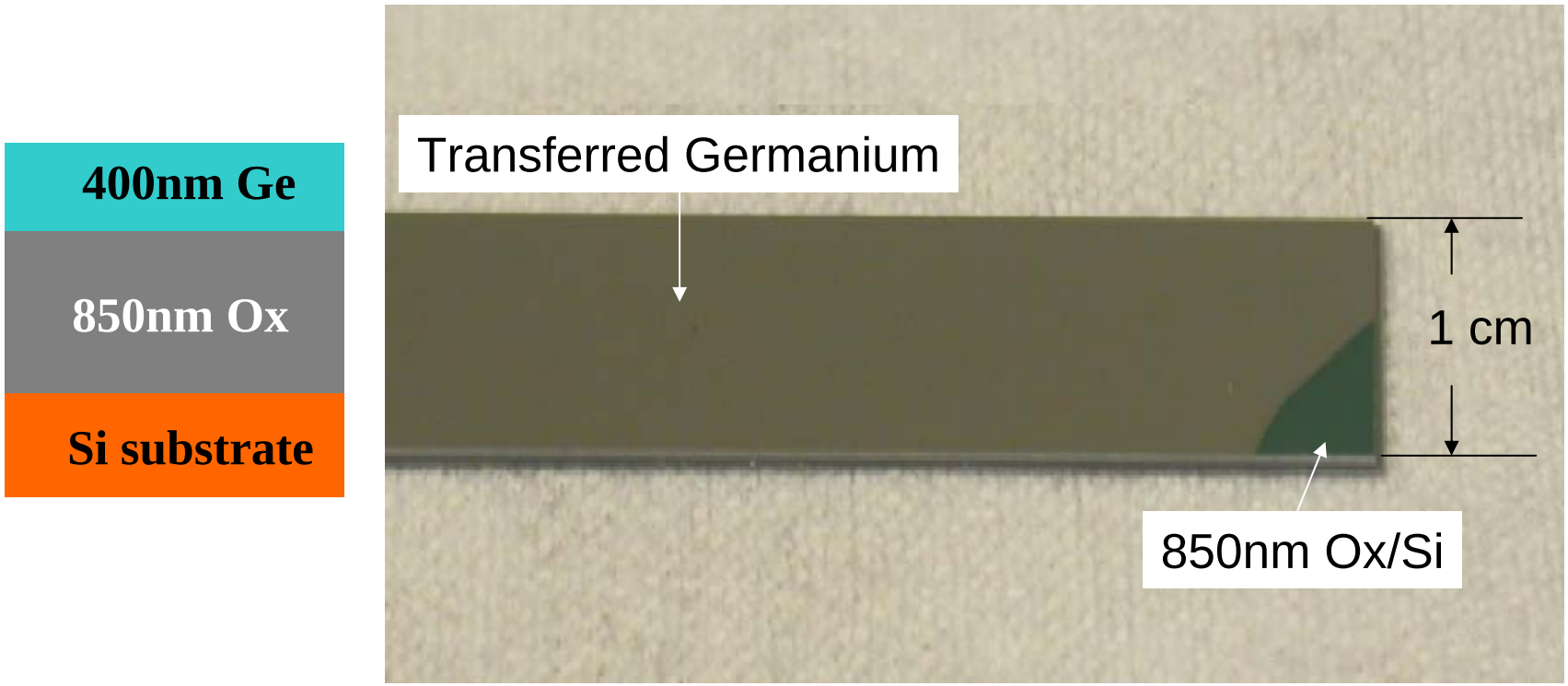
Advantages of ion-cut method

- Wafer-scale transfer for all wafer sizes
- Layout Pattern independent
- High quality GeOI decided by bulk Ge or Epi-Ge
- An extension of mature SOI technology

Part II Our research about GeOI

- Bulk and Epi Ge wafers were transferred
- A new method was presented to extract mobility
- Mobility and interface trap density are improved

Large-area GeOI formed by layer transfer processing



Fabrication processes:

(1) HF/DIW surface cleaning (pre-bonding cleaning); (2) N_2 plasma activation; (3) Direct bonding; (4) Post-bonding annealing at 220 ℃; (5)Mechanical-cut or thermal-cut at T>270 ° C ;

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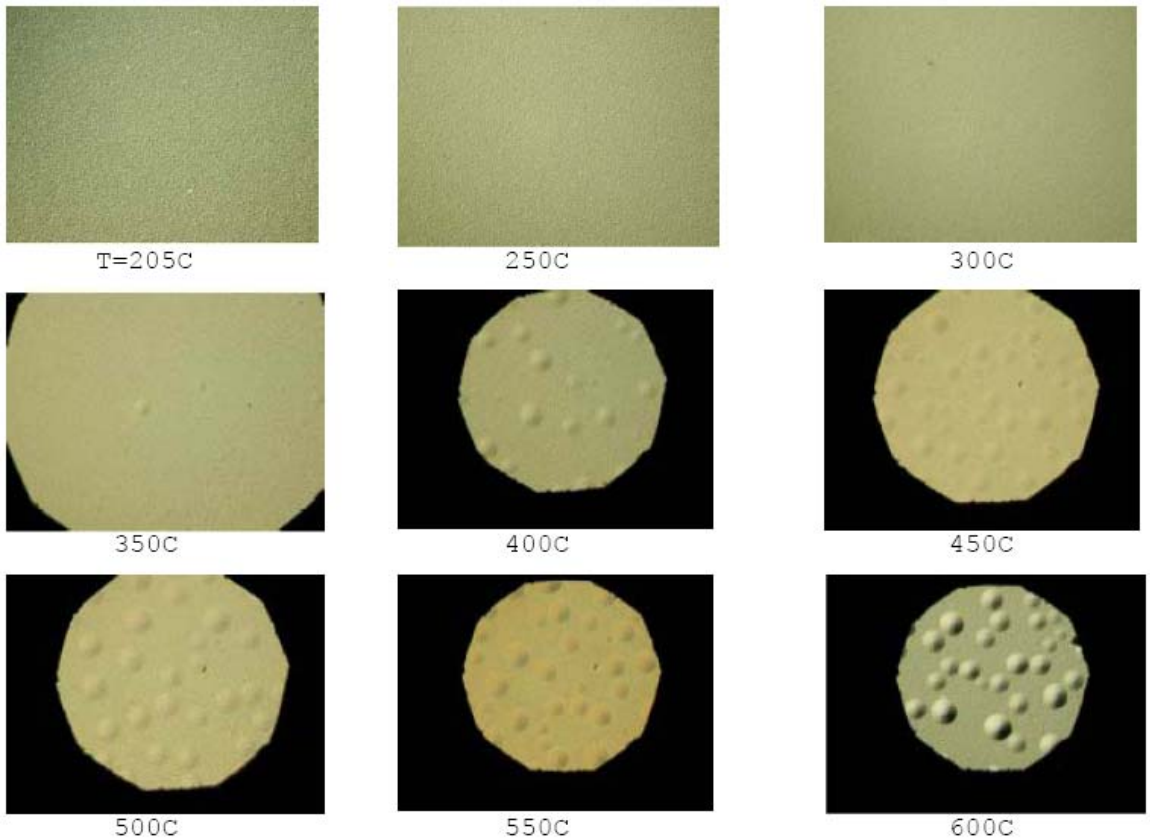
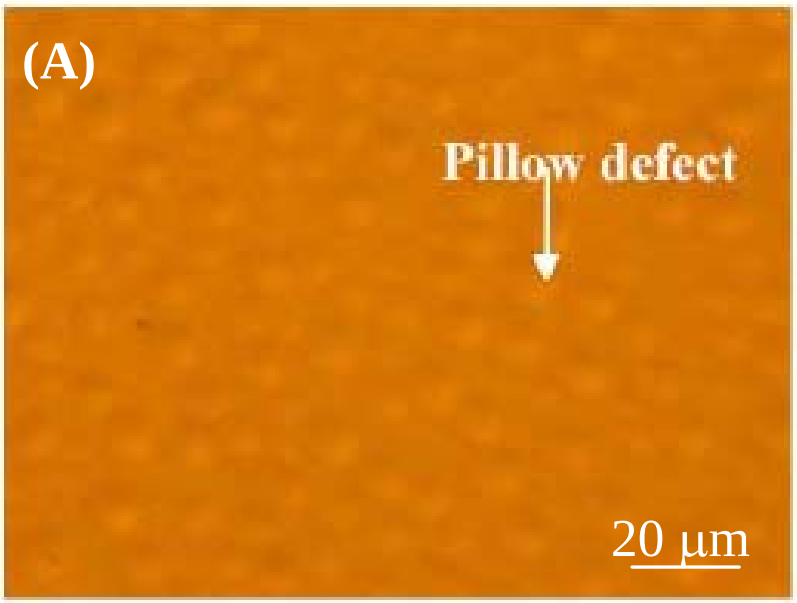
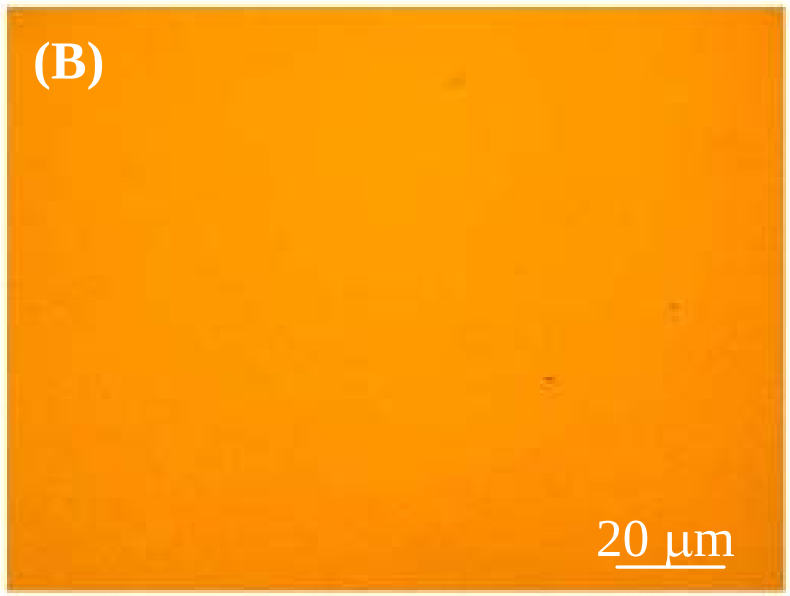
Pillow defect



The pillow defects of GeOI annealt at various temperature. No Ge wafer surface cleaning is performed before wafer bonding. The origin of pillow defects is usually attributed to contamination on the Germanium wafer surface such as hydrocarbons.

Layer Transfer Process Improvement

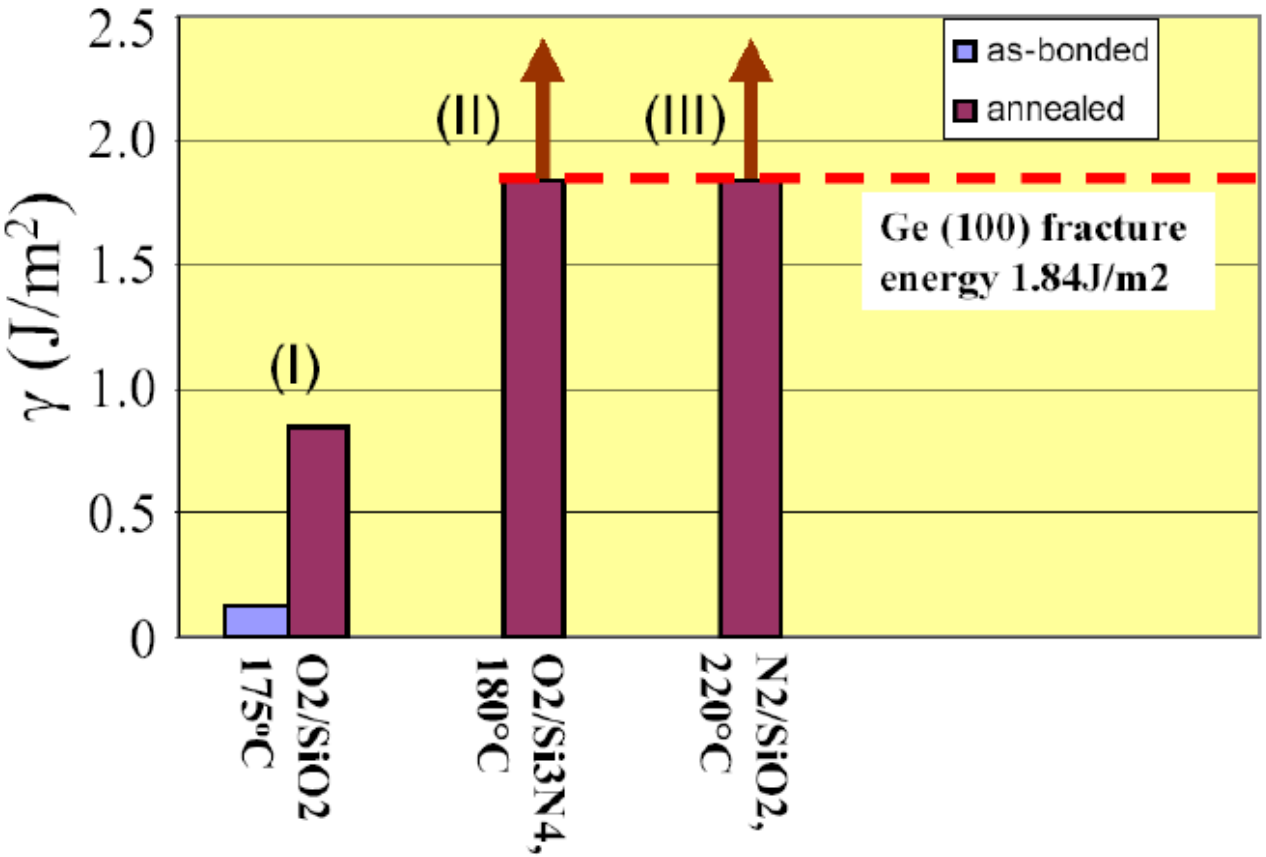




(A)GeOI sample after 540°C anneal for 90 min without pre-bonding cleaning

B)GeOI sample after 540°C anneal for 90 min with pre-bonding cleaning

Plasma surface activation



Bonding energy of Ge with (I) SiO_2/Si, O_2 plasma surface activation; (II) Si_3N_4/Si, O_2 plasma surface activation; (III)SiO_2/Si, N_2 plasma surface activation.

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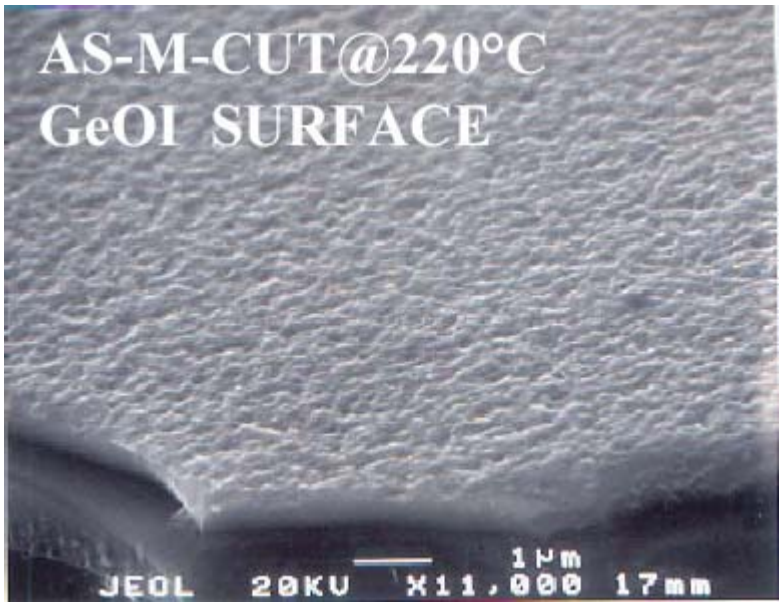
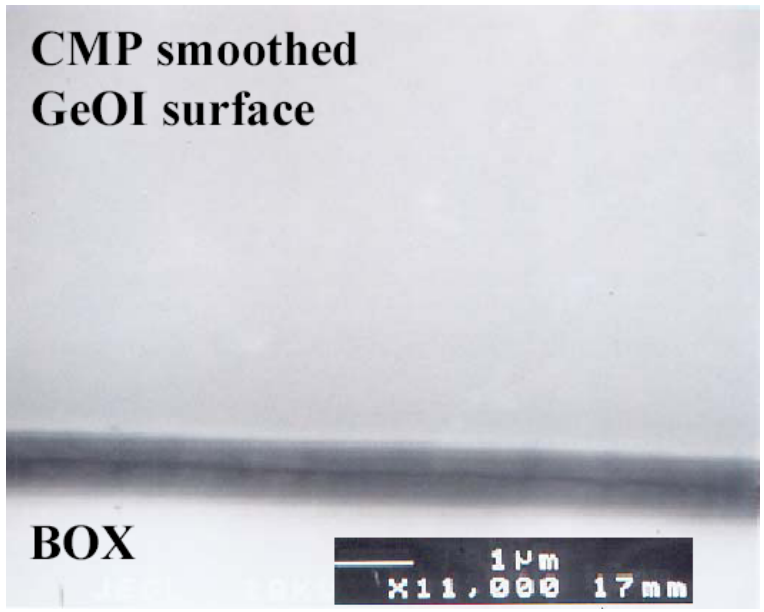
GeOI surface smoothing with CMP





- GeOI surface can be smoothed down to RMS =0.3nm by CMP
  (CMP slurry: 0.2μm SiO2 particle mixed with KOH)
- GeOI substrates are ready for device fabrication

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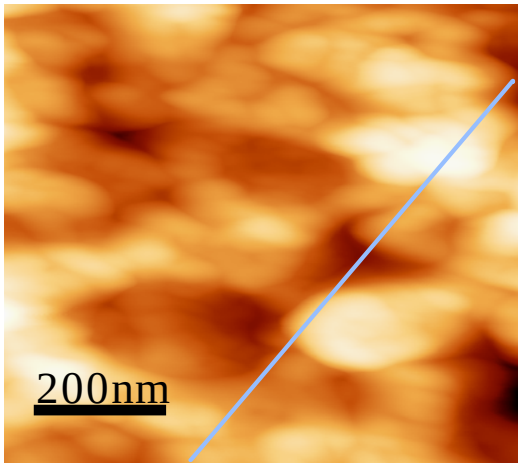
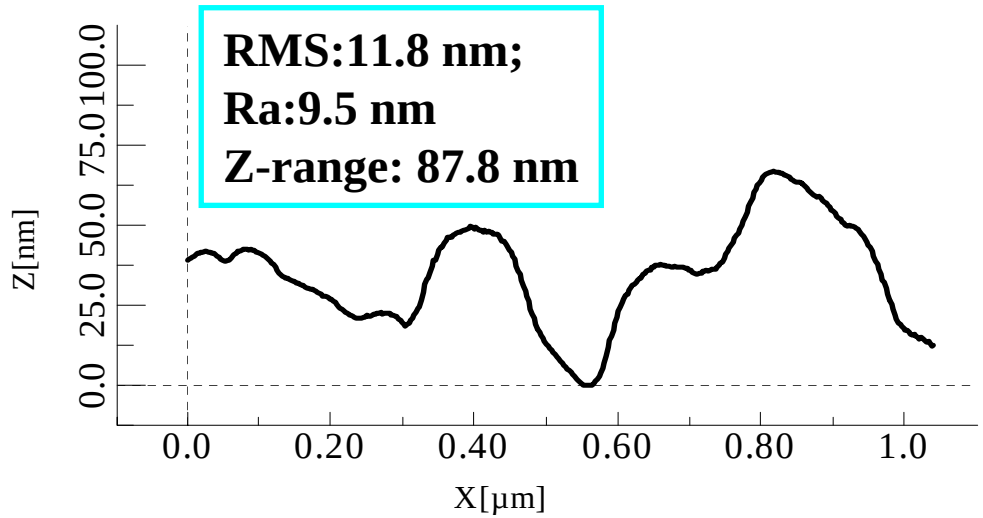
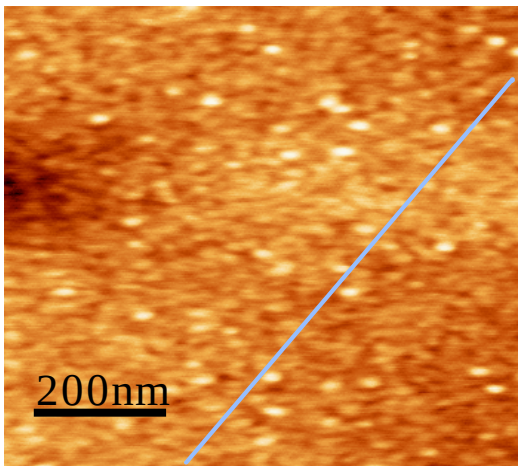
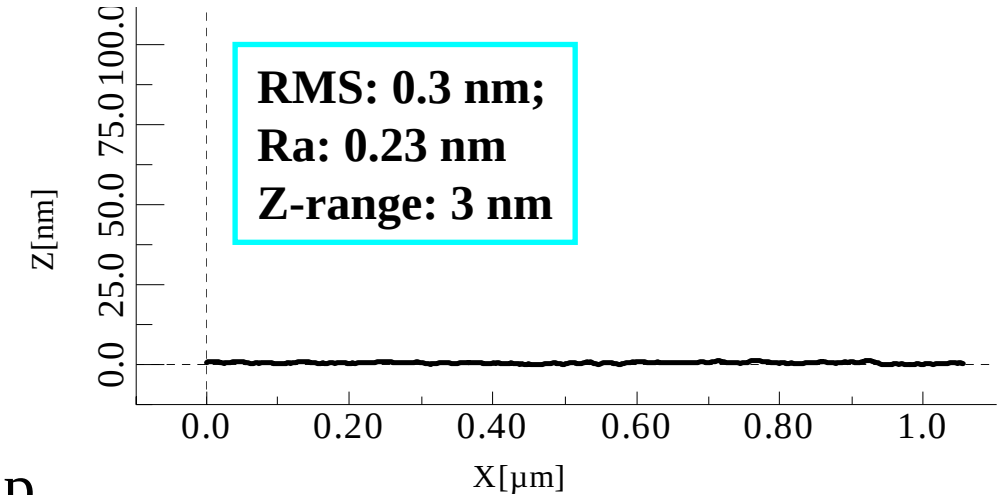
The GeOI surface smoothing by CMP





(a) as-cut GeOI





(b) after CMP and HF dip

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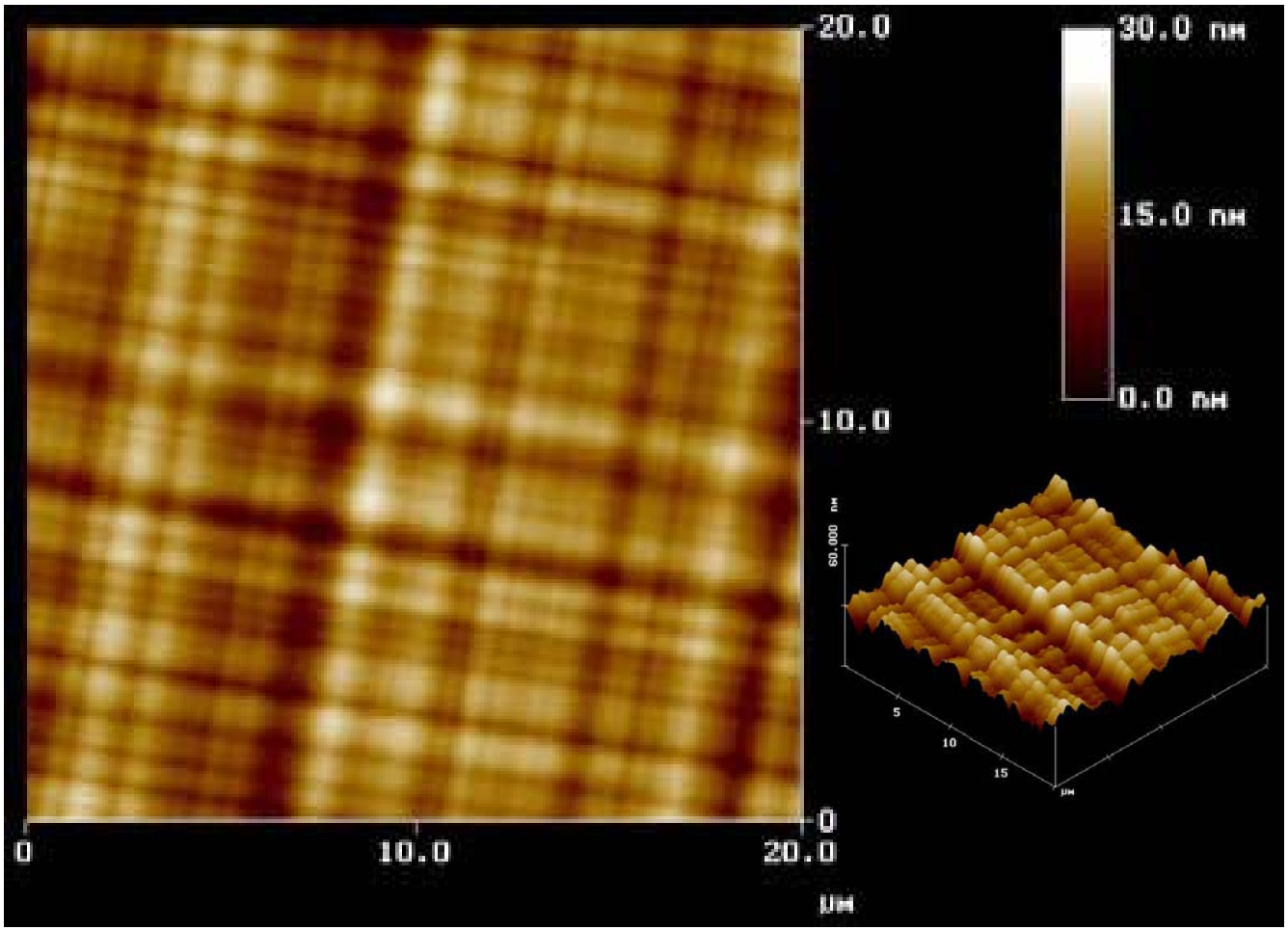
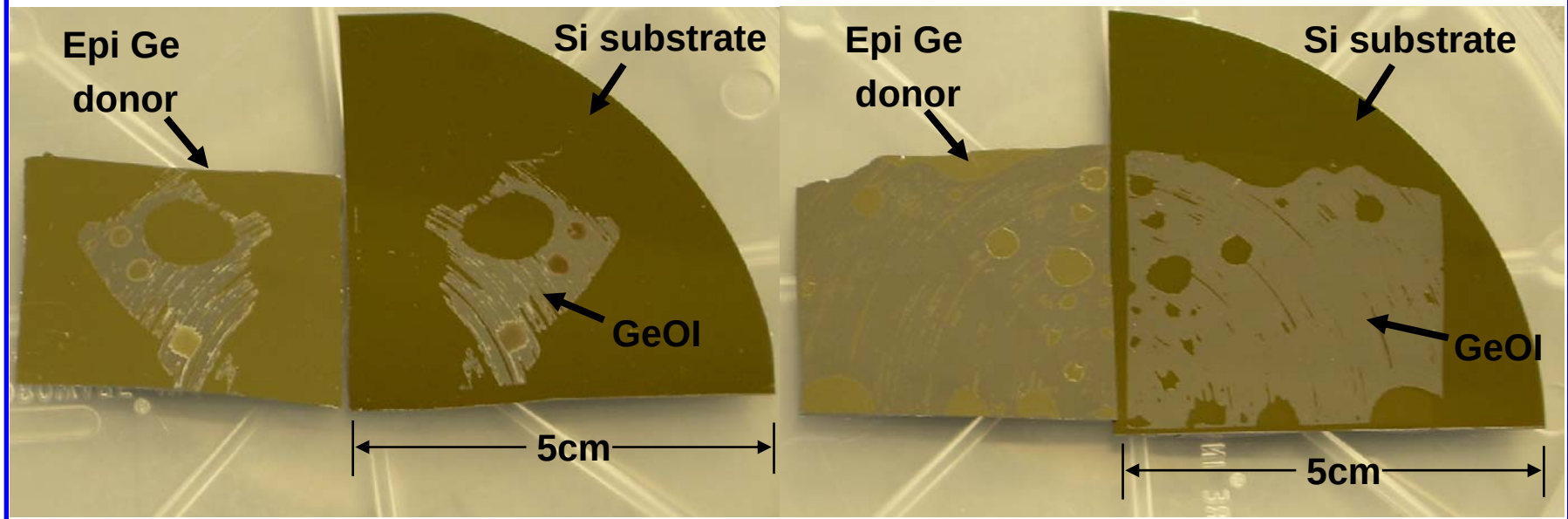
300mm Ge wafers (UMICORE)

Surface steps of Epi-Ge wafer



AFM image of a Epi-Ge surface

Large area Epi-Ge is transferred



3 days furnace annealing 7 days furnace annealing

Temperature increases slowly from 120 ℃ to 300 ℃

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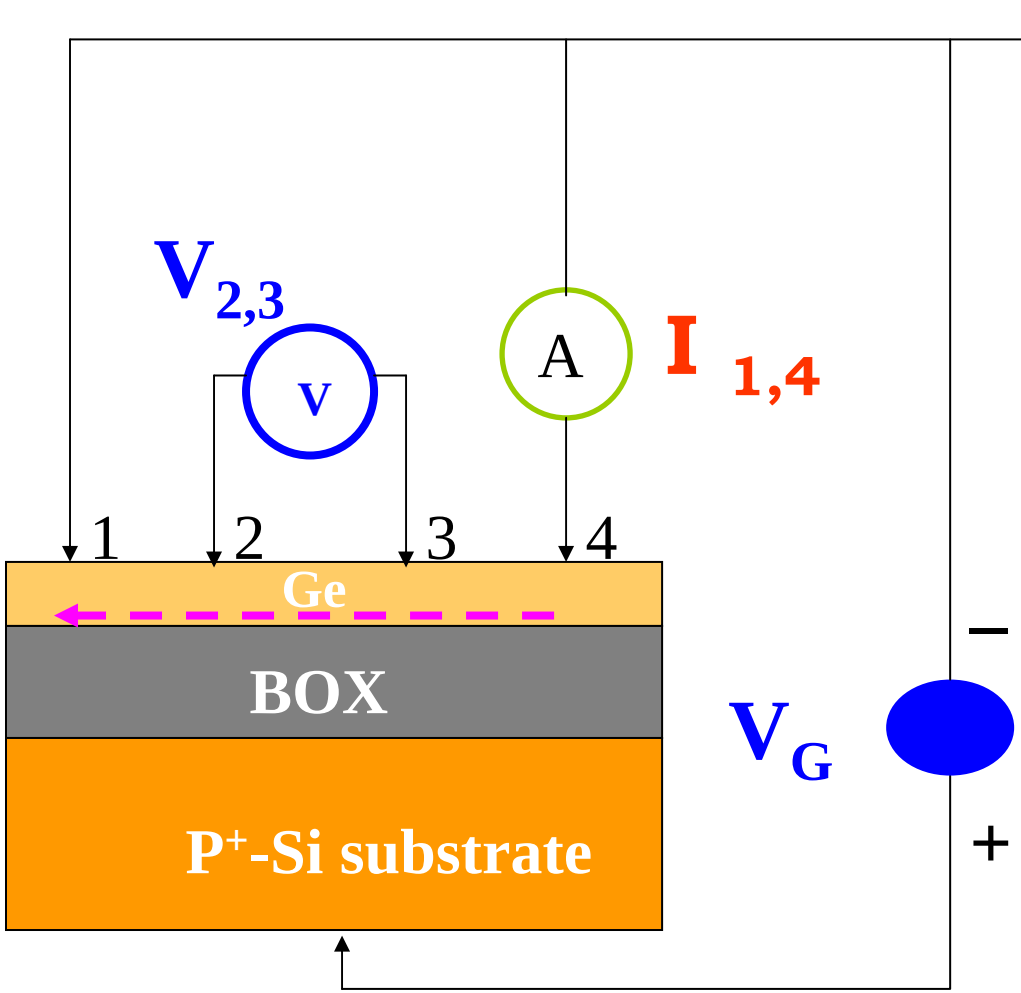
Part II Our research about GeOI

- Bulk and Epi Ge wafer are transferred on substrate
- A new method was presented to extract mobility
- Mobility and interface trap density are improved

Pseudo MOSFET Measurement (4-probe configuration)



- Rapid electrical evaluation of semiconductor-on-insulator substrate
- Extracting interface carrier mobility of GeOI

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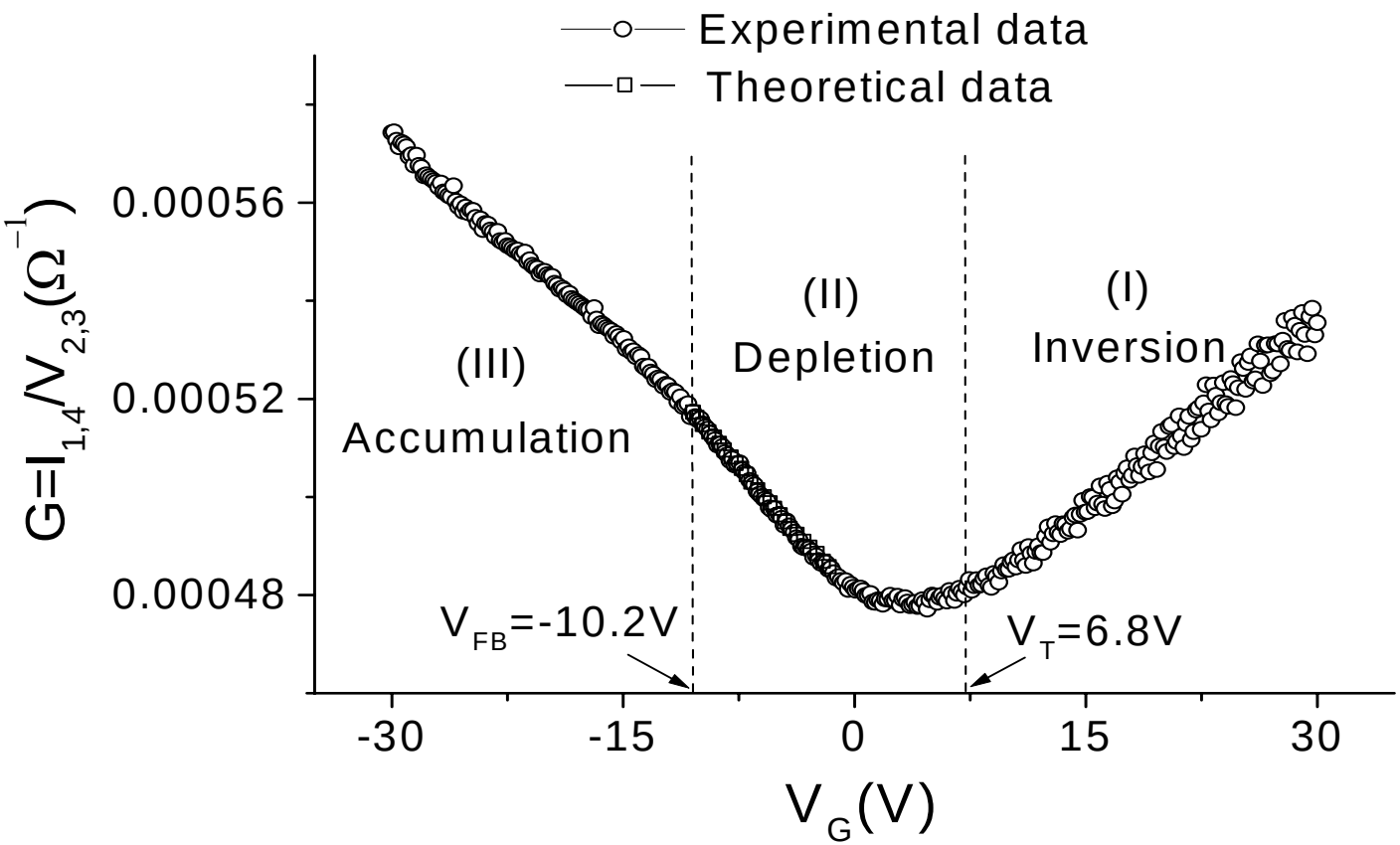
The pseudo-MOSFET experimental data



G vs VG plot, which shows the accumulation, depletion and inversion regions. In depletion mode, the bulk Ge mobility is extracted by fitting theoretical data with experimental data, which is 143.8cm²/V-sec.

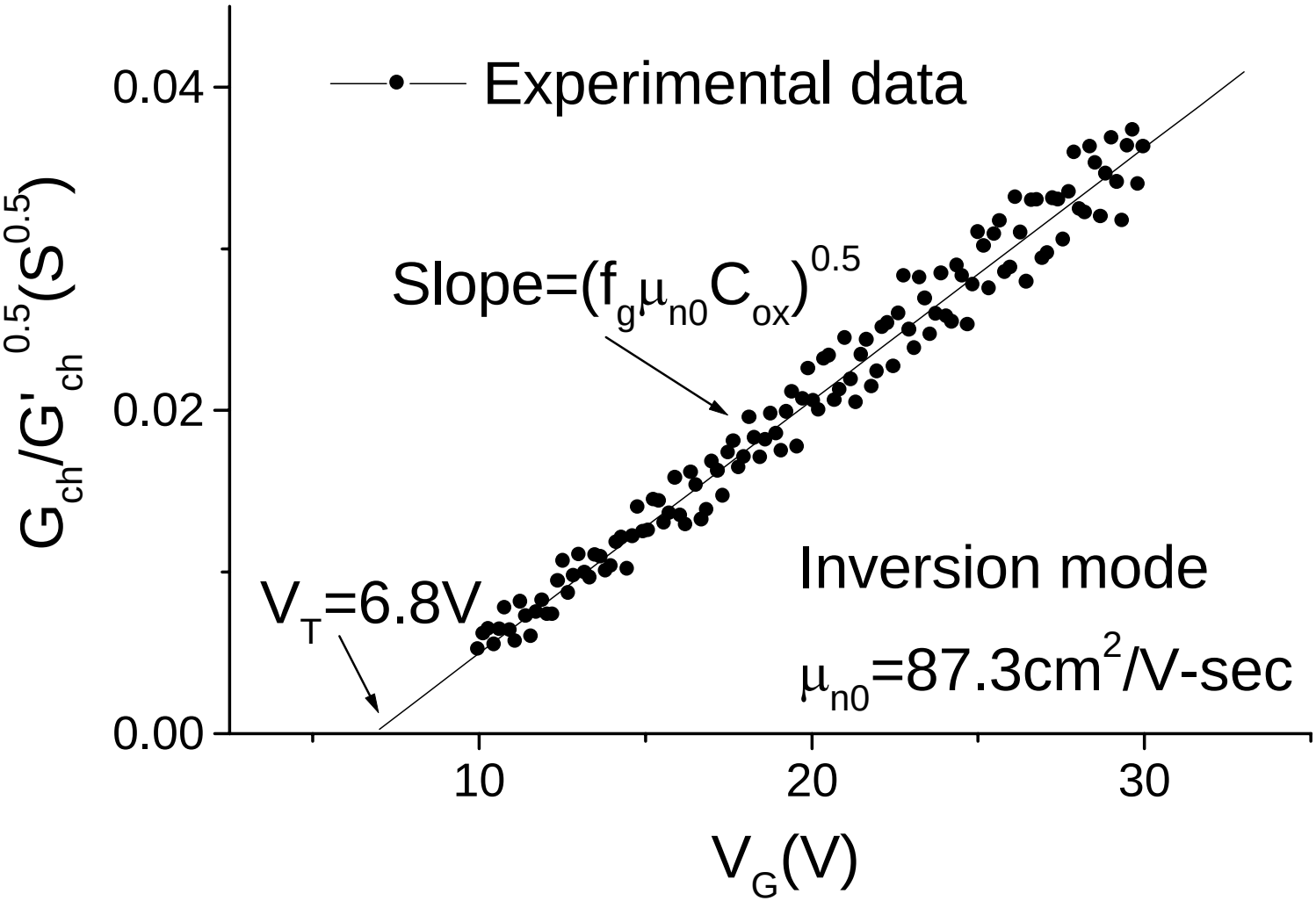
In inversion mode,
Channel conductance G_{ch} is given by:

$$G_{ch} = f_g \, \mu_{n0} \, C_{ox} \, (V_G - V_T) / [1 + \theta \, (V_G - V_T)]$$

Differentiating G_{ch}, we obtain:

$$G_{ch}^{'} = \frac{dG_{ch}}{dV_G} = \frac{f_g \mu_{n0} C_{ox}}{\left[1 + \theta (V_G - V_T)\right]^2}$$

$$\frac{G_{ch}}{G_{ch}^{' \ 0.5}} = \left(f_g \mu_{n0} C_{ox}\right)^{0.5} \left(V_G - V_T\right)$$



The extraction of the threshold voltage V_T; The low field electron mobility at interface was extracted from the slope of the fit lines, which is 87.3cm²/V-sec.

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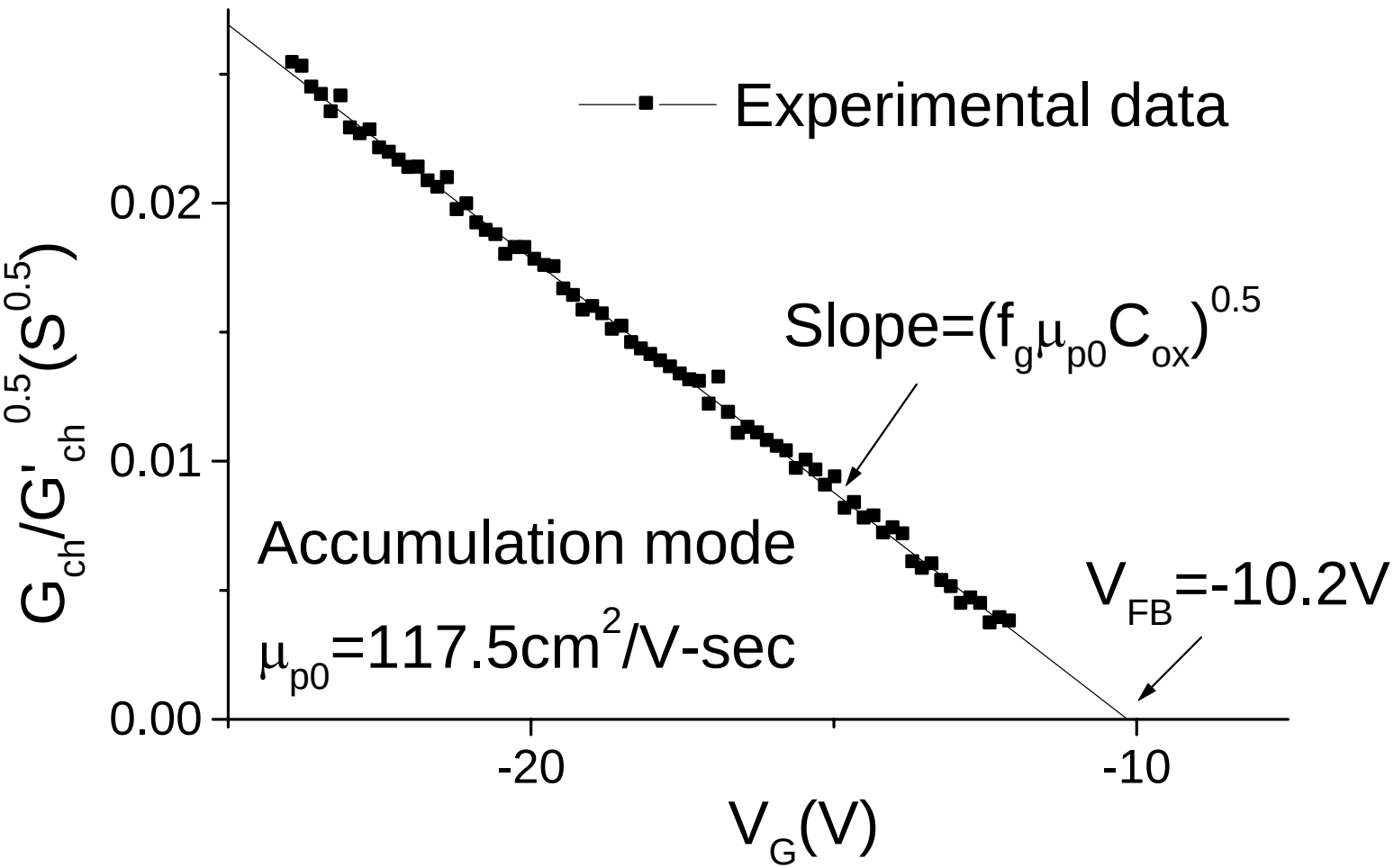
In accumulation mode:

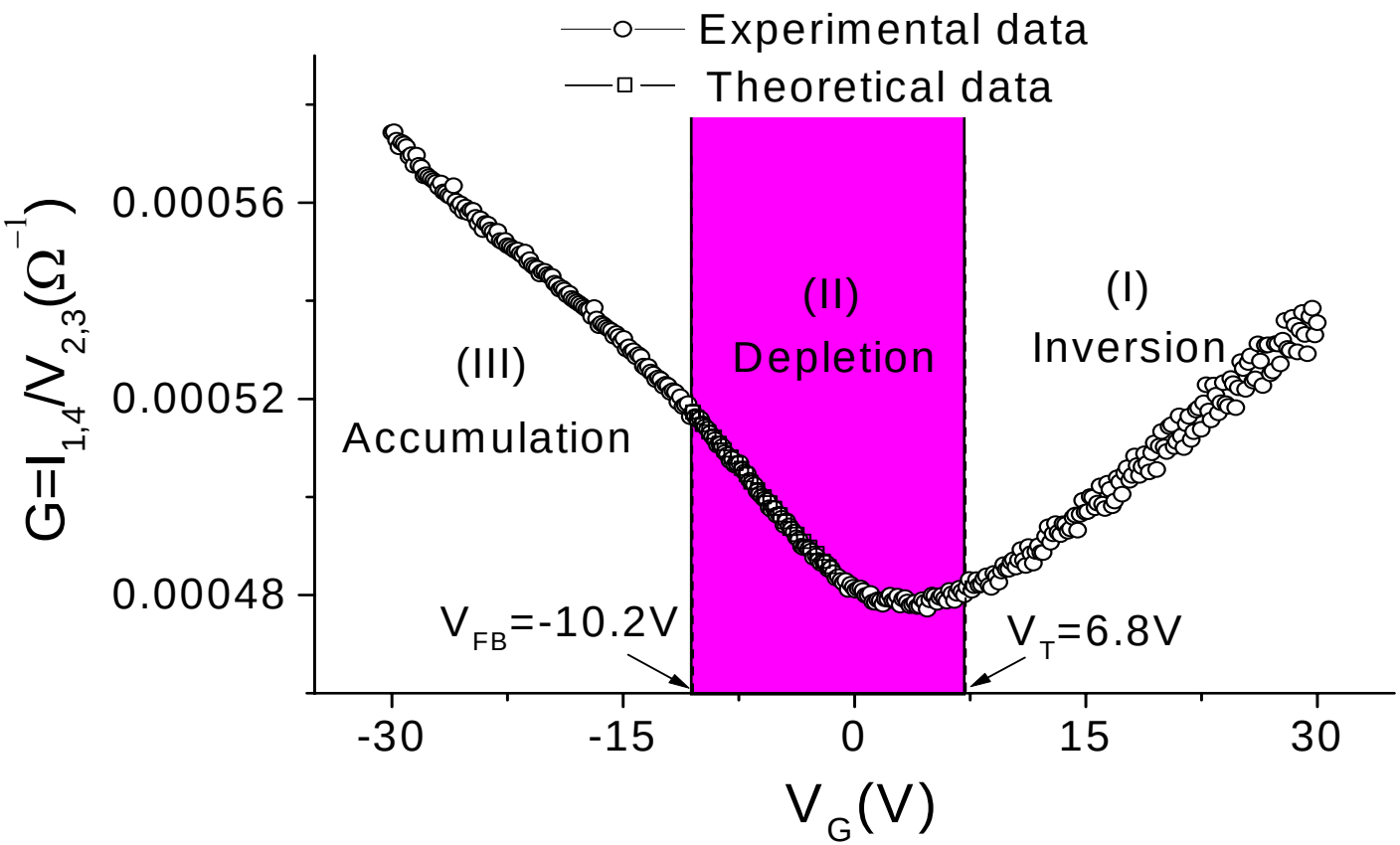
$$G_{ch}^{'} = \frac{dG_{ch}}{dV_G} = \frac{f_g \mu_{p0} C_{ox}}{\left[1+\theta'(V_G - V_{FB})\right]^2}$$

$$\frac{G_{ch}}{G_{ch}^{' \ 0.5}} = \left(f_g \mu_{p0} C_{ox}\right)^{0.5} \left(V_G - V_{FB}\right)$$



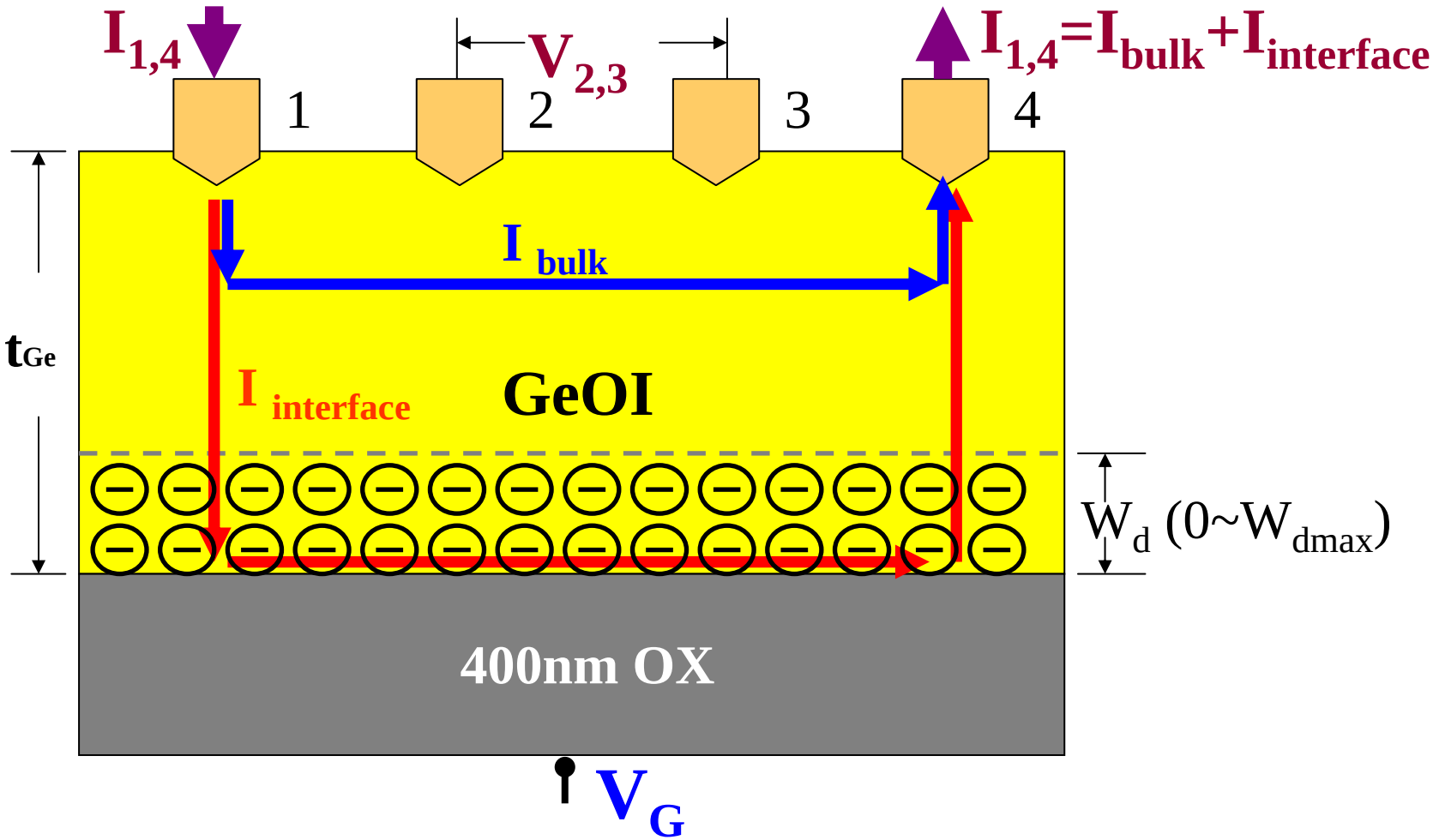
The extraction of the flatband voltage V_{FB}; The low field hole mobility at interface was extracted from the slope of the fit lines, which is 117.5cm²/V-sec.

The pseudo-MOSFET experimental data



G vs VG plot, which shows the accumulation, depletion and inversion regions. In depletion mode, the bulk Ge mobility is extracted by fitting theoretical data with experimental data, which is 143.8cm²/V-sec.

I-V of intrinsic point-probe MOSFET in partially depleted GeOI



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$I_{1,4}$ is given by:

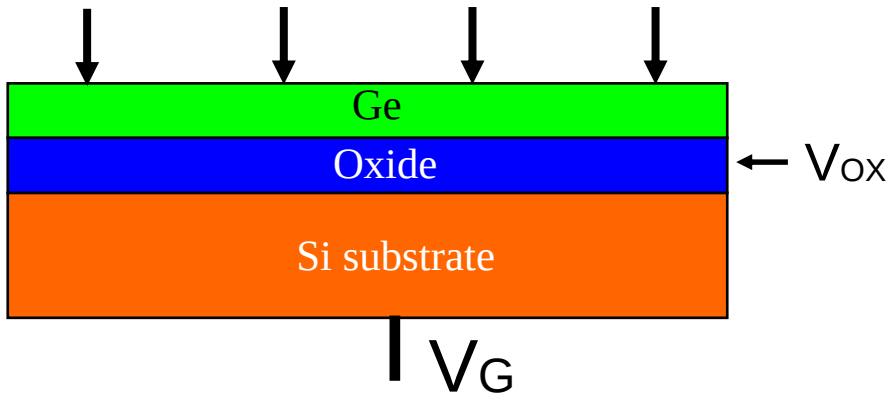
$$I_{1,4} = I_{bulk} + I_{interface}$$

In depletion mode:

$$I_{bulk} \quad >> \quad I_{interface}$$

$$I_{1,4} = I_{bulk} + I_{interface} = I_{bulk} = f_g q \mu_p (t_{Ge} - w_d) N_{Ge} V_{2,3}$$

$$G = I_{1,4}/V_{2,3} = f_g q \mu_p \left(t_{Ge} - w_d\right) N_{Ge}$$



$$w_d = \sqrt{\frac{2\varepsilon_s}{qN_{Ge}}\psi} = \sqrt{\frac{2\varepsilon_s}{qN_{Ge}}(V_G - V_{FB} - V_{ox})}$$

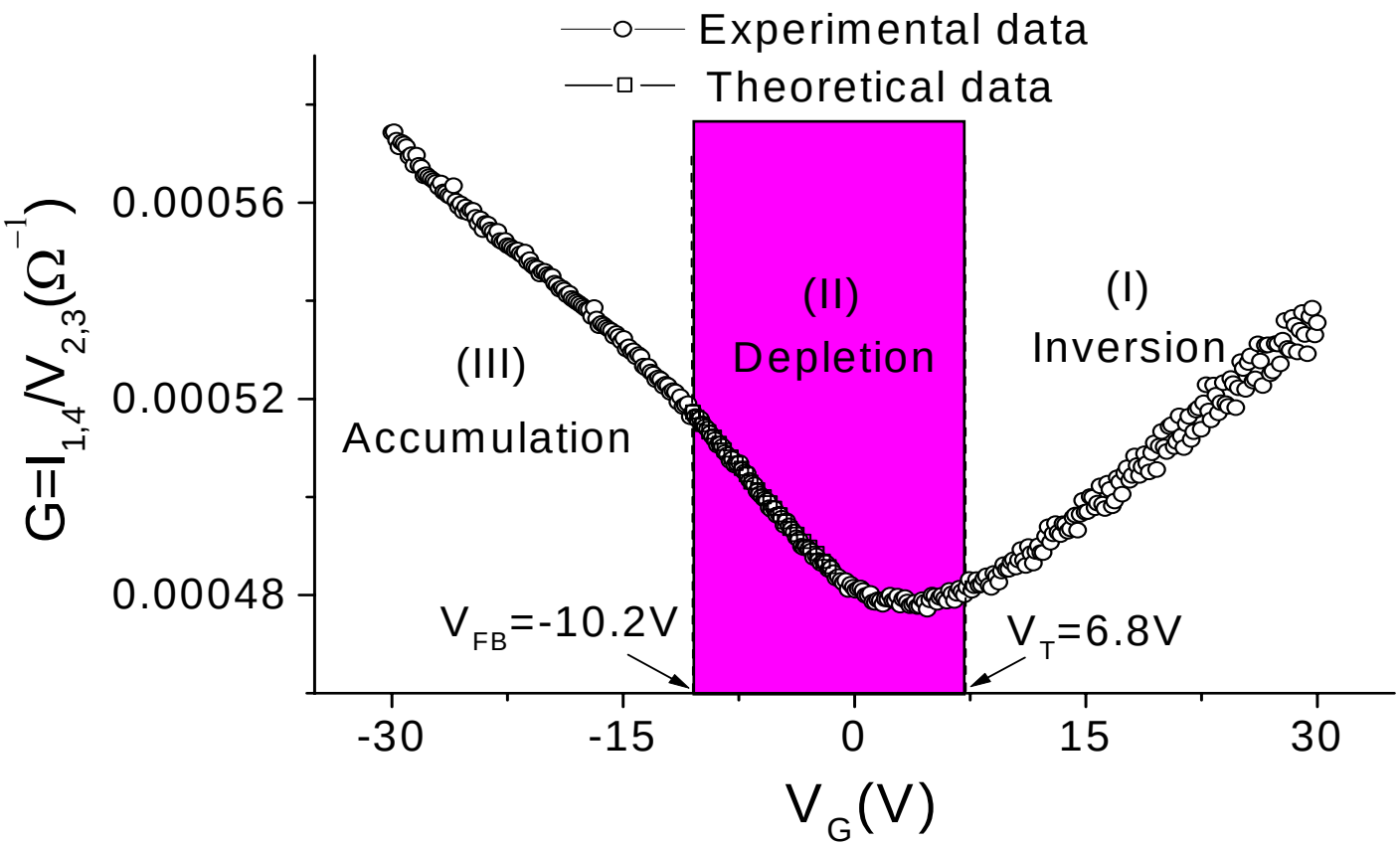
$$(A-G)^2 = BV_G + C$$

$$A = f_g q \mu_p N_{Ge} \left(t_{Ge} + \varepsilon_s / C_{ox} \right)$$

$$B = 2q \left(f_g \mu_p \right)^2 \varepsilon_s N_{Ge}$$

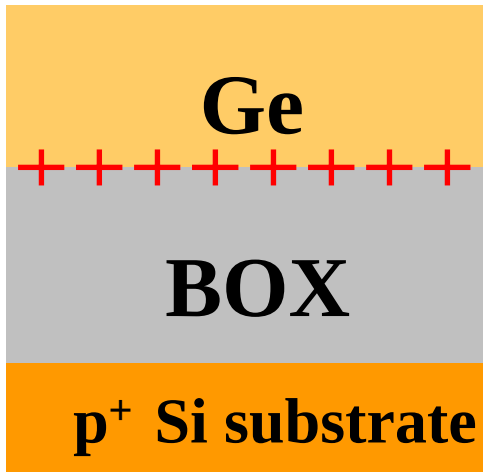
$$C = \left(f_g q \mu_p N_{Ge} \right)^2 \left[\left(\varepsilon_s / C_{ox} \right)^2 - \frac{2\varepsilon_s V_{FB}}{q N_{Ge}} \right]$$

The pseudo-MOSFET experimental data



G vs VG plot, which shows the accumulation, depletion and inversion regions. In depletion mode, the bulk Ge mobility is extracted by fitting theoretical data with experimental data, which is 143.8cm²/V-sec.

The extraction of interface fixed charge density, Q_f

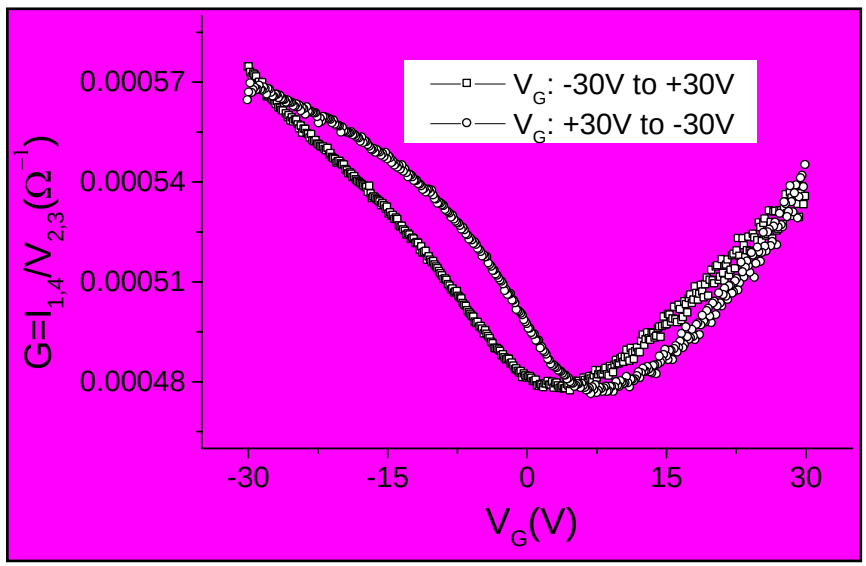


Q_f

$$V_{FB} = \Phi_{Ge\text{-}Si} - Q_f / C_{ox}$$

The extracted V_{FB} by pseudo-MOSFET is used to obtain Q_f

The extraction of interface trap density, Q_{it}



Hysteresis behavior is observed when V_G is swept along opposite directions. This is attributed to the interface traps between Ge and the buried oxide. The shift of V_T is used to obtain interface trap density O_{it} .

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Current GeOI Summary

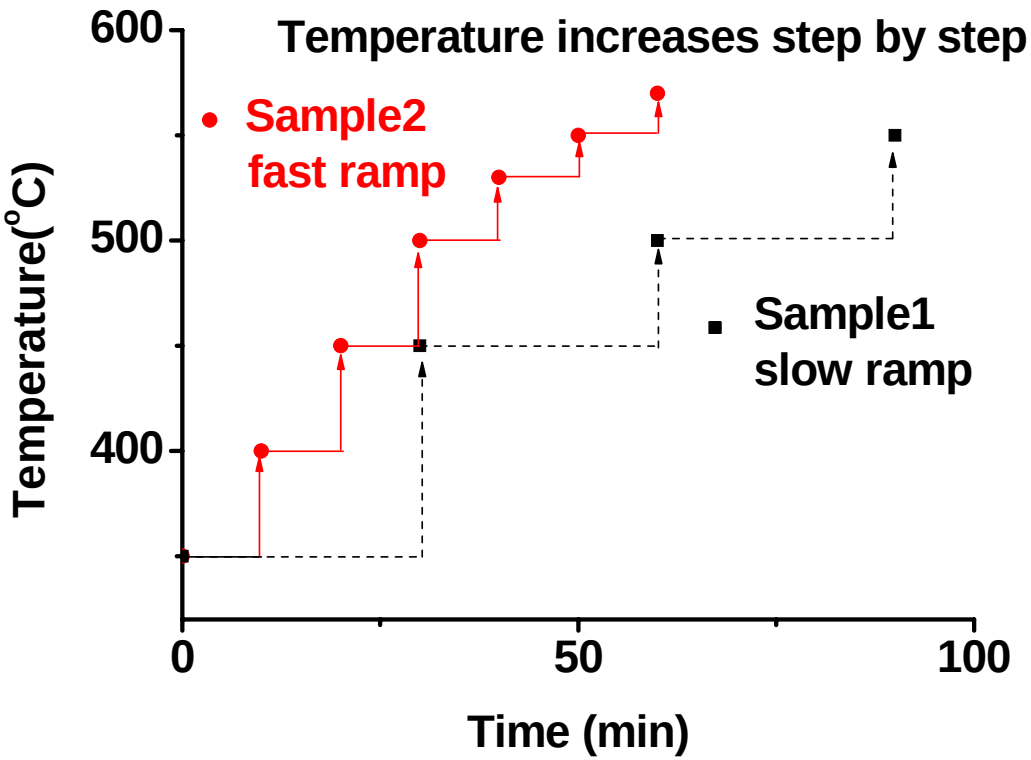
Interface fixed charge density, Q_f	~10^{11}q/cm^2
Interface trap density,Q_{it}	~10^{11}q/cm^2
Interface hole mobility, μ_{p0}	117.5 cm^2/V-sec
Interface electron mobility, μ_{n0}	87.3 cm^2/V-sec
Bulk hole mobility, μ_p	143.8 cm^2/V-sec

Part II Our research about GeOI

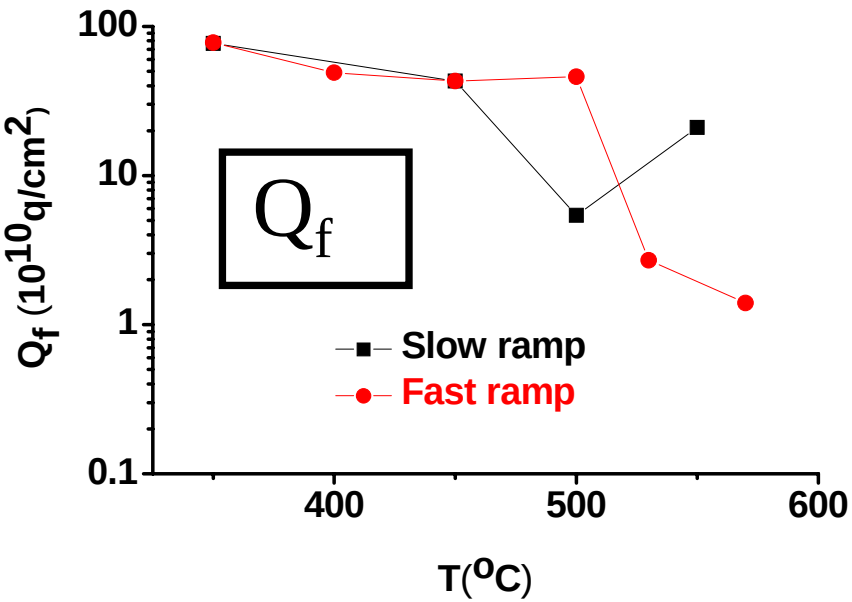
- Bulk and Epi Ge wafer are transferred on substrate
- A new method was presented to extract mobility
- Mobility and interface trap density are improved

The condition of forming gas annealing

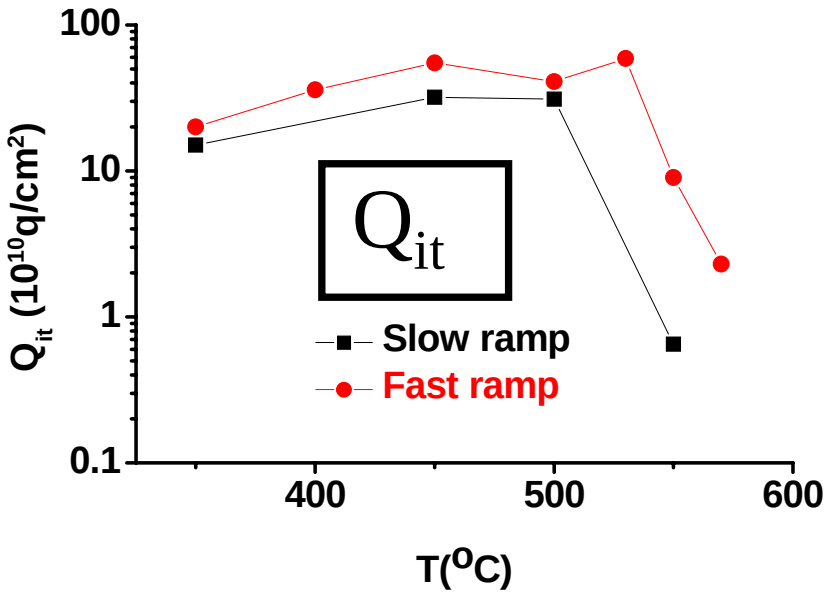
- Gas ratio : 10%H_2, 90%N_2
- Gas flow : 8L/min
- Temperature : 400℃~600 ℃
- Time : 10min or 30min at each temperature point



Interface trap (Q_{it}) and Interface charge(Q_f) improved through forming gas annealing



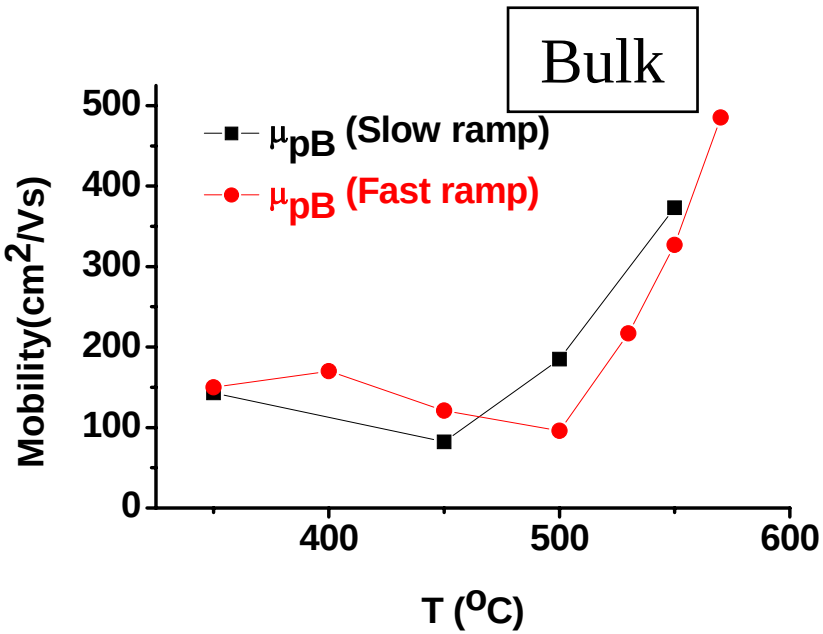
(A)



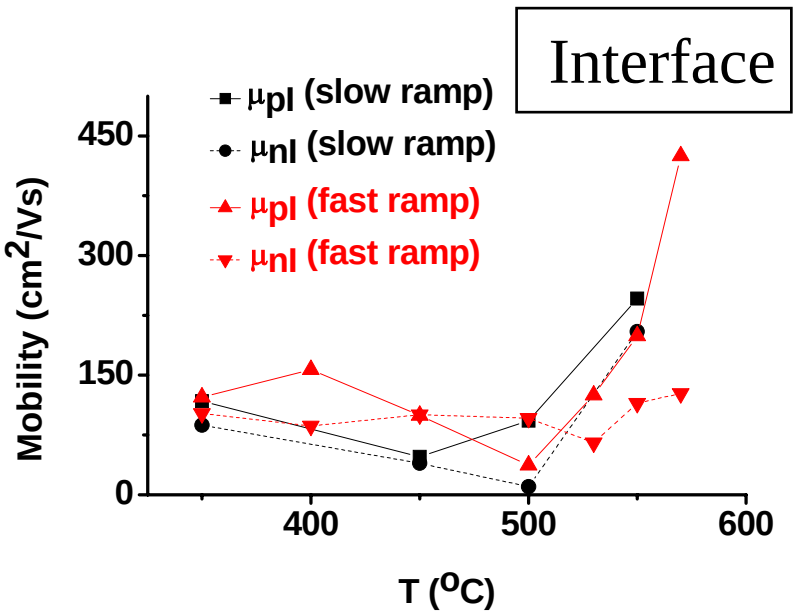
(B)

- **Both interface trap density Q_{it} and interface fixed charge density Q_f decrease to 10^{10}q/cm^2 after forming gas annealing.**

Carrier mobility improved through forming gas annealing



(A)



(B)

- **3X improvement of bulk hole mobility with fast ramp**
- **3X improvement of interface hole mobility with fast ramp**
- **2X improvement of interface electron mobility with slow ramp**

Seminar

In Progress

- Prototype GeOI MOSFET performance with ALD high-K dielectric (with Prof. J. Chang, UCLA)
- Demonstrate Strained GeOI layer transfer

Conclusion

- GeOI is a potential next-generation substrate
- A new pseudo-MOSFET methodology is presented to extract bulk mobility of GeOI
- Mobility and Interface trap is improved by forming gas annealing

Thanks!