Amorphous silicon thin-film transistors for flexible electronics

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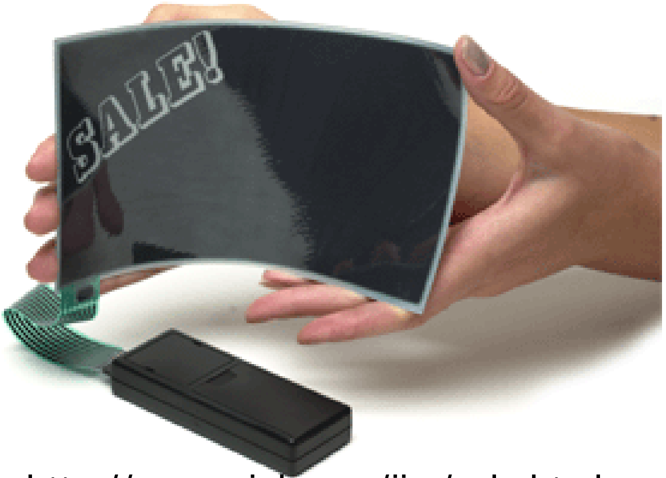
Berkeley, April 13, 2007

Flexible displays

Lucent, E-Ink

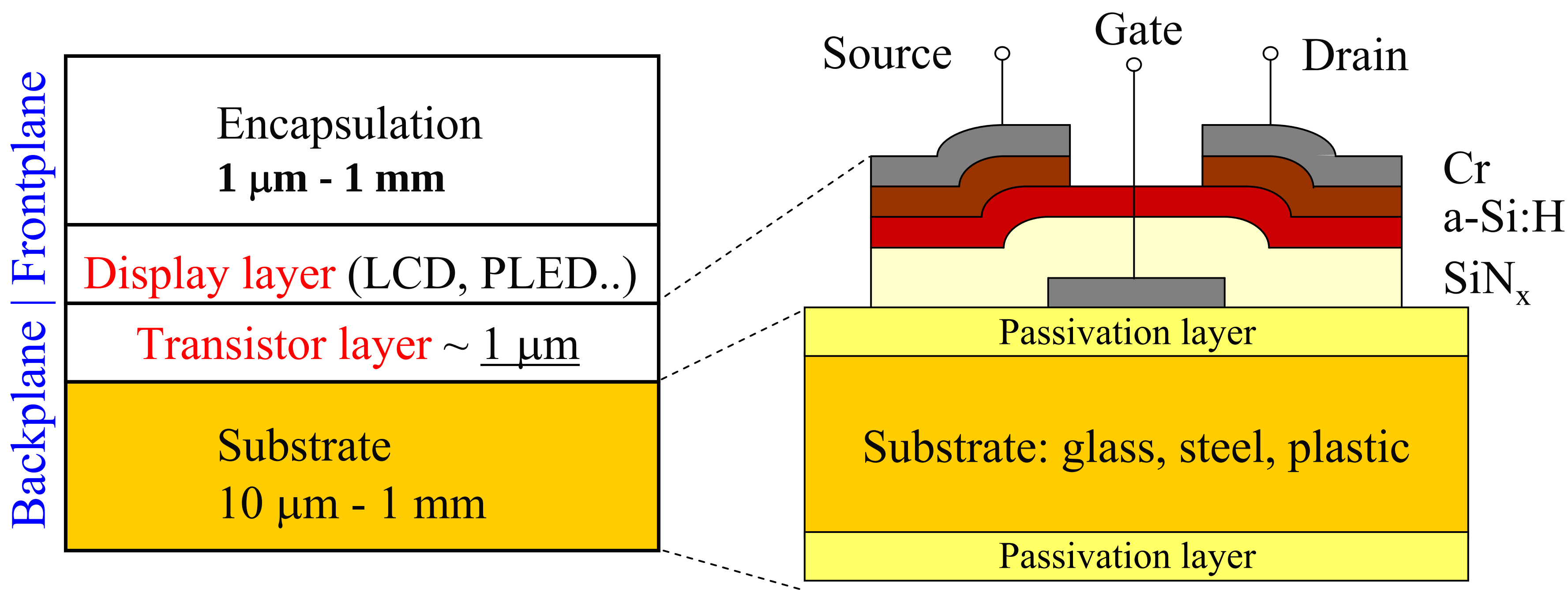


http://www.eink.com/iim/sale.html

Transistor "backplane" and display "frontplane"

Schematic cross section of a display

Amorphous silicon thin film transistor generic backplane



- TFT backplane is generic for all flat panel technologies
- Add display layer on top

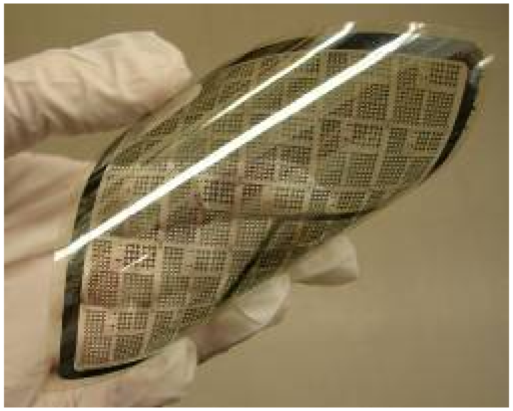
Gleskova H., Wagner S., IEEE Electron Device Letters **20** (1999), pp. 473-475.

Outline

- Metal versus plastic foil substrate
- a-Si:H TFT deposition temperature
- Overlay alignment

Steel versus plastic

Cheng I-C. et al., IEEE EDL **27** (2006) 166.



polymer foil substrate

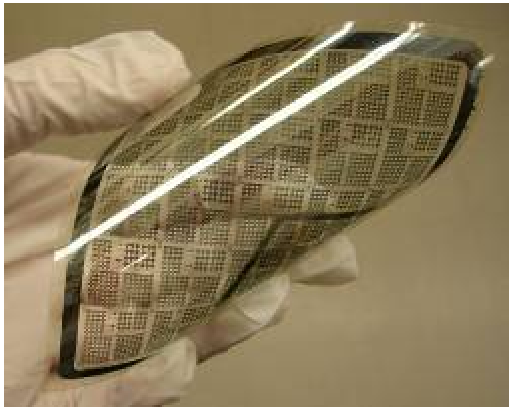
Kattamis A.Z., Princeton University

steel foil substrate

< 280°C	**process temperature**	up to ~1000°C
low	**dimensional stability**	> 10 times higher
some	**visually clear**	no
yes	**permeable to O_2 or H_2O**	no
moderate	**surface roughness**	rough
some	**inert to chemicals**	yes
no	**electrical conductor**	yes

Steel versus plastic

Cheng I-C. et al., IEEE EDL **27** (2006) 166.



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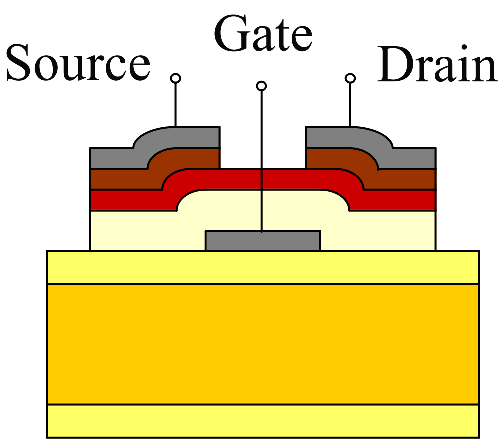
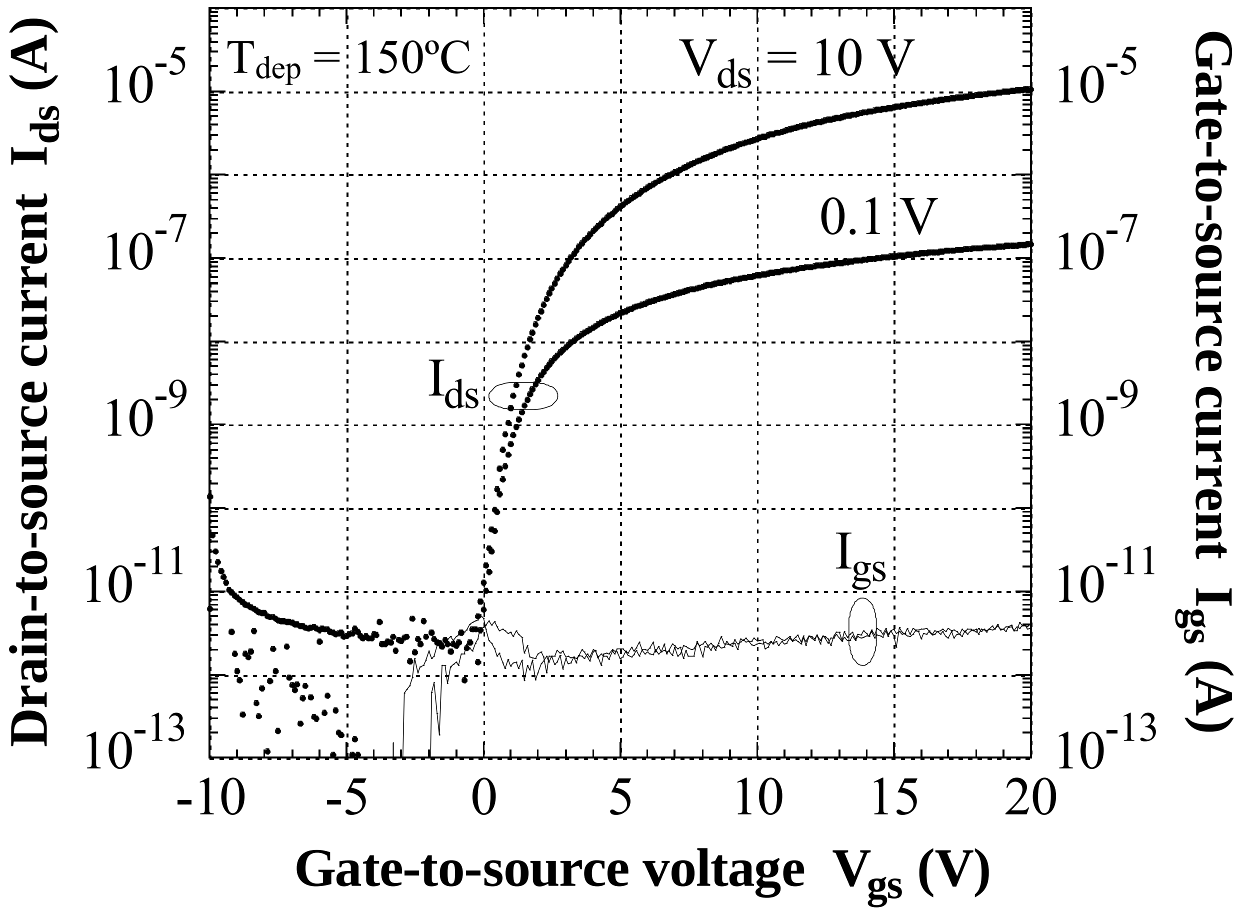
a-Si:H TFTs made at 150°C on Kapton



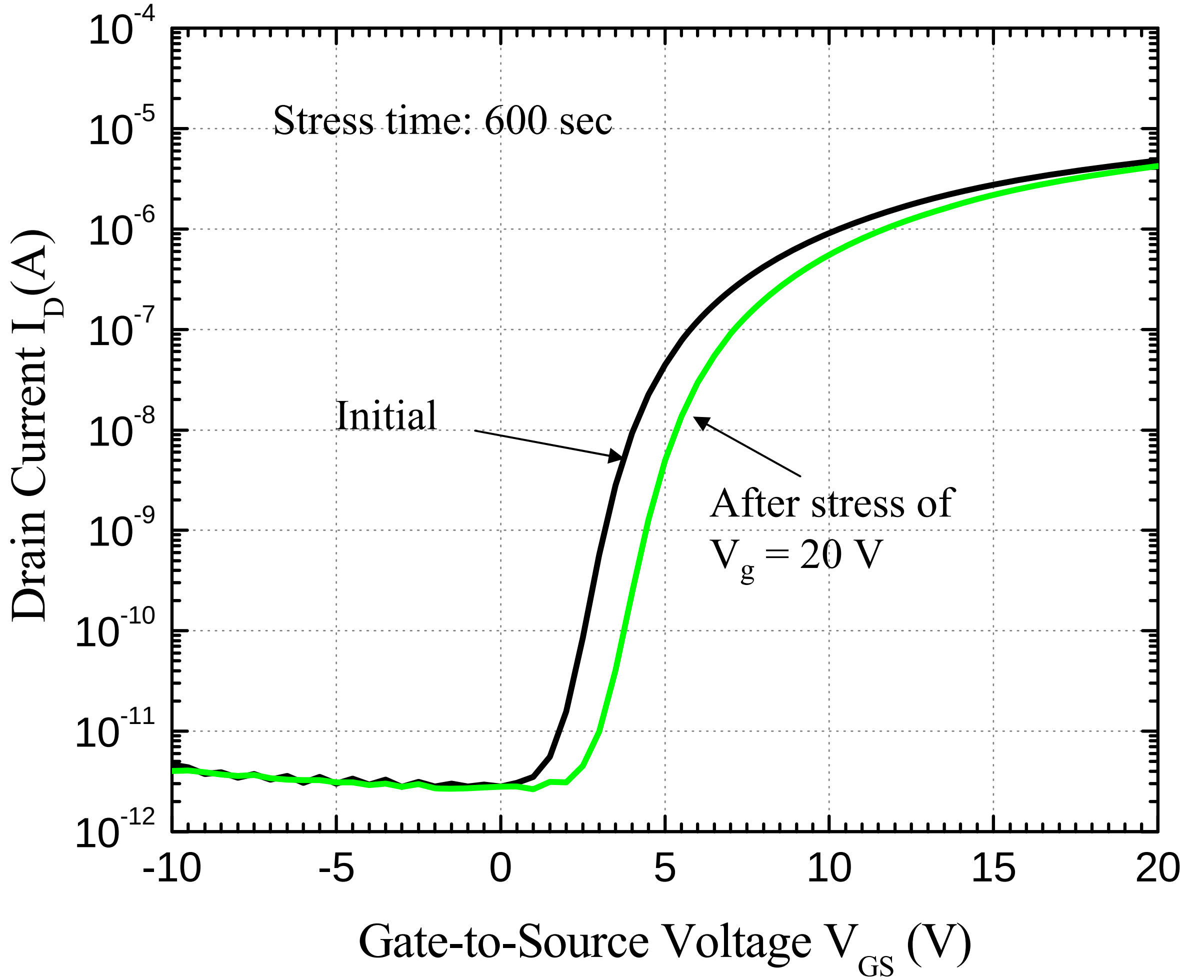


$I_{on}/I_{off} > 10^7$, $\mu_{lin} \sim 0.45$ cm^2/Vs, $V_T \sim 2$ V

Acceptable TFT performance, but …

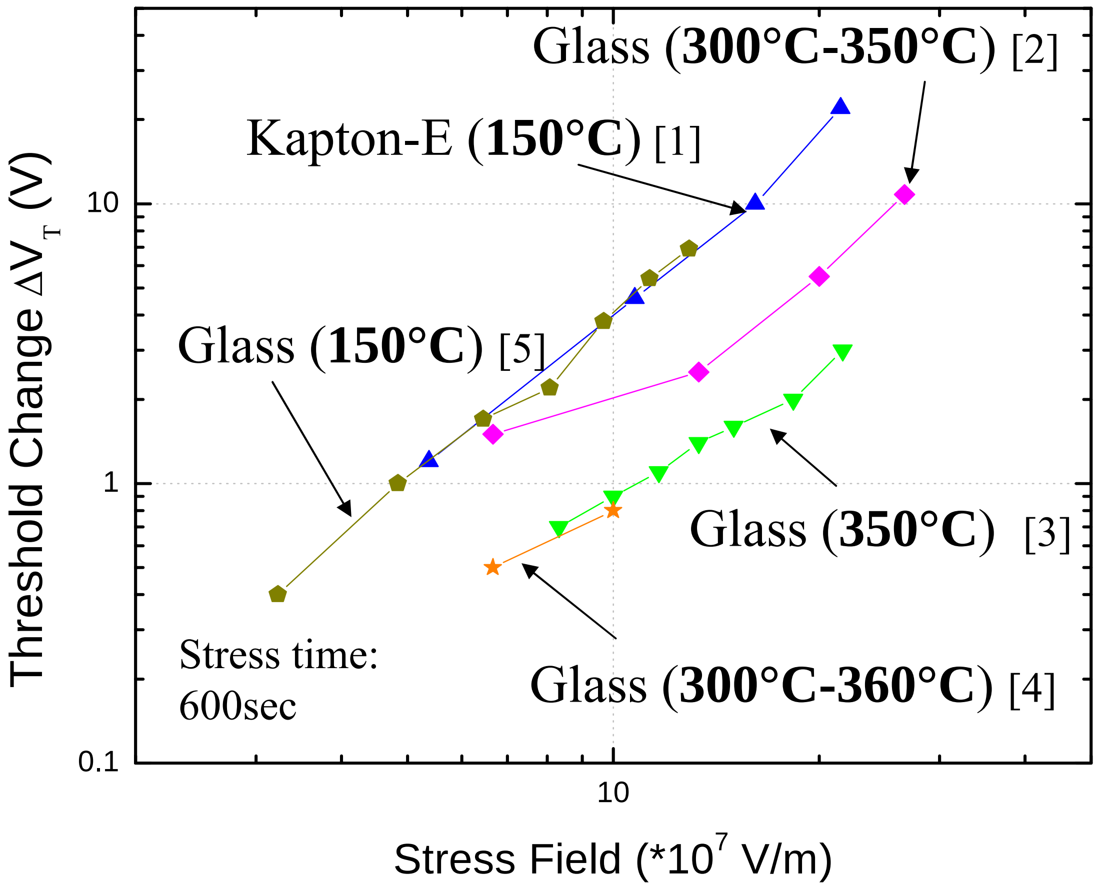
Gleskova H. et al., J. Electrochem. Society **148** (2001), pp. G370-G374.
Gleskova H. et al., J. Appl. Phys. **92** (2002), pp. 6224-6229.

Bias-stress instability of a-Si:H TFTs



Long K. et al., IEEE Electron Device Lett. **27** (2006), pp. 111-113.

a-Si TFT stability rises with process temperature



[1] Gleskova, IEEE TED, 2001

[2] Cheng, IEEE Proc. Solid-State and Integrated Circuit Tech., 1998

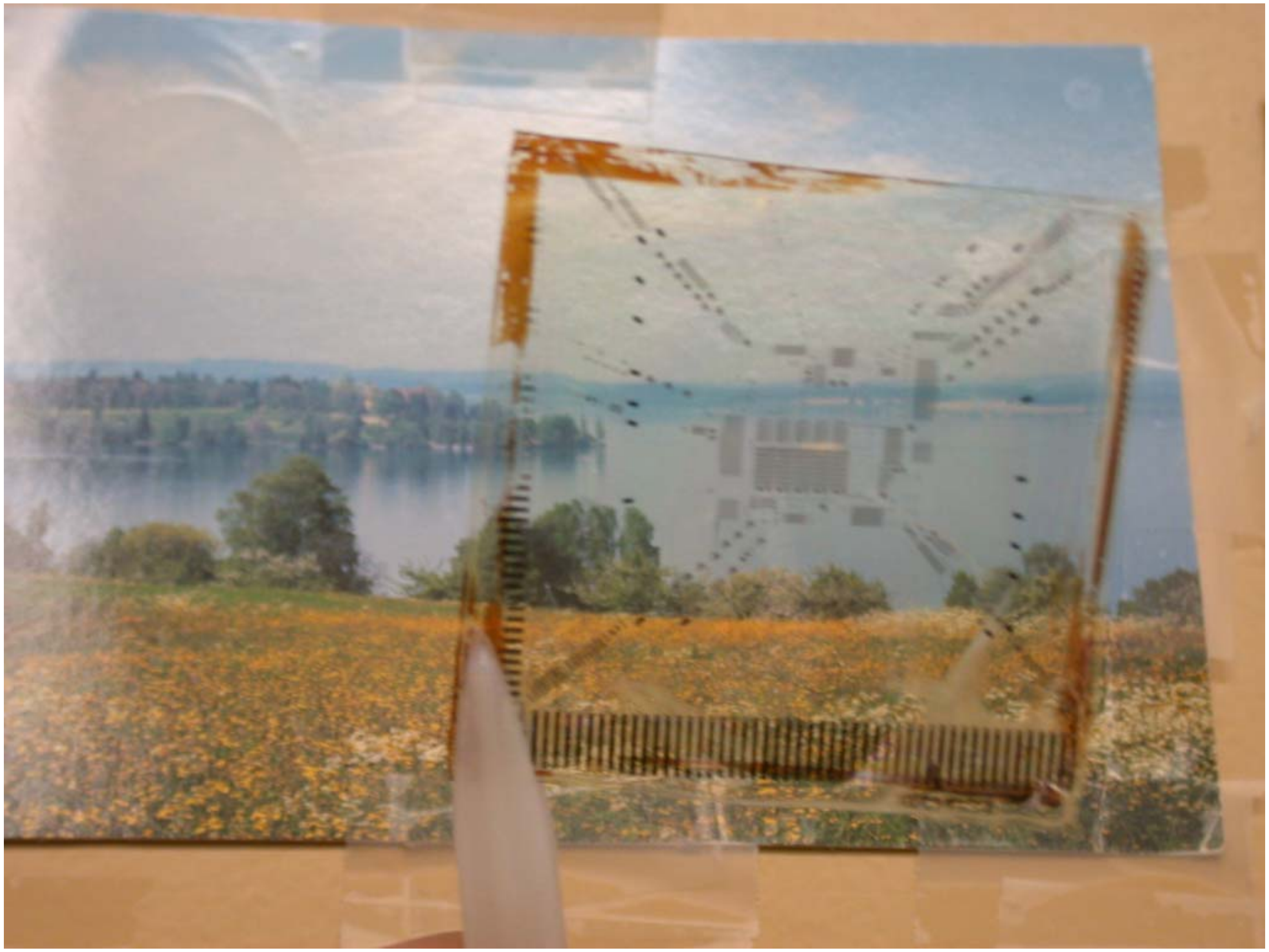
[3] Kanicki, APL, 1993

[4] Tsukada, JAP, 1991

[5] Long, Princeton Univ.

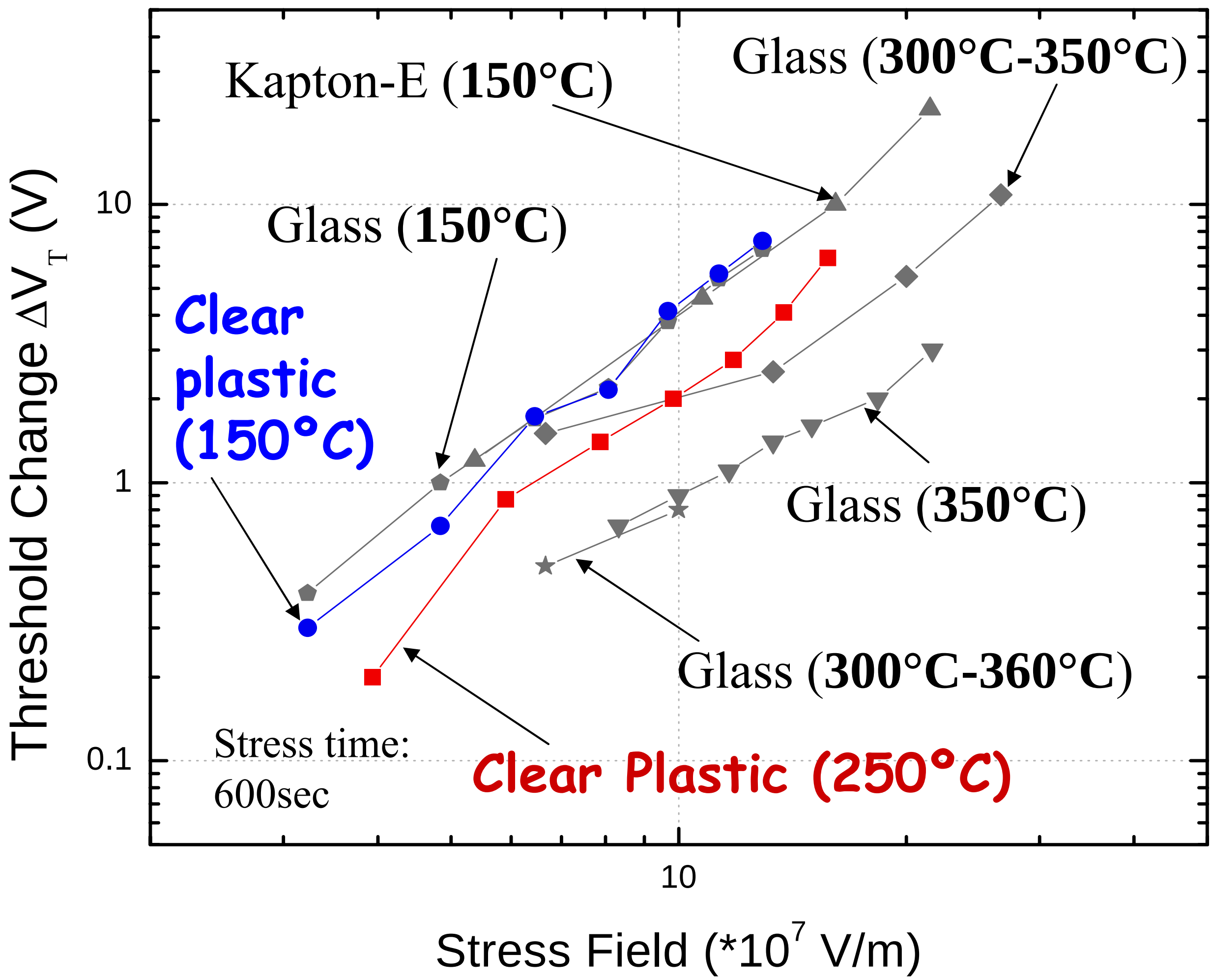
⇒ Must make a-Si:H TFTs at high process temperature

a-Si:H TFTs made on clear plastic at 280°C



Cherenack K., Princeton University

a-Si:H TFT stability on clear plastic substrates

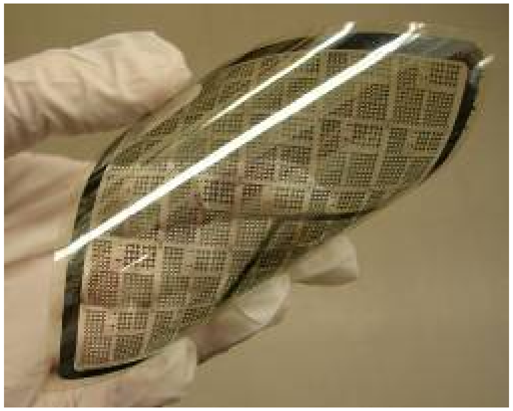


ΔV_T depends only on process T, not on substrate material

Long K. et al., IEEE Electron Device Lett. **27** (2006), pp. 111-113.

Steel versus plastic

Cheng I-C. et al., IEEE EDL **27** (2006) 166.



polymer foil substrate

Kattamis A.Z., Princeton University

steel foil substrate

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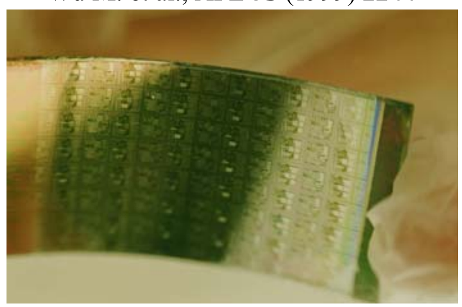
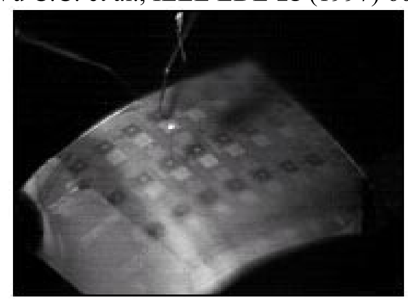
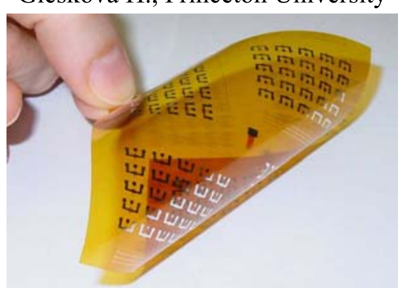
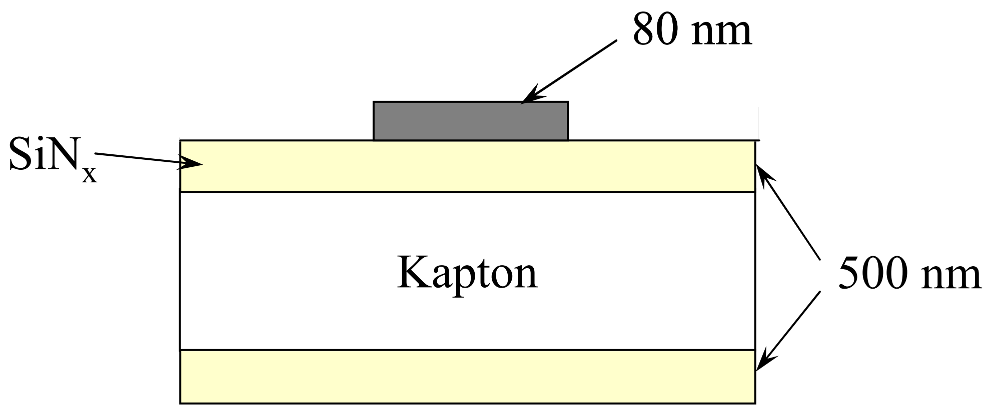
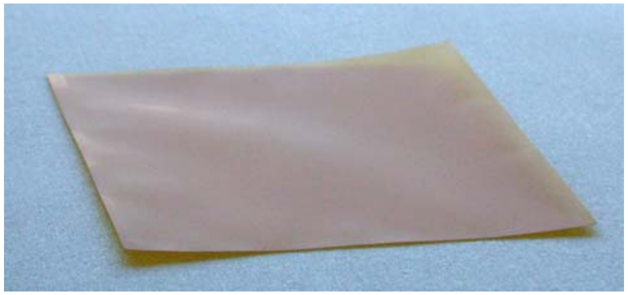
Substrate stiffness affects dimensional stability

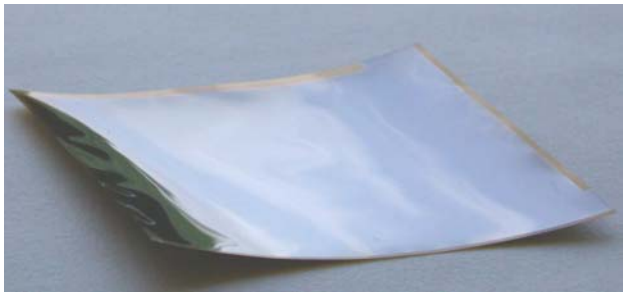
$Y_s \cdot d_s$ versus $Y_f \cdot d_f$		thin film (small d_f)	
		stiff (large Y_f)	compliant (small Y_f)
thick substrate (large d_s)	stiff (large Y_s)	poly-Si TFT / steel substrate Wu M. et al., APL **75** (1999) 2244  $Y_s \cdot d_s >> Y_f \cdot d_f$	OLED / steel substrate Wu C.C. et al., IEEE EDL **18** (1997) 609  $Y_s \cdot d_s >> Y_f \cdot d_f$
	compliant (small Y_s)	a-Si TFT / polymer substrate Gleskova H., Princeton University  $Y_s \cdot d_s \approx Y_f \cdot d_f$	OTFT / polymer substrate Jackson T., Penn State Univ.  $Y_s \cdot d_s >> Y_f \cdot d_f$

a-Si:H TFT process

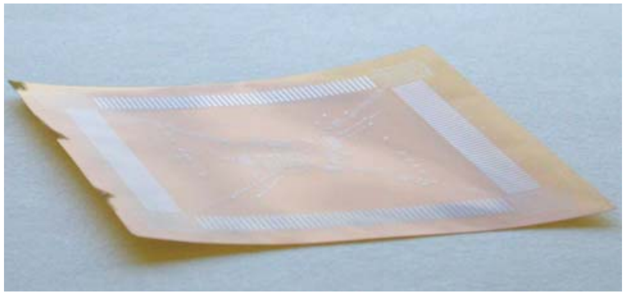




1. Front SiN_x passivation
2. Back SiN_x passivation



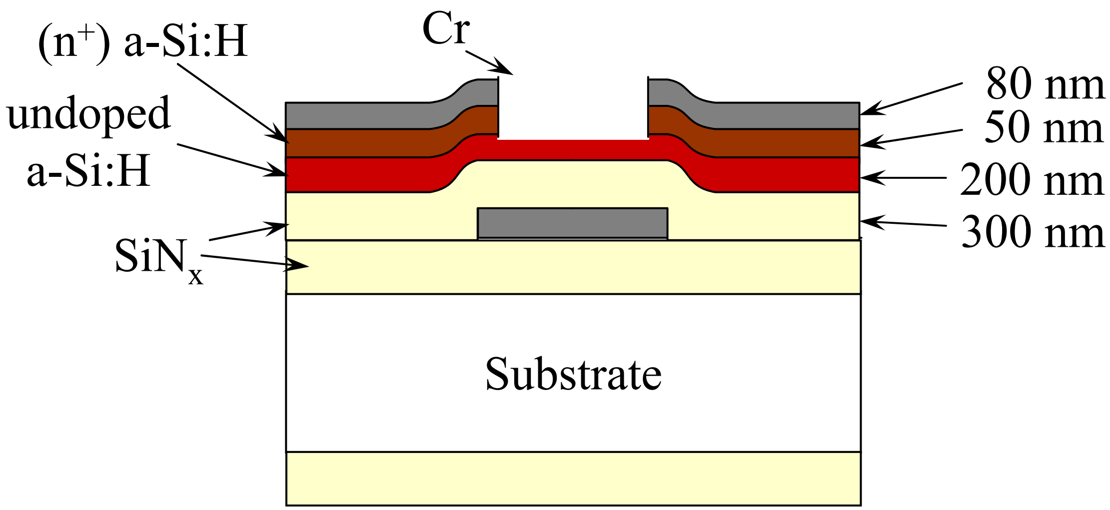
3. Cr gate metal deposition

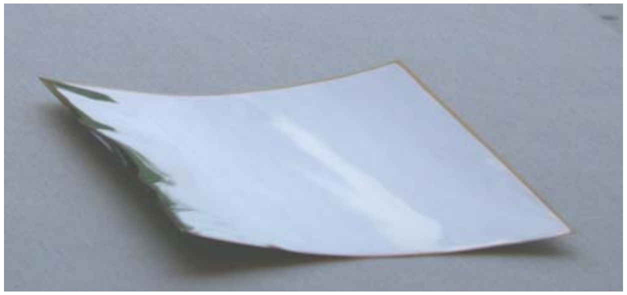


4. Cr gate patterning - **mask 1**

Cheng I-C. et al., J. SID **13** (2005), pp. 563-568.

a-Si:H TFT process – cont.





5. PECVD TFT stack: **5 W** SiN_x
(i) a-Si:H
(n^+) a-Si:H
6. Cr S/D deposition

↓

7. S/D patterning – **mask 2**

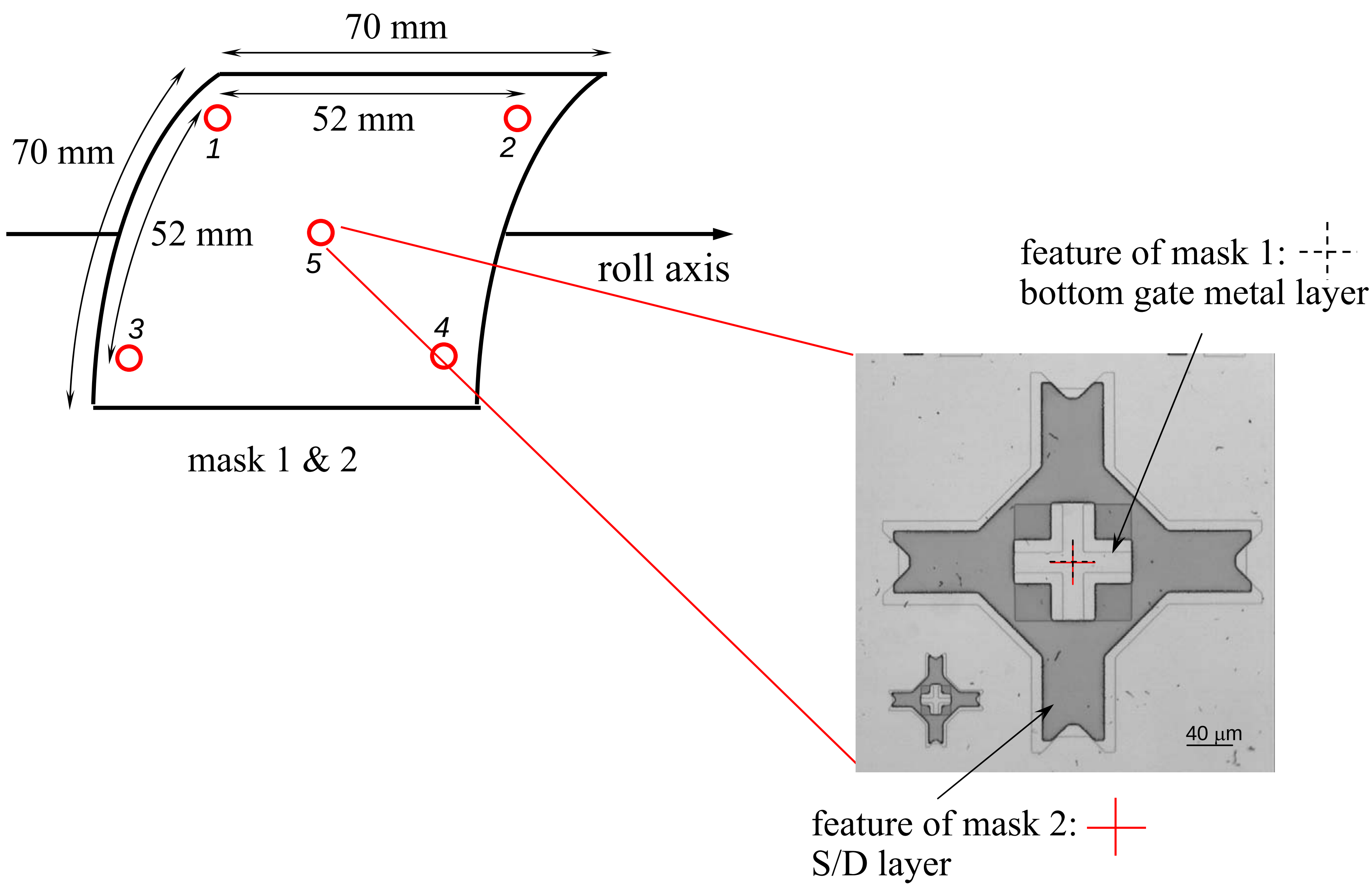
5. PECVD TFT stack: **12 W** SiN_x
(i) a-Si:H
(n^+) a-Si:H
6. Cr S/D deposition

↓

7. S/D patterning – **mask 2**

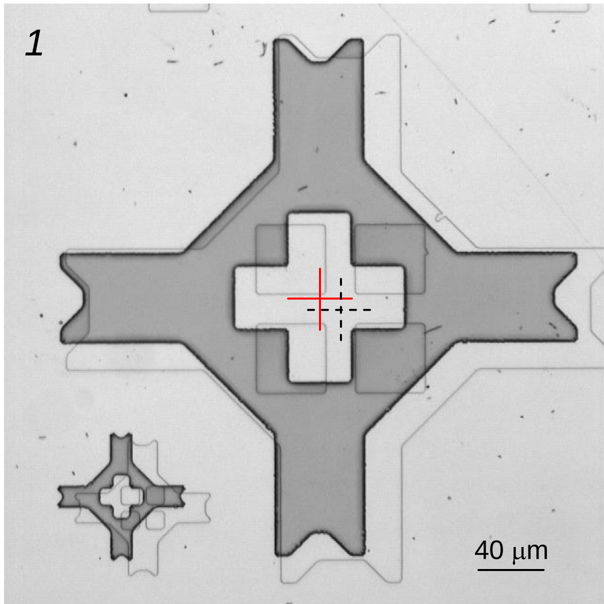
Cheng I-C. et al., J. SID **13** (2005), pp. 563-568.

Location of alignment marks



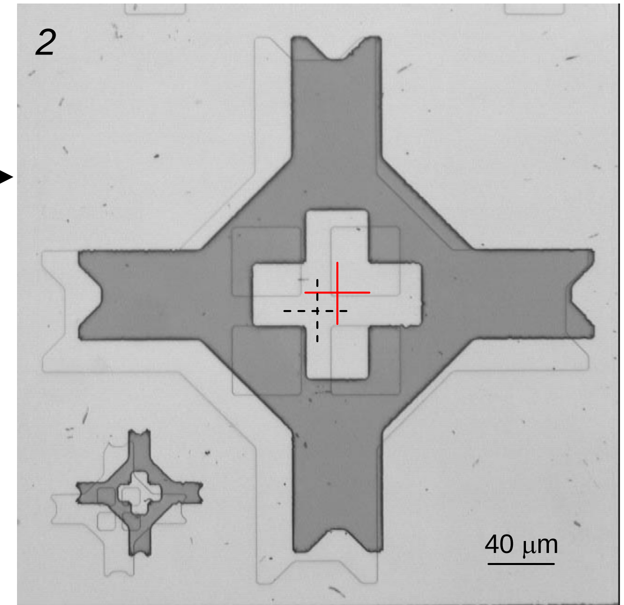
Cheng I-C. et al., J. SID **13** (2005), pp. 563-568.

5W gate SiN_x

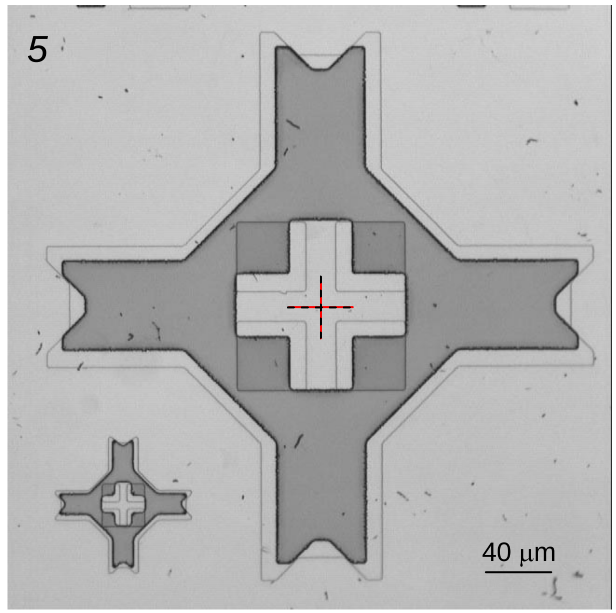


~ 52 mm

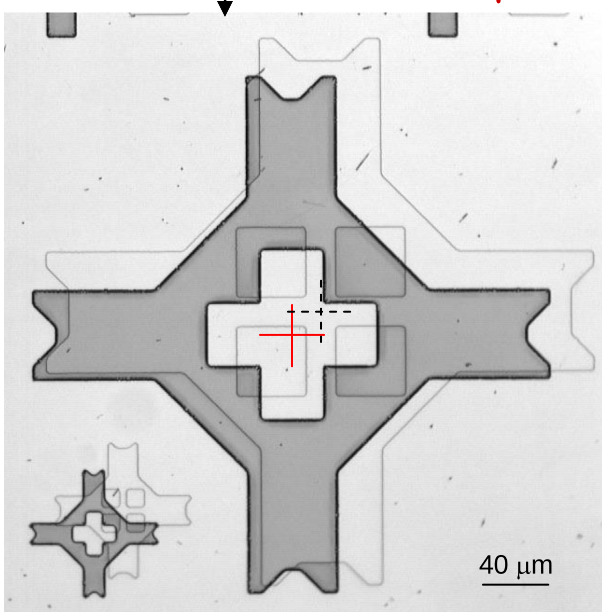
shrinkage ~ 30 µm



~ 52 mm shrink. ~ 25 µm

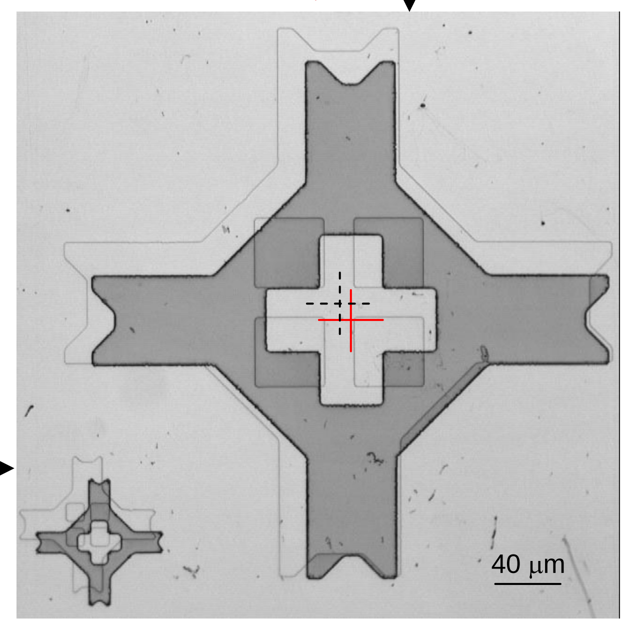


shrink. ~ 20 µm ~ 52 mm



shrinkage ~ 28 µm

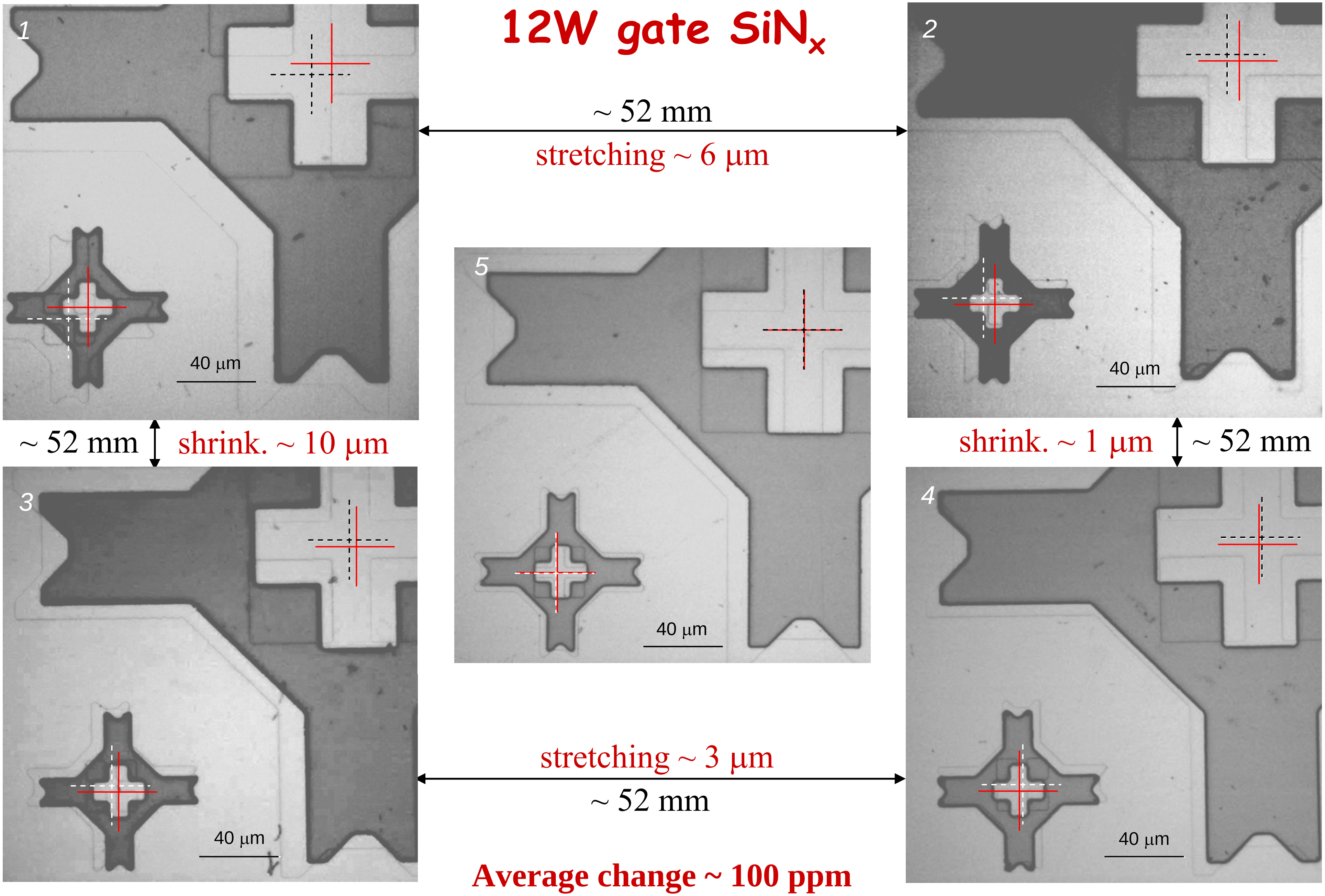
~ 52 mm



Average shrinkage ~ 500 ppm

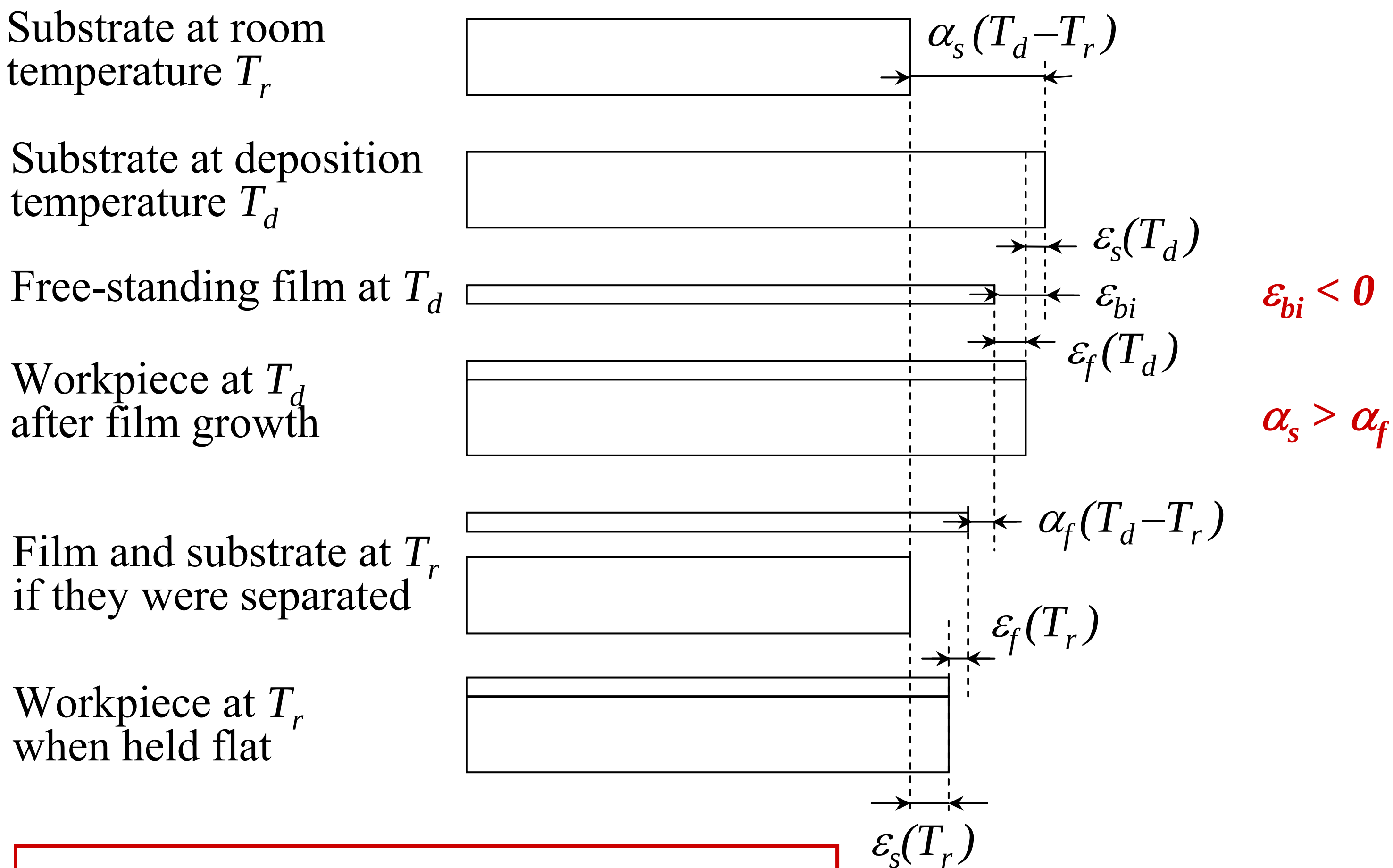
Cheng I-C. et al., J. SID **13** (2005), pp. 563-568.

12W gate SiN_x



Cheng I-C. et al., J. SID **13** (2005), pp. 563-568.

Film grown on foil substrate at elevated temperature



$$\boxed{\varepsilon_s(T_r) = \frac{\left[(\alpha_f - \alpha_s)\cdot(T_r - T_d) + \varepsilon_{bi}\right]}{1 + \frac{Y_s d_s}{Y_f d_f}}}$$

$$\nu_f = \nu_s$$

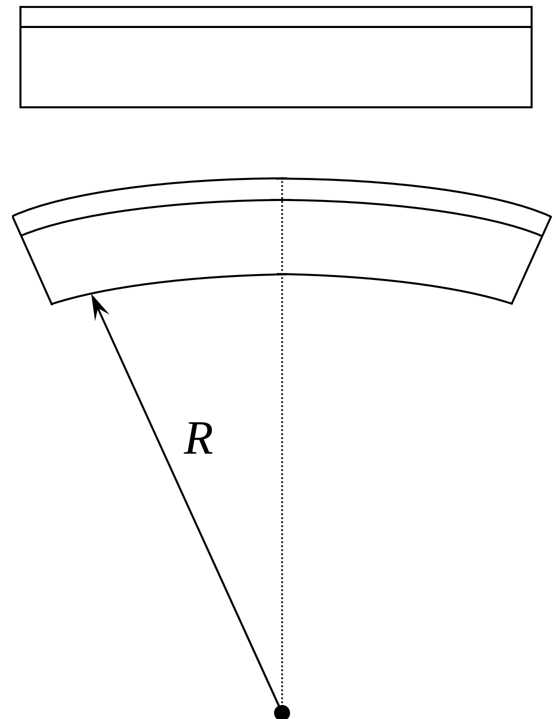
Gleskova H. et al., Appl. Phys. Lett. **88** (2006), 011905.

Gleskova H. et al., *in* Flexible Electronics: Materials and Applications, Eds. Wong W.S., Salleo A., Springer-Verlag – to be published.

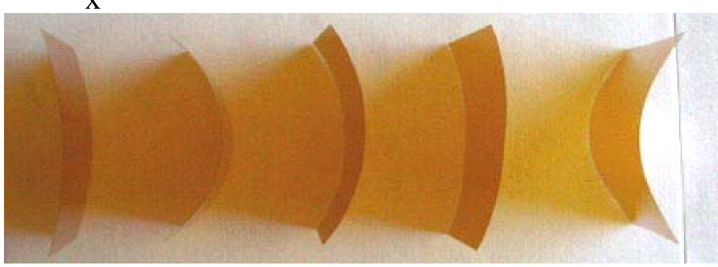
Film release from the substrate holder

Workpiece at T_r
when held flat

Workpiece at T_r
when released from
the substrate holder



SiN_x



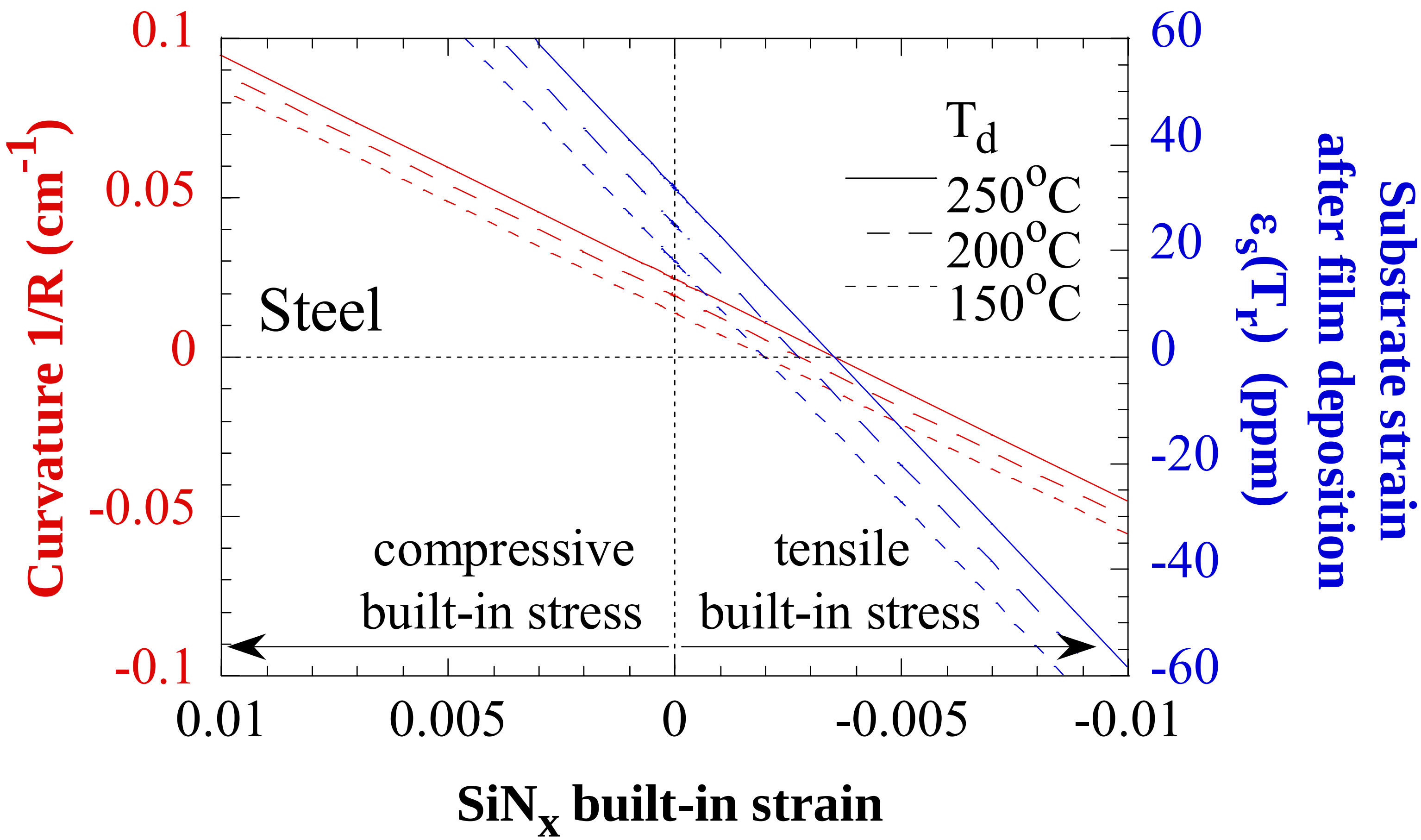
Bare 8 19 24 40 mW/cm^2

$$R = \frac{d_s}{6\frac{Y_f d_f}{Y_s d_s}(1+\nu)\left[\left(\alpha_f - \alpha_s\right)\cdot\left(T_r - T_d\right)+\varepsilon_{bi}\right]} \cdot \frac{\left(1-\frac{Y_f d_f^2}{Y_s d_s^2}\right)^2 + 4\frac{Y_f d_f}{Y_s d_s}\left(1+\frac{d_f}{d_s}\right)^2}{\left(1+\frac{d_f}{d_s}\right)}$$

Cheng I-C. et al., J. SID **13** (2005), pp. 563-568.

Suo Z. et al., Appl. Phys. Lett. **74** (1999), pp. 1177-1179.

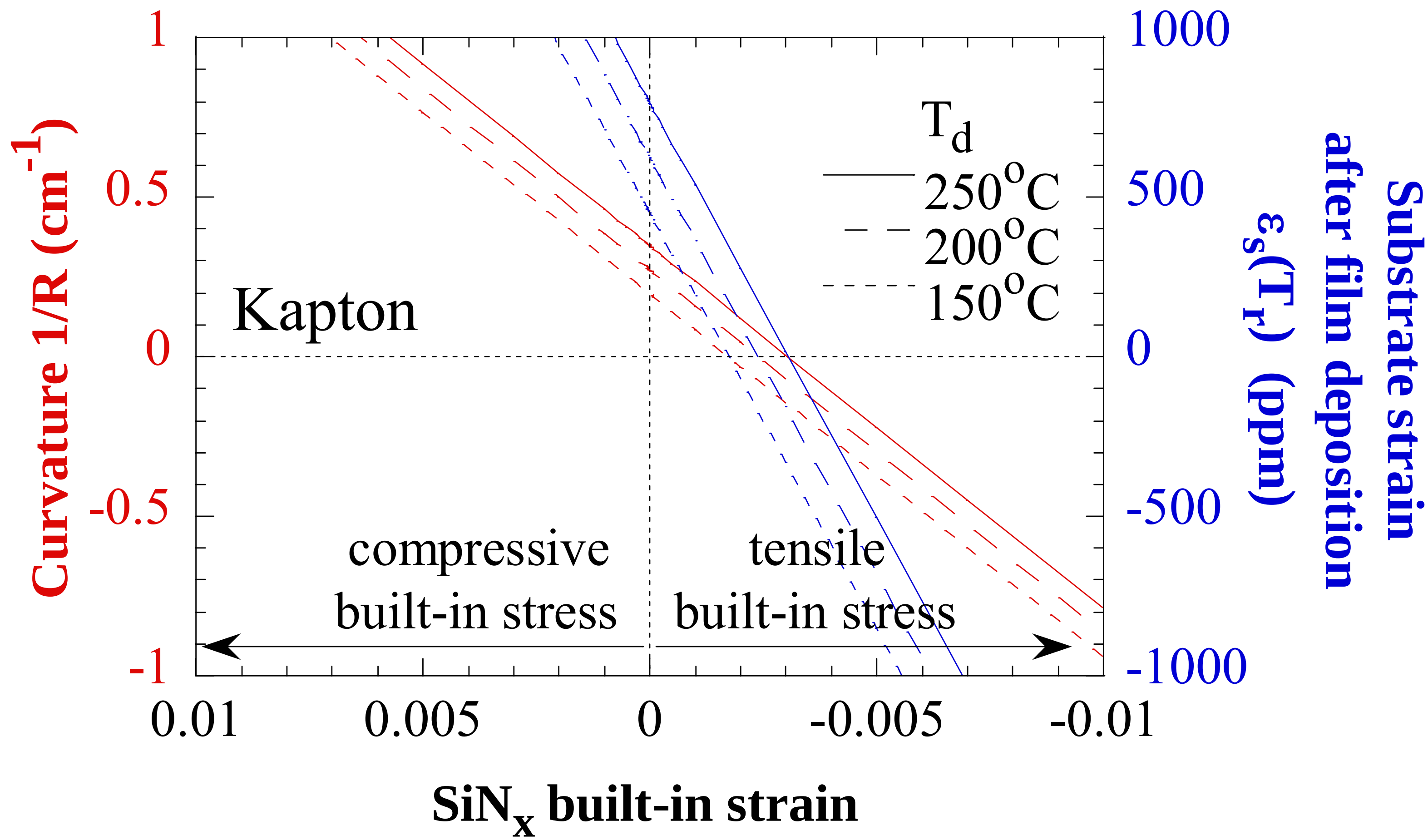
Steel foil



A rigid substrate foil is not changed much by CTE mismatch
Possible to maintain reasonable overlay accuracy

Gleskova H. et al., *in* Flexible Electronics: Materials and Applications, Eds. Wong W.S., Salleo A., Springer-Verlag – to be published.

Kapton foil



Stress built into the SiN_x can compensate thermal mismatch and eliminate curvature and misalignment

Gleskova H. et al., *in* Flexible Electronics: Materials and Applications, Eds. Wong W.S., Salleo A., Springer-Verlag – to be published.

Summary

- Higher deposition temperatures needed for good TFT stability
- Deposition at elevated temperature changes in-plane dimensions
- Changes are small if $\dfrac{d_f}{d_s} \lesssim 0.05$ (steel) or $\dfrac{d_f}{d_s} \lesssim 0.001$ (Kapton)
- CTE mismatch change in in-plane dimensions is

  ~ 20 ppm for a-Si:H TFTs on 100-μm steel foil

  ~ 500 ppm for a-Si:H TFTs on 100-μm Kapton foil

- Tailor built-in stress in the film to compensate CTE mismatch

  ⇒ **possible to eliminate misalignment**

  ⇒ **possible to eliminate curvature of the workpiece**