# 3-Dimensional Monolithic Nonvolatile Memories and the Future of Solid-State Data Storage

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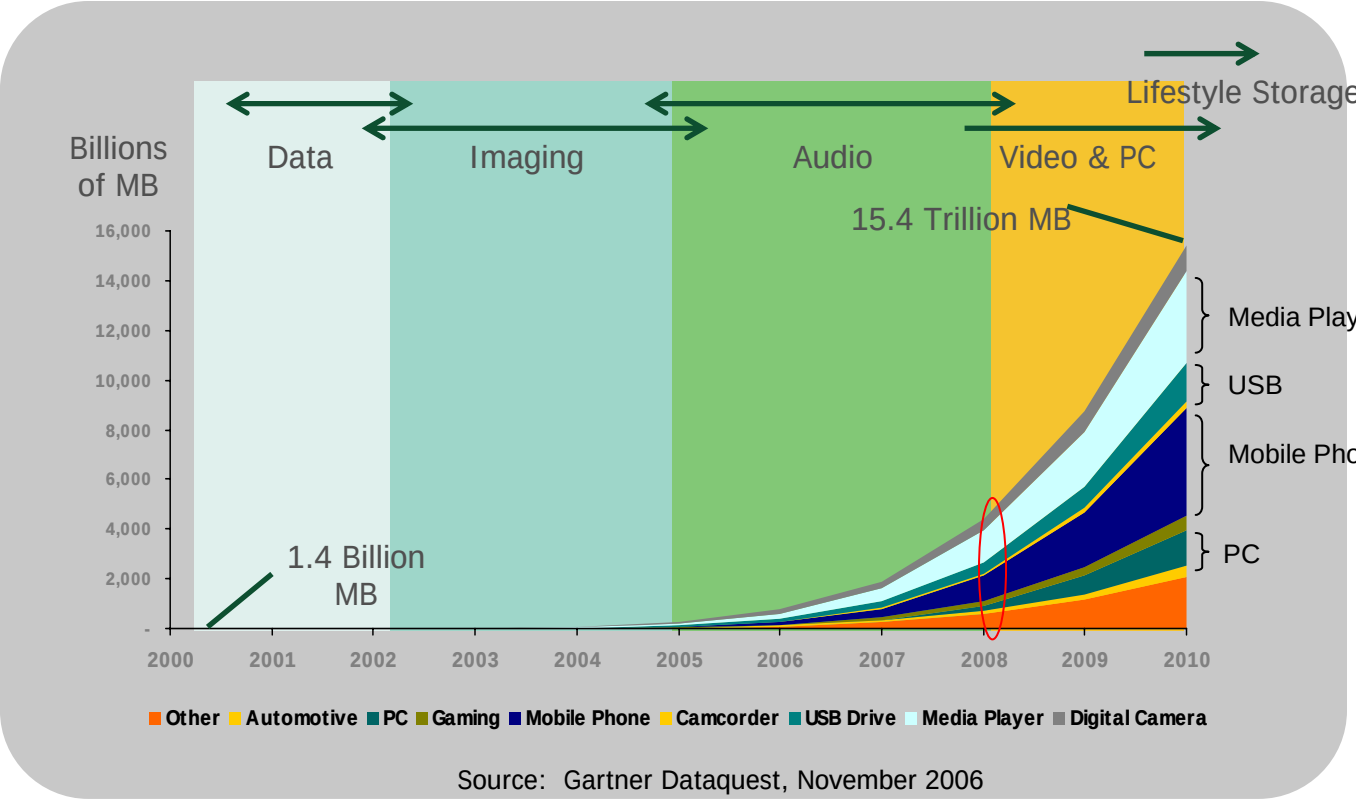
# Outline

- Flash memory market dynamics: what drives technology advances?
- The floating-gate technology roadmap
- Scaling challenges: what will replace the floating gate?
- Monolithic 3D memory: technical overview and future potential

# Flash Memory Market Dynamics

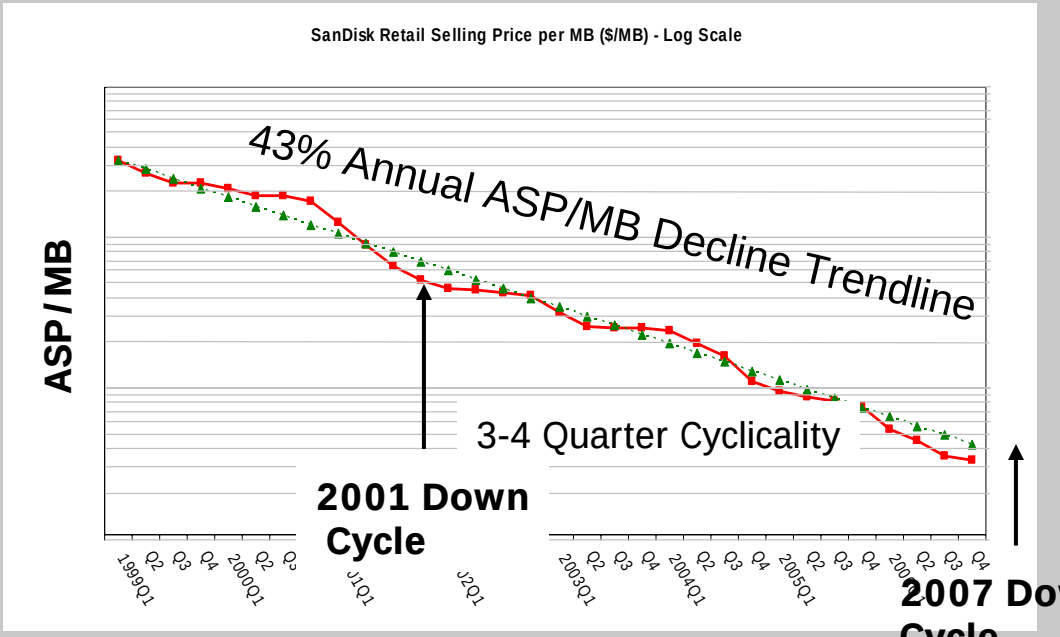
# Strong Demand Drivers of Flash Market Growth




Source: Gartner Dataquest, November 2006

- Bits shipped routinely doubles-to-triples year-over-year, fueled by rapid average-selling-price (ASP) reduction (next page)
- This is enabling exciting new markets such as flash-based MP3 players and video recording

# Continual $/MB Reductions Driving New Markets




*Source: SanDisk*

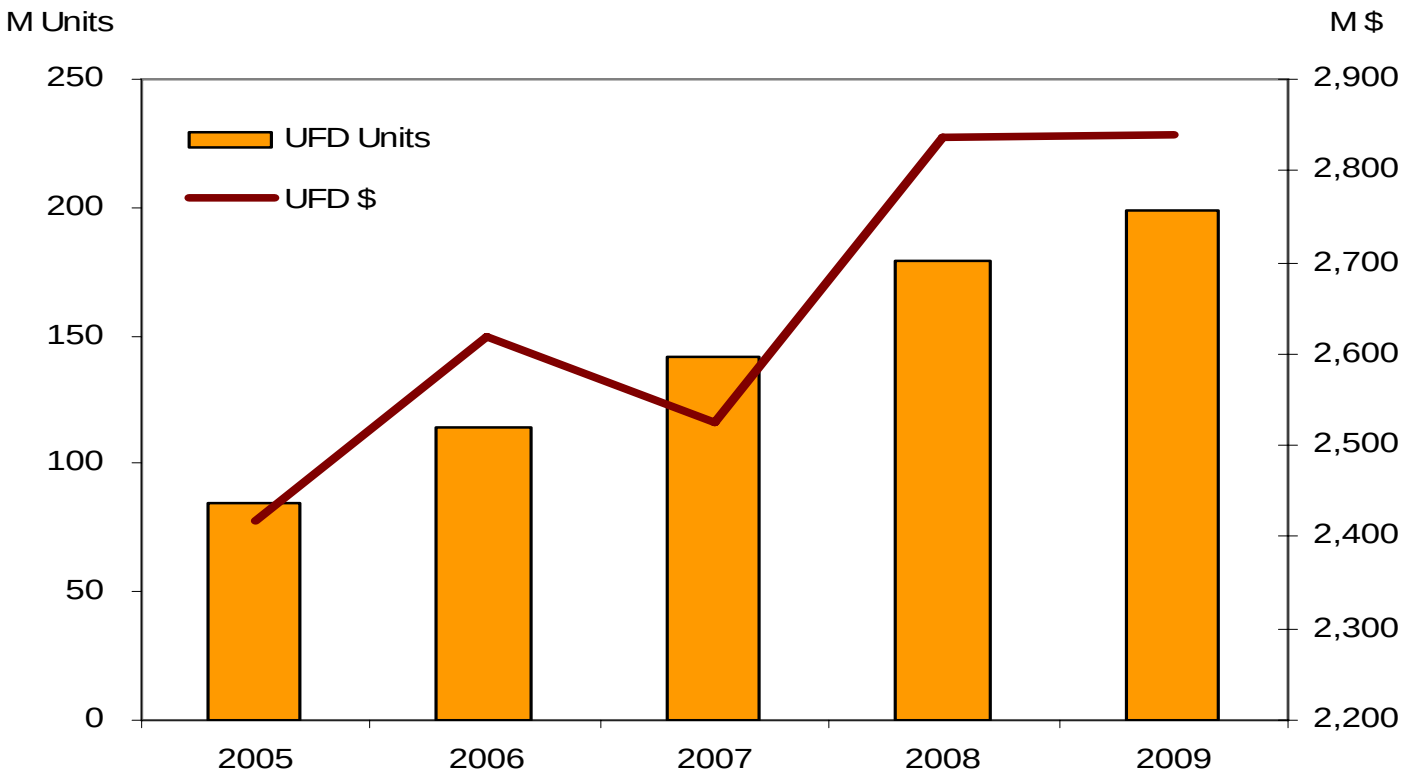
- Persistent, unrelenting price reductions, enabled by aggressive technology innovation, driving new markets shown on previous page
- Superimposed boom/bust cycles of more benign/more rapid ASP decline

# Projected Flash Trends: 2008 - 2011

- 40%-50% annual price reductions sustainable only by top tier players
- Smooth transitions to 5Xnm (2007), 43nm (2008/2009)
  - Transition points to date have been limited by photolithographic constraints (more on this later)
- Increasingly more complex NAND (Floating-Gate to Charge-Trap-Flash) transitions at 32nm, 22nm (2009-2011)
- 3- and 4-bit-per-cell critical for competitiveness in 2009-2011
- 200mm Fabs no longer competitive; 300mm wafers are now the norm in cutting-edge Fabs
- In next 1-2 years capacities should grow dramatically: 512MB-2GB → 4GB-32GB
- In next 3-5 years cumulative price reductions (~10X from 2007 to 2011) should become disruptive to DVD, HDD (hard disk drive), stimulate huge demand and create new Flash markets

# Sub-segment Market Growth

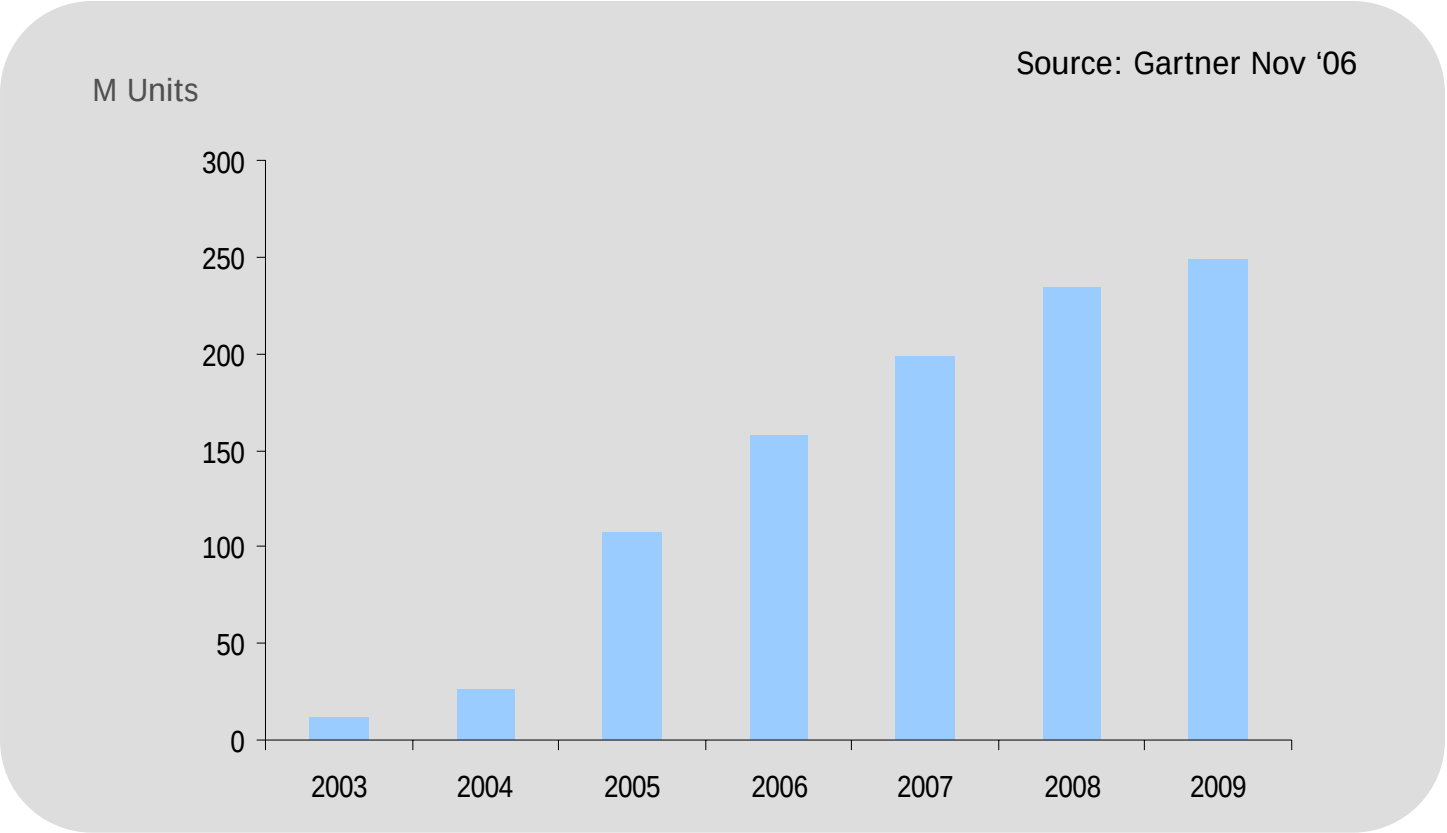
# USB ("Thumb Drive") Market Size




*Source: Gartner Nov '06*

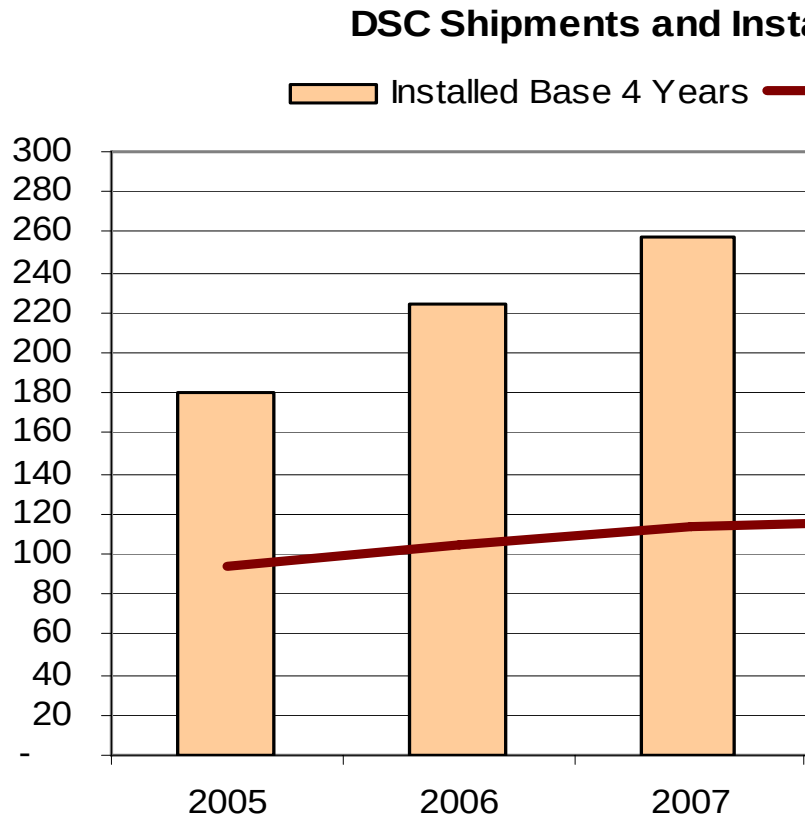
- 18% compound-annual-growth-rate (CAGR) in units shipped from 2006 → 2009, much higher than the semiconductor industry in aggregate
- Dollar growth less strong due to ASP declines

# Flash MP3 Player Market Size




- Very strong growth in the 2003 → 2006 timeframe as MP3 player manufacturers adopted flash memory
- 16% CAGR 2006 → 2009, as with USB showing continued strong growth

# Digital Still Camara (DSC) Market Size





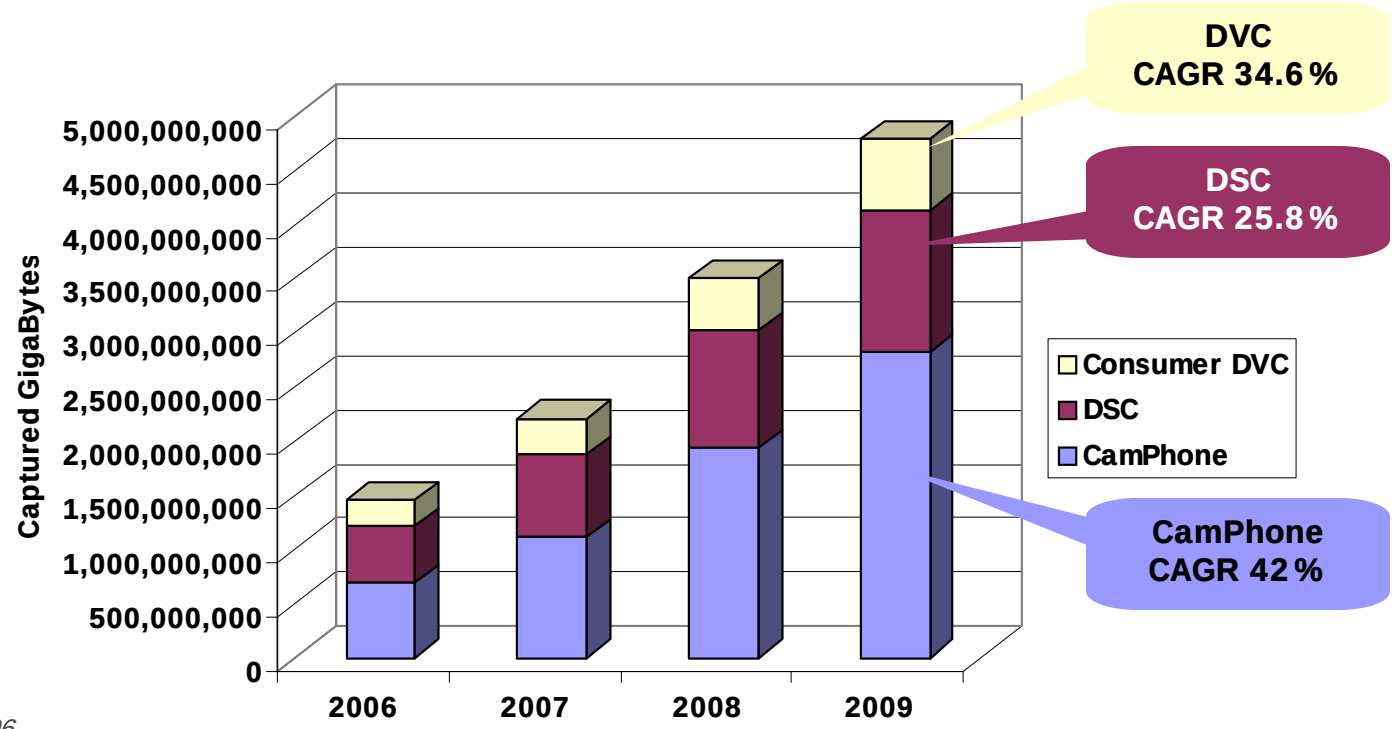


*Source: DSC Forecast IDC Sep'06, Installed Base: SanDisk Estimates*

- Roughly 120M DSC units ship per year, with a 260M DSC installed base (!)
- ~240M Flash cards sold per year with market size <$4.5B in 2007

# Video Consuming More Memory

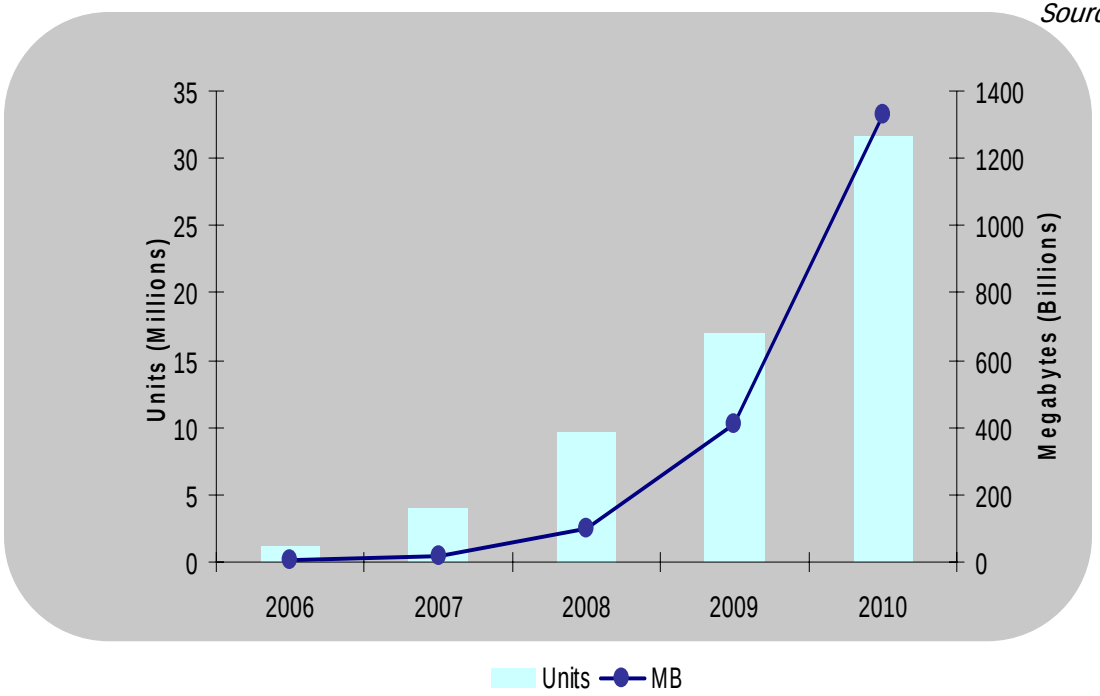
- Video Capture becoming a large driver of bit growth
  - IDC predicts that 4800 PBs will be consumed by Video in 2009[1]
  - Today 20% of all PBs used in Video is used for archival storage and will grow to >40% through 2009[1]
  - Camera phones are a large component of this




*Source1: IDC Dec. 06*

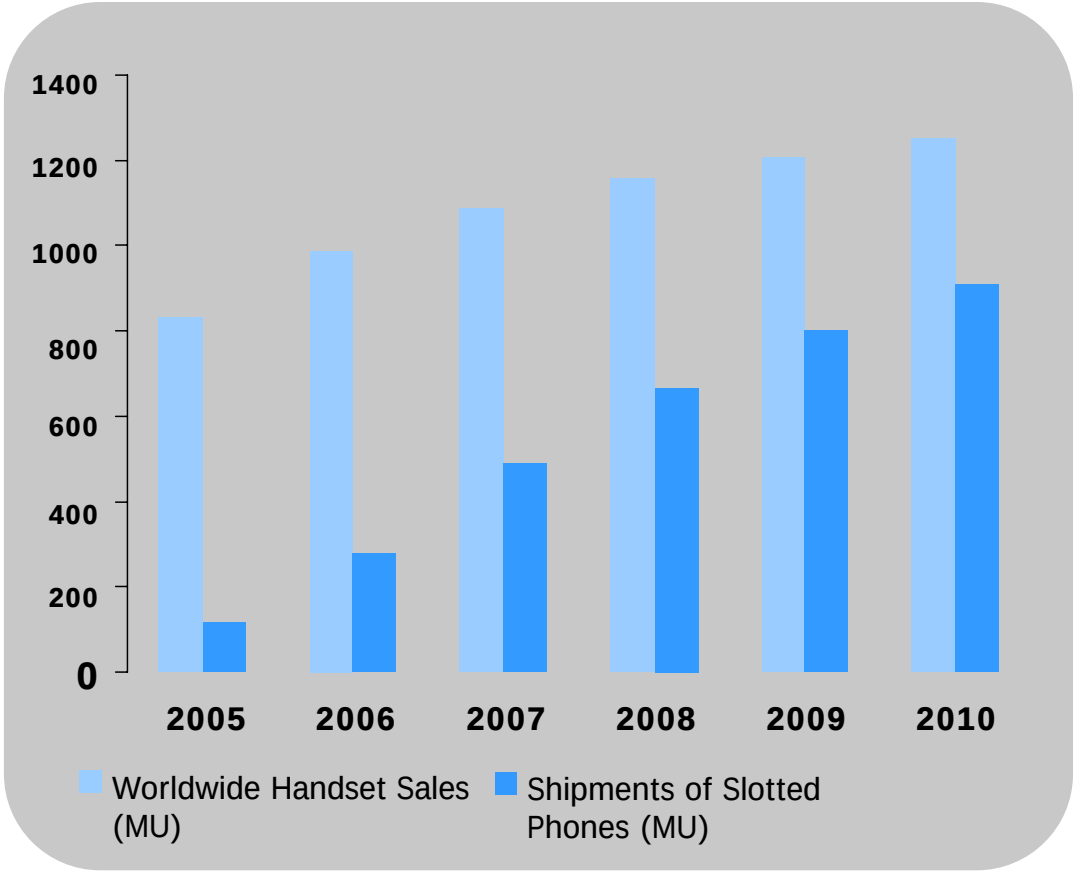
# Projected SSD Penetration in Notebooks by 2010

*Source: Gartner, December, 2006*
*Notebook market in 2010 is estimated at 153M units*




- Solid-state-drive (SSD) adoption driven by price elasticity and MLC adoption (must reasonably compete with rotating-media)
- SSD penetration in ~20% of the notebook market = 32M units
- 1300 PB of NAND flash to be used in SSDs or 11% of NAND output
- TAM >$3B in 2010 $100/system ASP

# Finally: Mobile Phones as the Market Leader




Source: Strategy Analytics, December 2006

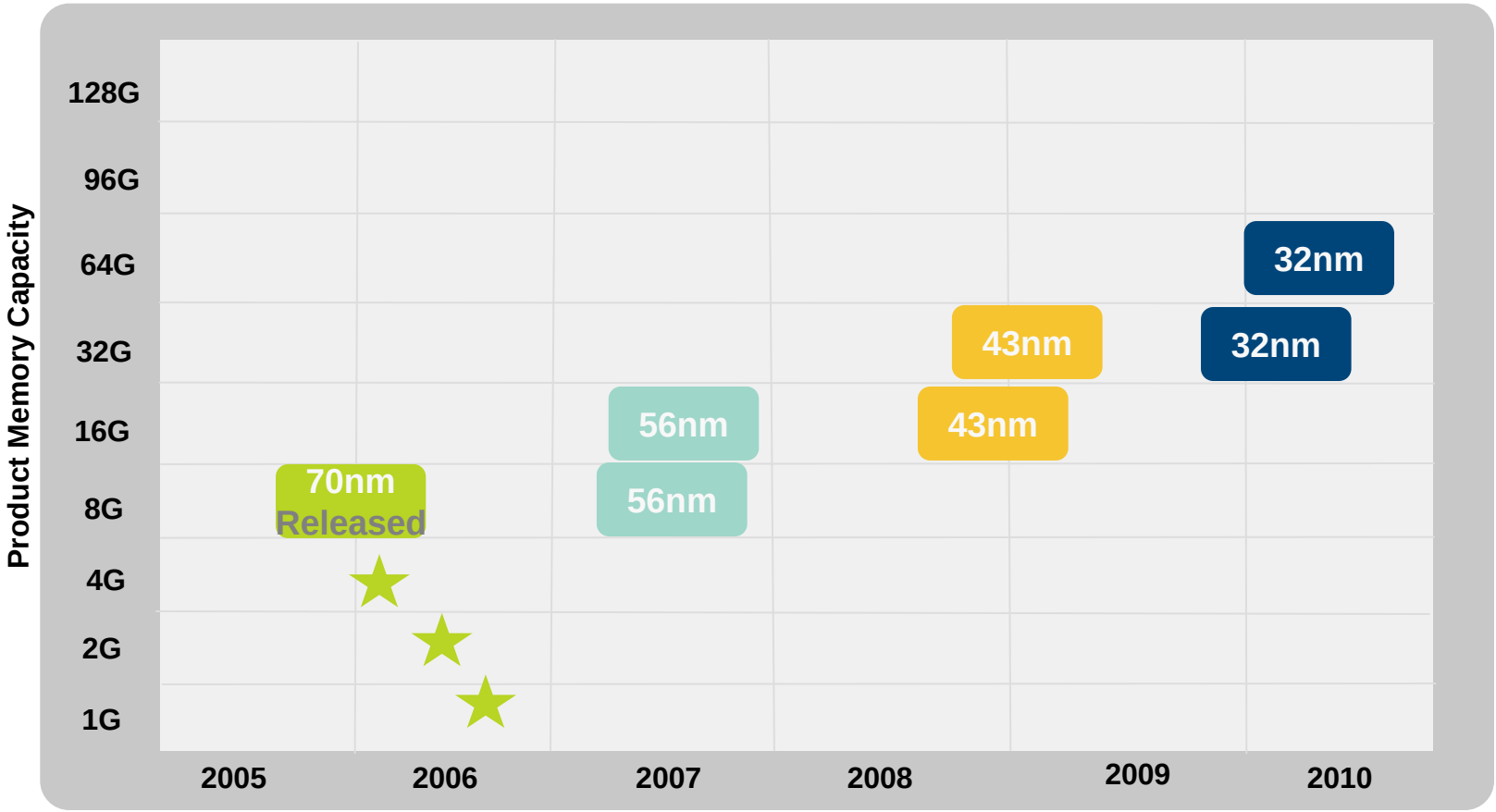
- 500M phones with Flash-card slots shipped in 2007, projected to almost double by 2010

# Conclusions – Market Dynamics

- The solid-state data storage market, dominated by Flash memory, has grown and will continue to grow very rapidly in the foreseeable future
- This growth has been driven entirely by the effects of price elasticity: lower prices lead to nonlinear growth in bits shipped, due to the appearance of new markets for memory
- The markets for Flash memory are now very diverse, ranging from music to video to still images to hard-disk replacements

# NAND Technology Roadmap

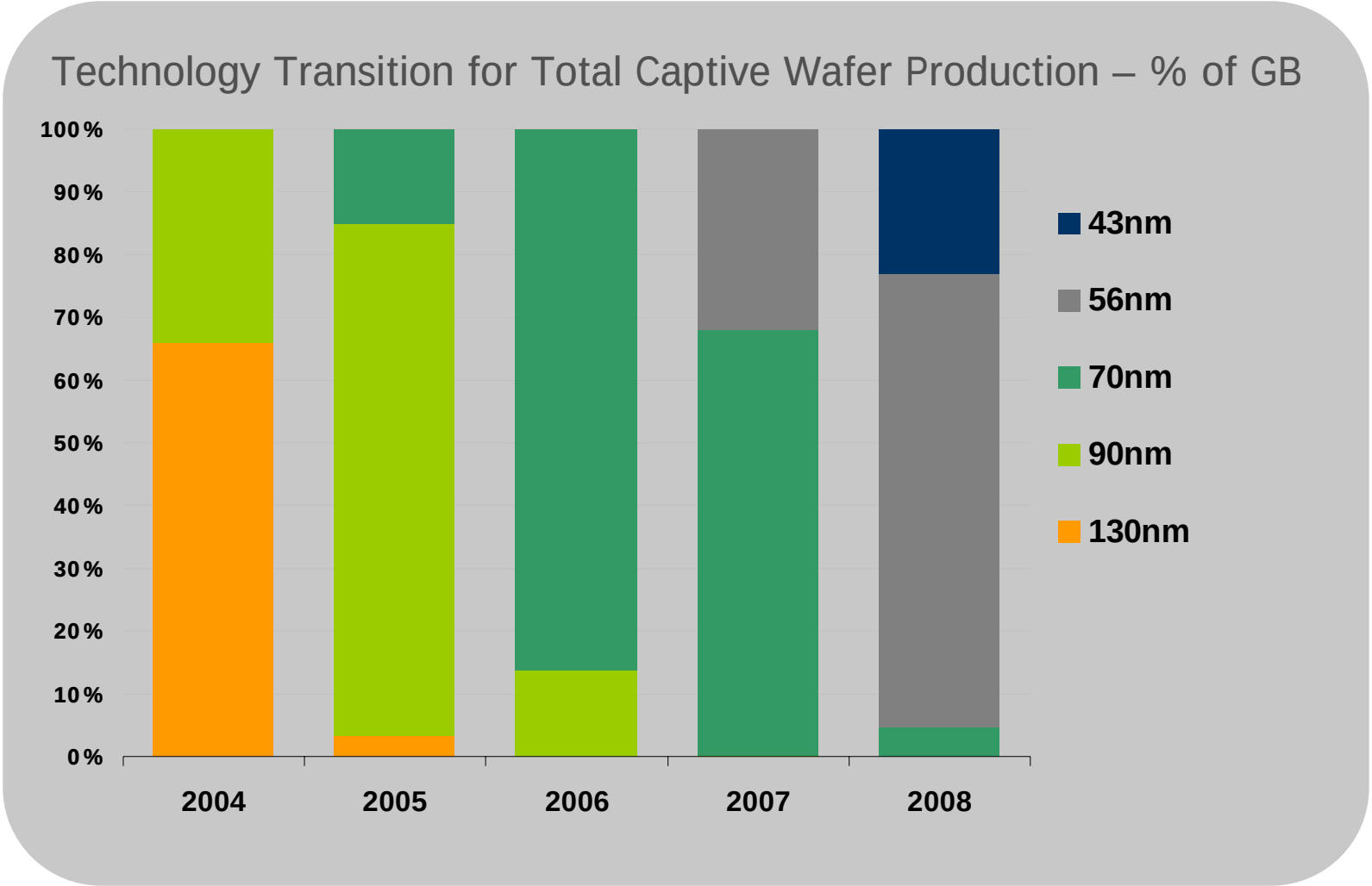
# NAND Memory Product Roadmap




Source: SanDisk

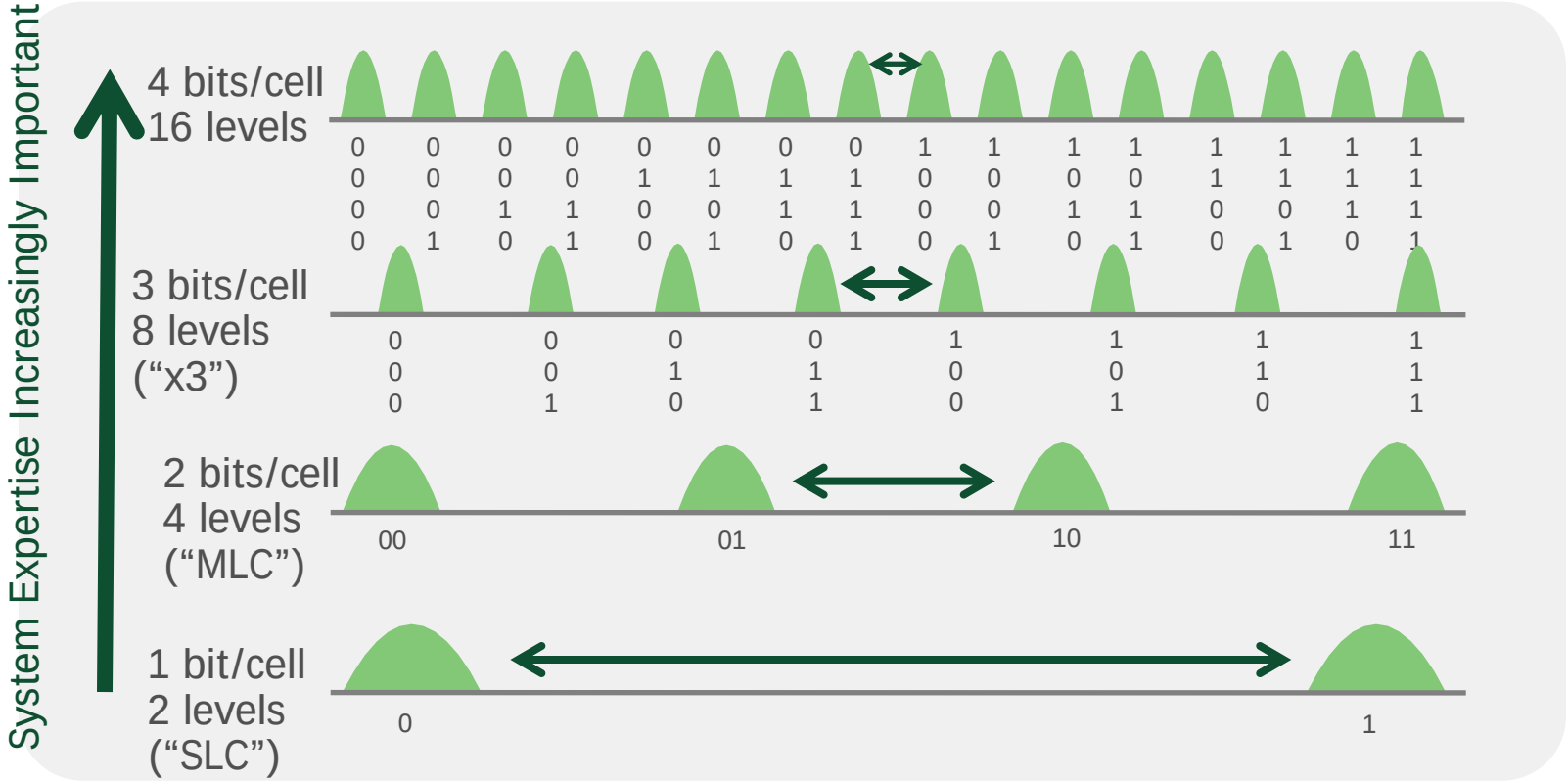
- Near-yearly technology-node transitions are responsible for the price declines and bit-growth described in the previous slides
  - 50% year-over-year price declines matched by YOY cost declines

# New Process Node Transition Every Year




Source: SanDisk

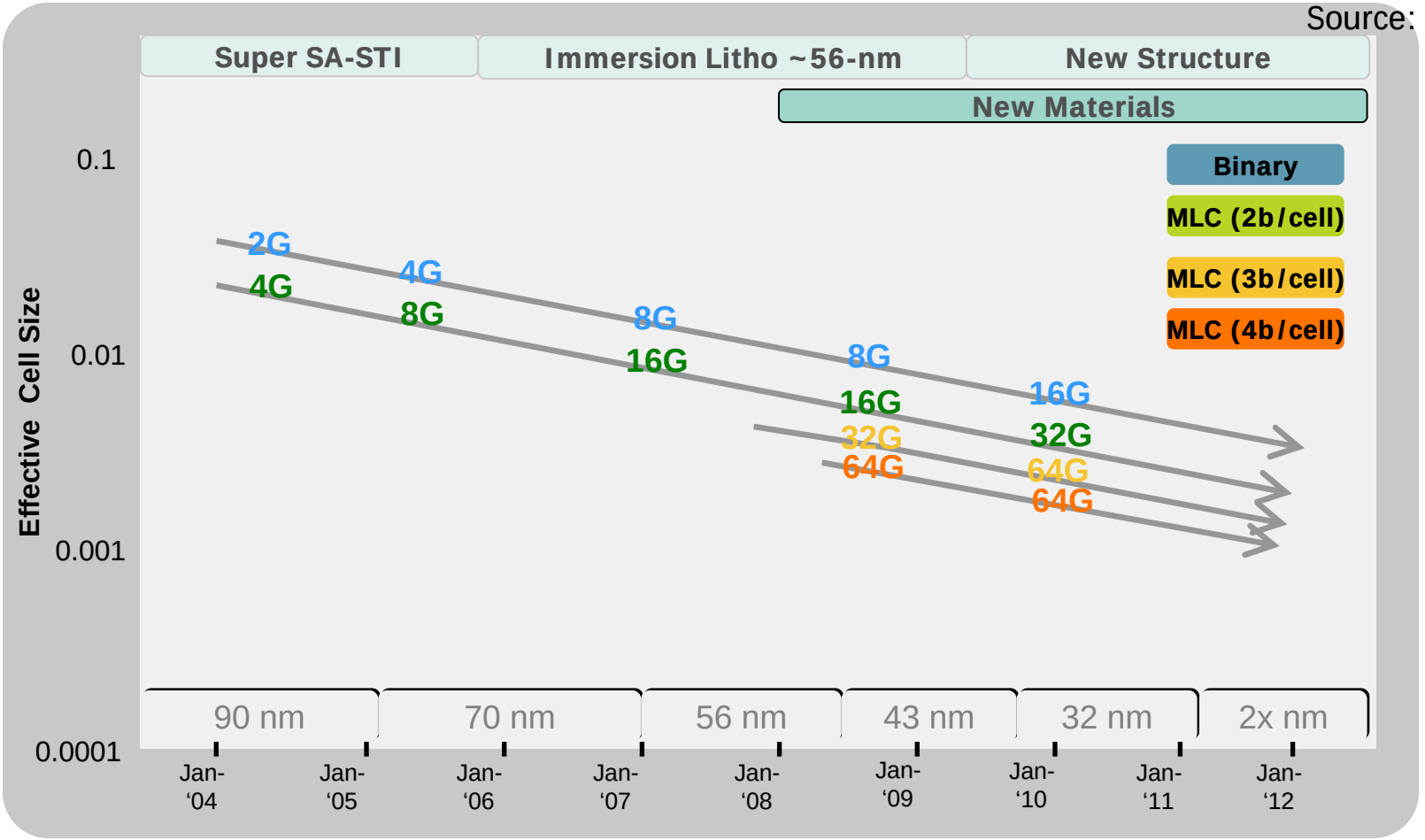
# Going Beyond 2 Bits/Cell ("MLC")




- Very advanced controller chips required to move above 2-bit/cell
  - Signal processing and other algorithm innovations to maintain high write speeds and data retention
  - Wear-leveling algorithms to increase endurance

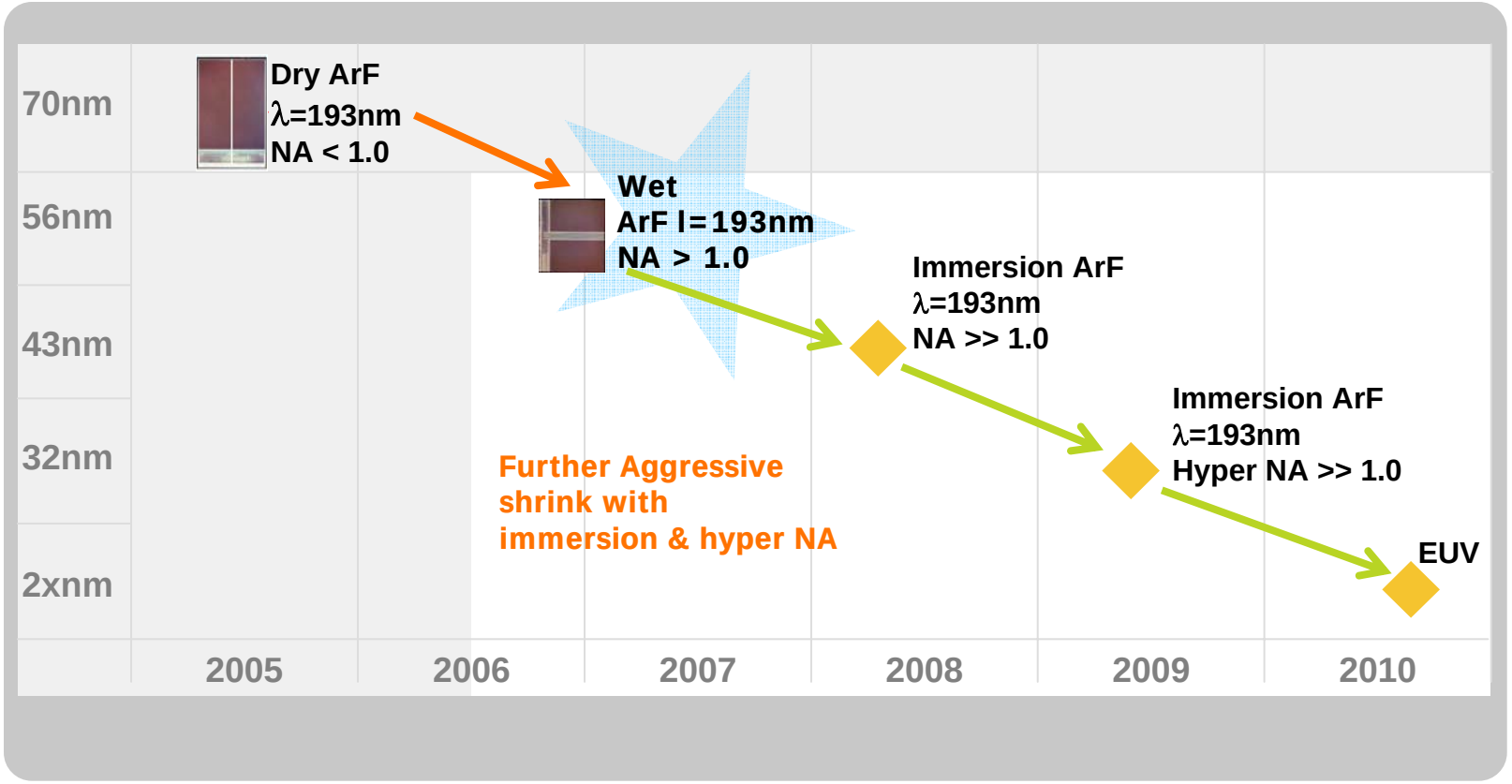
# Multi-bit-per-cell Implementation

Source: SanDisk




- 2-bit-per-cell (MLC) has been mainstream for several years now, among the top-tier suppliers
- 3-bit-per-cell (x3) on SanDisk's 56nm technology will ramp in mid-'08

# Photolithography as a Technology Enabler




Source: SanDisk

- For the past several years, brute-force physical scaling as lead the way to technology-node transitions
- Immersion lithography as a key enabler for 56nm and onwards

# Scaling Challenges and Alternate Devices

# Scaling Challenges

- Physical limitations
  - How do we print, etch and fill lines/spaces below 3xnm?
  - To continue on the Moore's Law trajectory of cost reduction, innovation is needed
- Cell-to-cell coupling
  - Vt shift due to coupling from adjacent cells exacerbated at tighter geometries
- Electron-loss tolerance (from floating gate)
  - Reduced allowance for electron loss to avoid large Vt shift

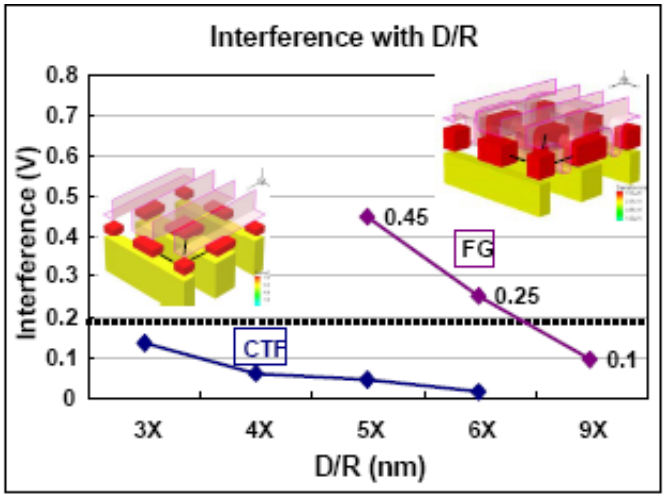



Fig. 4. Comparison of cell-to-cell interference for floating gate and CTF type NAND flash memory.

Source: Kim and Jeong, 2007 IEDM

SanDisk

| | NONVOLATILE MEMORY TECHNOLOGIES COMPARISON | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | FG NAND | SONOS (CTF) | Mirror Bit | PCM | FeRAM | MRAM | RRAM | Probe Storage | 3D NAND | 3D Diode |
| Cell Size | Small ~ $4F^2$ | Small ~ $4F^2$ | Medium ~$10F^2$ | Small ~$6F^2$ | Large ~$20F^2$ | Large ~ $30F^2$ | Small~$4F^2$ | Very small (nm) Tip size and scan precision dependent | Small~$4F^2$ | Very small $4F^2/n$ |
| CMOS Integration | Good | Good | Good | Good Compatible with back end process | Poor Etching difficult | Poor | Potential good. But no sufficient data | Not compatible. | Good | Good |
| W/E Current per cell | Very Small | Very Small | Medium 10 – 100µa | High ~mA | Small ~1µa | Very High 5-10 ma Scales poorly | Potential small. Scales poorly | Not known. Storage media dependent | Very Small | No Data |
| Endurance | **$10^4$-$10^5$** | **$10^4$** | **$10^4$** | **~$10^5$** | **$10^8$ - $10^{12}$** | Theoretically infinite | No data | Not Known. Potentially very high | Comparable w/ NAND (?) | No Data |
| Scalability | Good down to 2x nm | Good down to 2xnm. Possible 1xnm(?) | Down to 5x nm | Questionable. Endurance is affected by the volume of the PCM material | Poor | Poor. Write current increases with scaling | Good | Good. Tip size and scan precision only dependent | Good | Good |
| MLC Capability | Yes. In production. | Possible with improved material | 2 bits proved. 4 bits ?? | Has potential. Not proved on products. | No | No | Has potential. Not proved. | Not sure | Has potential. | No Data |
| Company | SanDisk Toshiba Samsung Hynix, Micron | In Development Samsung SanDisk / Toshiba, Macronix | Spansion 1Gb (ORNAND) | In Development Intel, IBM, Samsung 512Mb Quimonda | Fujitsu Ramtron 1Mb | Freescale 4Mb Samsung IBM 16Mb | In development cell level (many companies) | Seagate Nanochip IBM(?) | Samsung Macronix Toshiba | SanDisk – . .. |

# NVM Technology – Next Five Years

- Floating Gate (FG) NAND
  - Likely scalable to ~20nm
  - x3 will likely become mainstream by 2009
  - x4: SanDisk plans to lead through system/controller solutions, initially targeting A/V markets (starting 2008, growing impact in later years)
- Charge Trapping (CTF) NAND
  - Advocated by Samsung and Hynix for below 40nm (~2009)
  - Planar structure has scaling advantages, unknown difficulties/risks
  - x3, x4 implementation may be more challenging for CTF
- NROM (Quadbit)
  - Competitive with NOR, probably not a serious threat to high-density NAND
- PCM, MRAM, Nanotubes, Milipede
  - Not a serious threat to high-density NAND in the next five years

# NVM Technology – Next Five Years (Cont'd)

- 3D Read/Write
  - Long-term potential to disrupt/displace NAND, HDD
  - R/W switching actively researched: expected productization in the next several years (more on this later...)

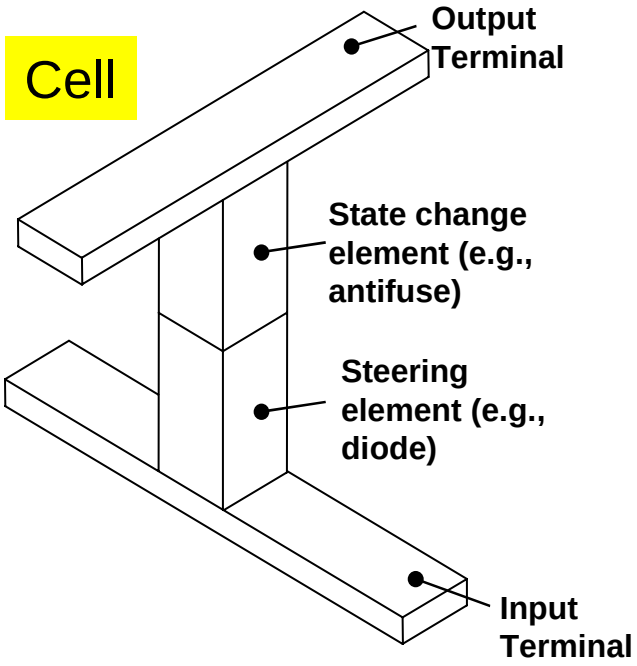
# SanDisk 3D Technology Overview

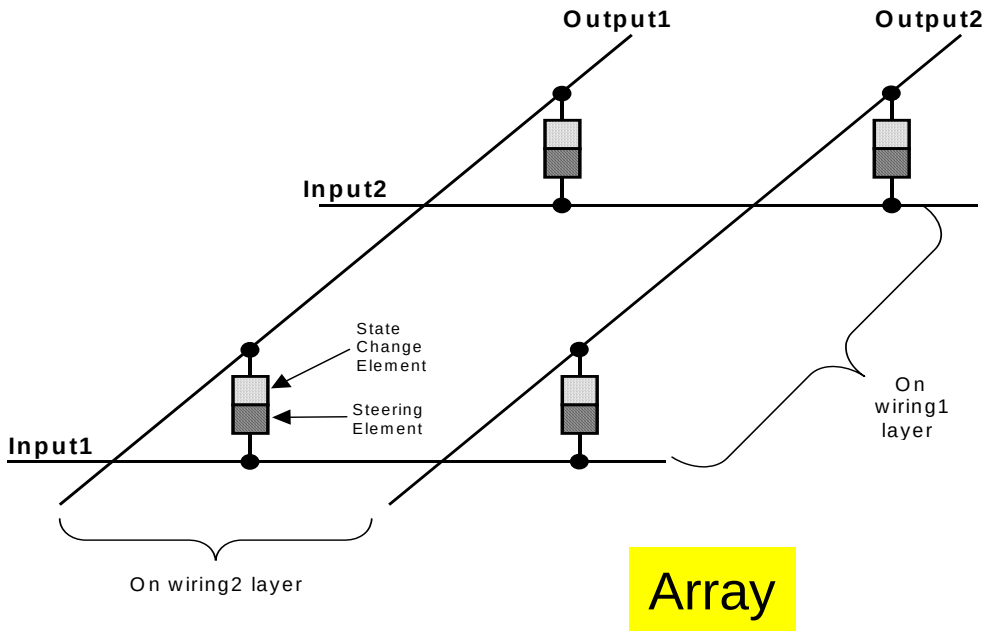
# SanDisk 3D Technology Summary

- SanDisk 3D has brought to high volume an NVM where arrays of memory cells are stacked above control logic circuitry in the 3rd dimension
  - Stacking 3D memory directly over CMOS allows for high array efficiency and very small die size
- The technology uses no new materials, processes or Fab equipment
  - Control logic circuitry composed of typical CMOS
  - Memory construction using typical backend processing tools
  - Each memory layer is a repeat of layers below
  - CMOS node can lag memory node ("hybrid scaling")
    - Example: 0.13um-generation CMOS with 80nm-generation memory
- The technology is inherently scalable
  - Multiple technology generations proven using the same cell architecture
  - Lithography-driven scaling allows for rapid cost reduction

# SanDisk 3D Memory Cell

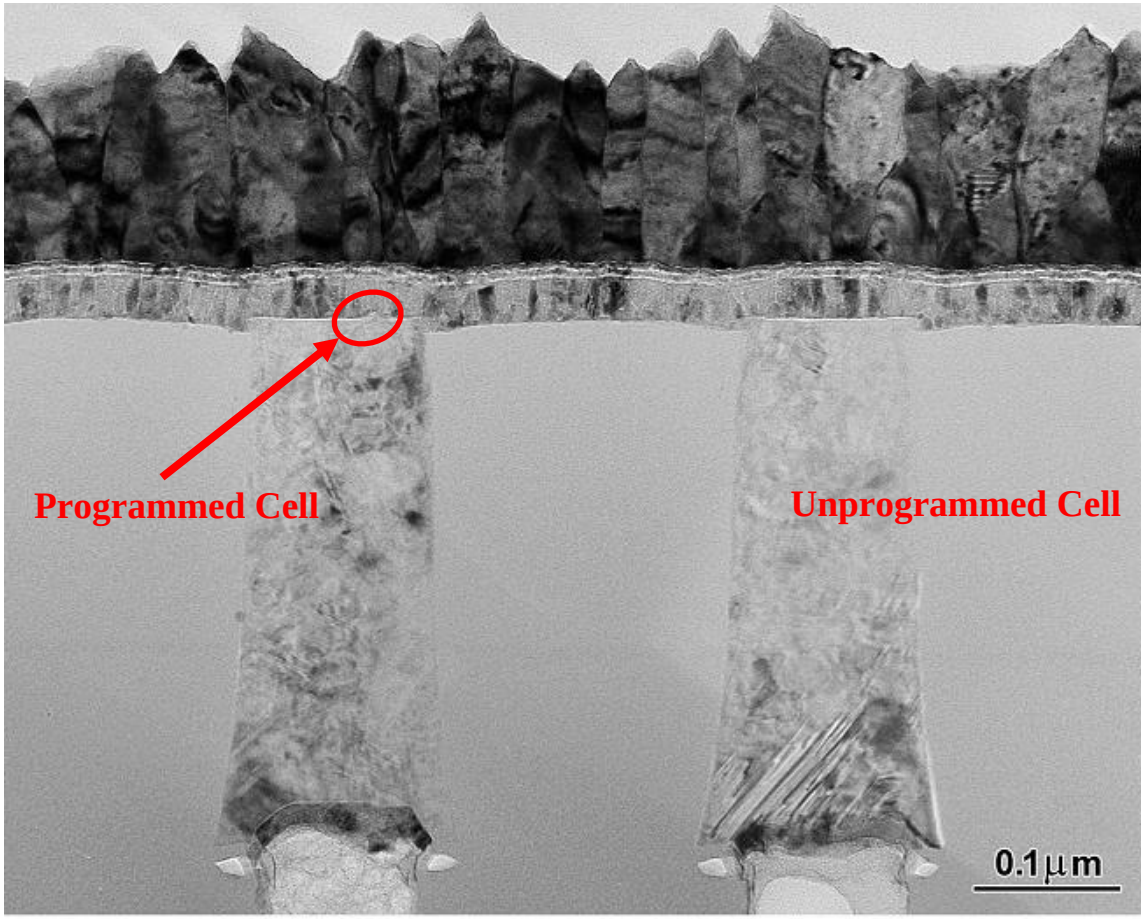
- The 3D cell consists of a vertical diode in series with a memory element



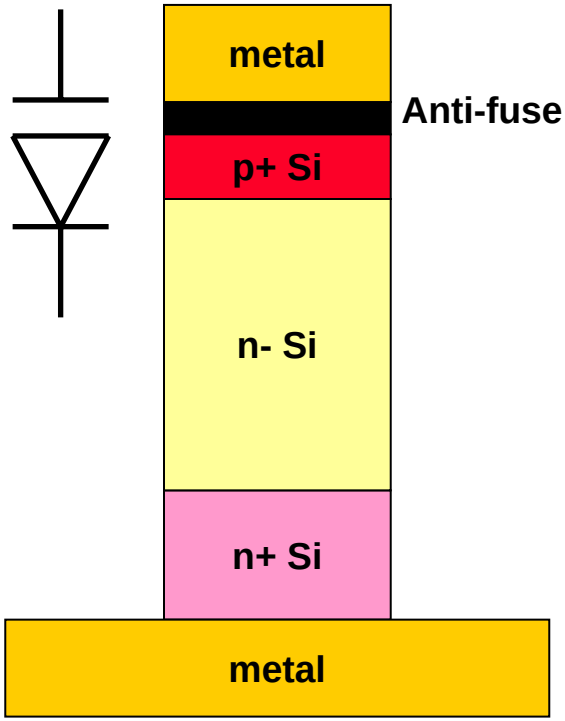




- State-change element is...
  - Irreversibly altered in the case of OTP memory
  - Reversibly altered in the case of re-writeable (R/W) memory

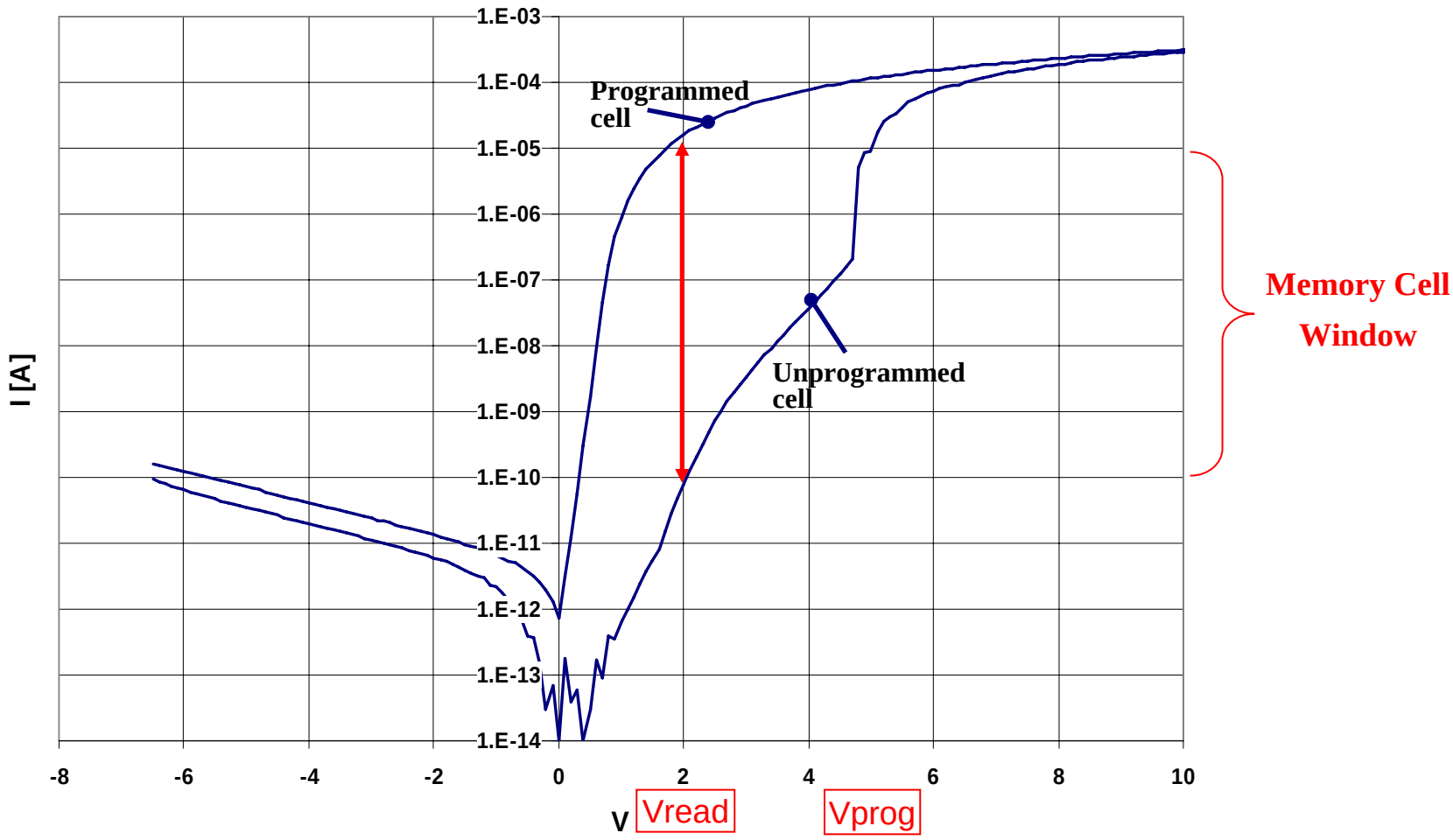
# SanDisk 3D OTP Memory Cell




Precision TEM, Inc. (408) 980-8898 Q80047.1 wafer #2 Die ( 20,19 ) X-cut



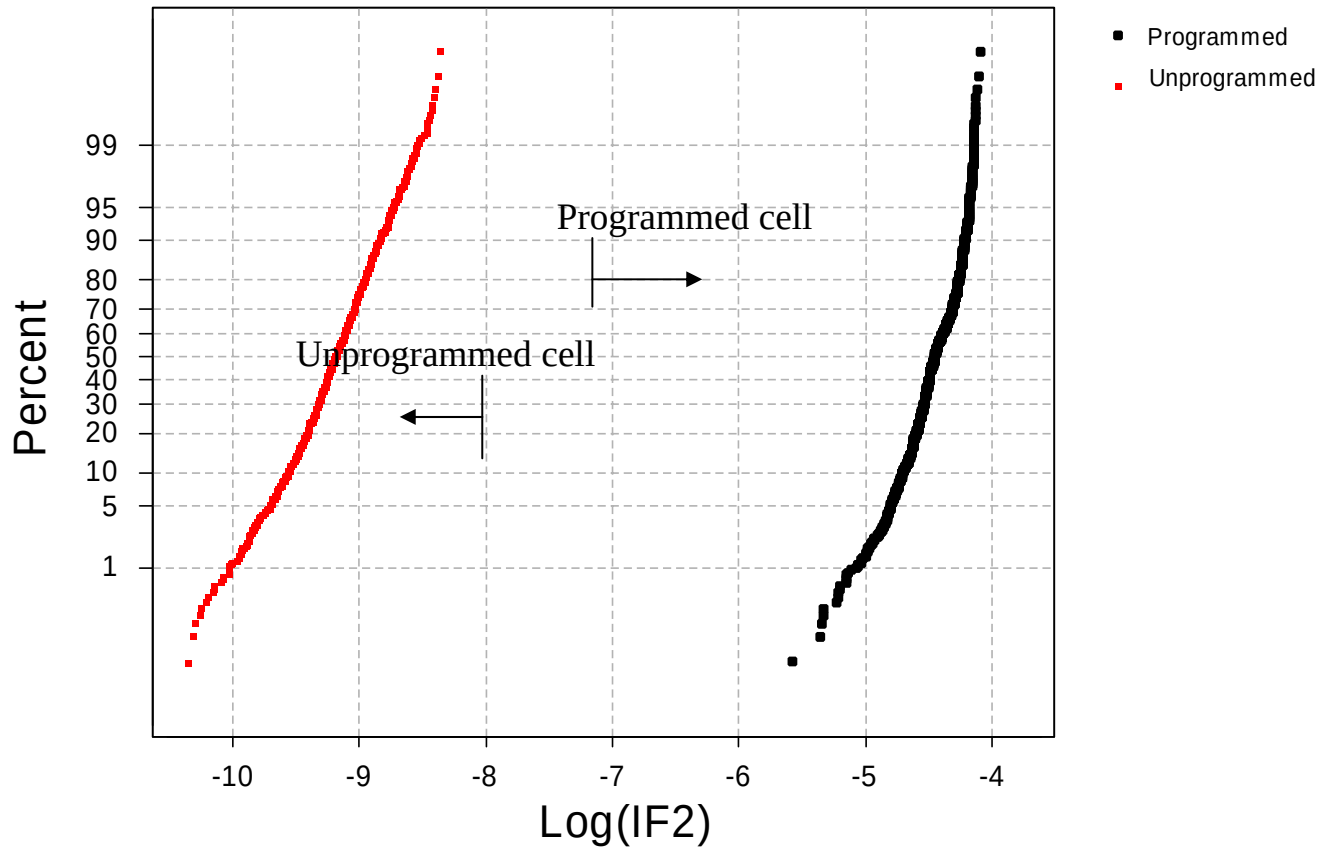
# OTP Memory Cell I-V Curve




- > 4 orders cell window at 2V read voltage

# OTP Memory Cell Read Window

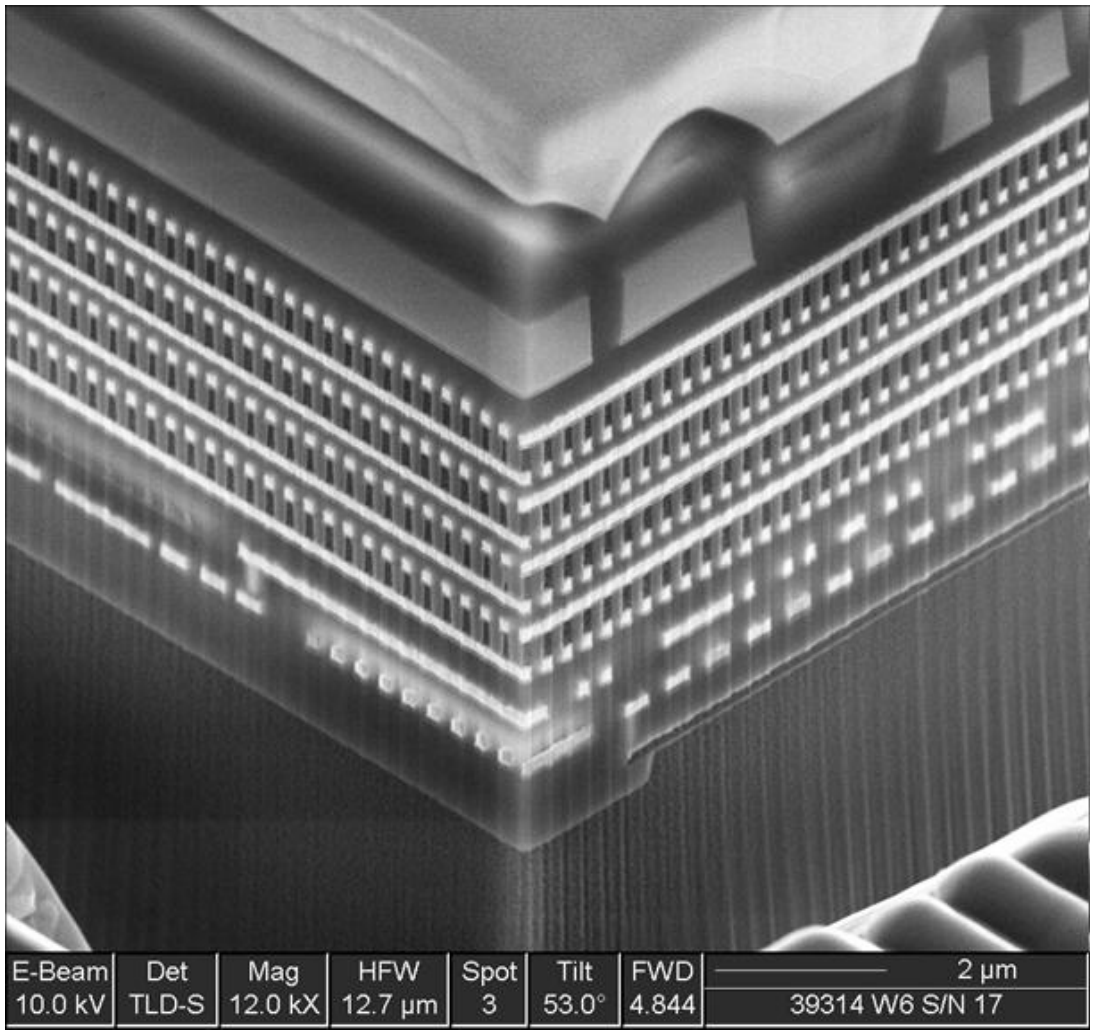
Current at 2V for programmed and unprogrammed cells




- Wide [> 4 orders] read margin when considering distributions of millions of cells

# SanDisk 3D Physical Cross Section

- Memory array is composed of repeating layers of poly-Si memory cells built directly above CMOS




**Al top metal**

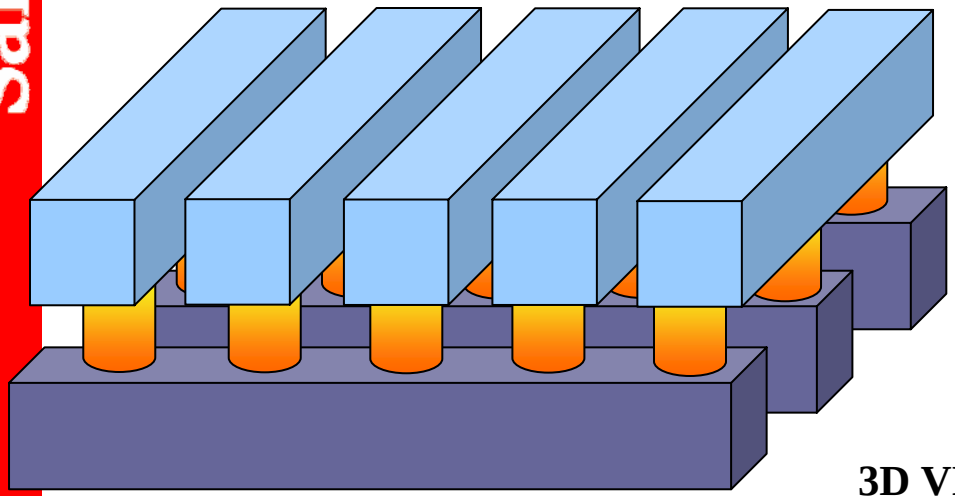
**4 layers of memory cells + tungsten interconnect**

**2 levels of tungsten routing**

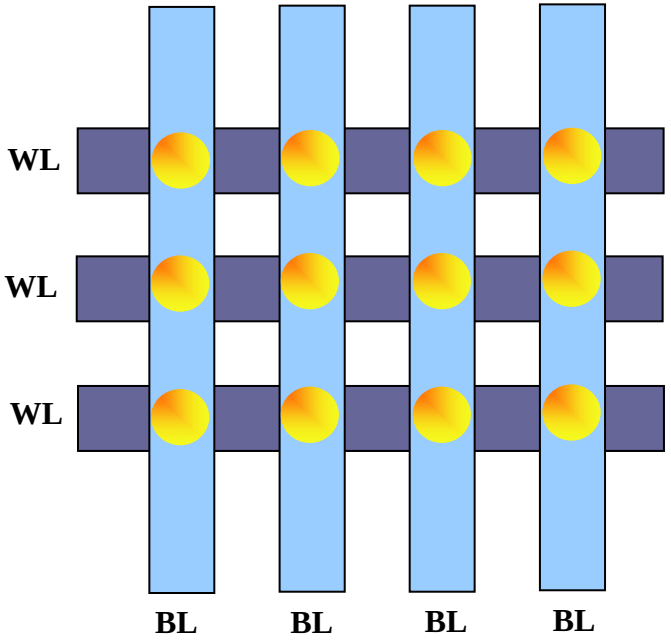
**LV + HV CMOS logic**

# SanDisk 3D Array Architecture

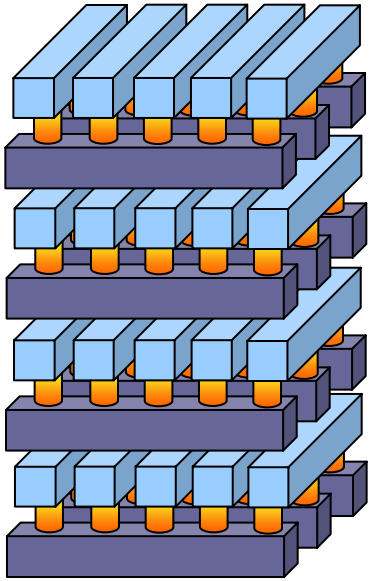
SIDE VIEW



TOP VIEW




3D VIEW



# SanDisk 3D R/W Cell Development Update

- OTP and R/W cell developments are tightly coupled and share most of the process module and design architecture ideas
  - Recall that the identity and behavior of the switching element defines OTP or R/W capabilities
- Several parallel research activities are being pursued, exploring several types of switching behavior
- We have produced several distinctly different cells, each capable of being integrated into the existing 3D architecture
- We have developed a test vehicle to test out some of the ideas being generated that allows us to rapidly collect statistics on large number of cells
- We are seeing very encouraging results from our development efforts – *please stay tuned for results in the near future…*

# Overall Concluding Remarks

- The flash memory marketplace is one of the most vibrant and exciting in the semiconductor industry, not to mention one of the most competitive
- The dominant flash cell architecture, the conventional floating gate, will see significant, if not unsurpassable, scaling challenges below the 2x nm technology node
- In order to continue the pace of price reductions that consumers demand, significant innovation is needed, both at the device and system level
- Many candidate device architectures are in development; we are strong believers that 3D is a viable candidate