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CIGS PV Technology: Challenges, Opportunities, and Potential

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CIGS: A High Content Technology

Outline

- Review: State of the CIGS technology
- Technical Challenges
- Opportunities: Efficiency and Cost
- Potential: - Closing the gap between laboratory cells & modules

  - Cost ? **$ 0.50 module + 0.50 BOS = $1/W**

Acknowledgement: Thin Film Group, M&C Group, and Alan Goodrich

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CIGS Device Structure

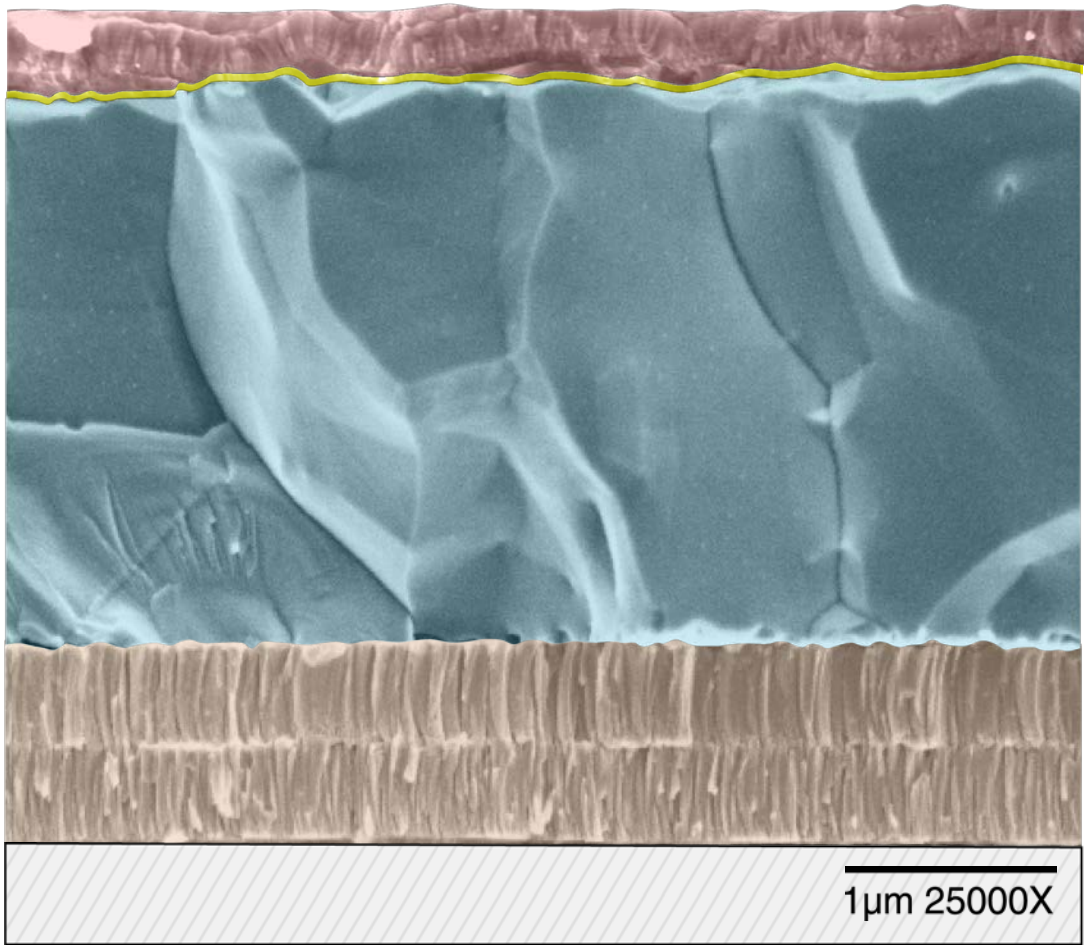
ZnO, ITO
2500 Å

CdS or ZnS
500 Å

CIGS
1-2.5 µm

Mo
0.5-1 µm

Glass,
Metal Foil,
Plastics



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Parameters of High Efficiency CIGS Solar Cells

Sample Number	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill factor (%)	Efficiency (%)
ZSW	0.740	35.40	77.5	20.3 ZSW
M2992-11	0.690	35.55	81.2	20.0 NREL
S2229A1-3	0.720	32.86	80.27	19.0
S2229A1-5	0.724	32.68	80.37	19.0
S2229B1-2	0.731	31.84	80.33	18.7
C3010-22-4	0.803	29.15	79.47	18.6
AIST, Monolith Flex. Module	11.60 (0.683)	34.00	68.40	16.0 (75 cm^2)
EMPA, Polyimide	0.670	34.00	74.10	16.9 (18.6)
NREL, Nakada, SS	0.650	36.38	74.20	>17.5

Tolerance to wide range of molecularity

Cu/(In+Ga) 0.95 to 0.82

Ga/(In+Ga) 0.26 to 0.55

Yields device efficiency of 18% to >20%

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“High End” Modules from MFG Line (pilot line)

Company	Device	Aperture Area (cm^2)	Efficiency (%)
Stion	CIGS (glass)	0.985 m^2	14.5
AVANCIS	CIGSS (glass)	4938 (26 x 26)	13.0 (15.5)
Solar Frontier	CIGSS (glass)	3600 (30 x 30)	13.0 (18)
Solibro	CIGS (glass)	0.684 m^2 (cell)	14.4 (17.4)
Global Solar	CIGS (flexible)	8390 (120 cm^2)	13.0 (15.3)
Miasole	CIGS (flexible)	1.2 m^2 (cell)	15.7 (17.5)
Solopower	CIGS (flexible)	0.33 m^2 (120 cm^2)	13.5 (15.1)
TSMC	CIGSS (glass)	30 x 30 cm^2	15.7 (16.4)
First Solar	CdTe (glass)	6623, high volume	12.7 (16 champ)

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Technical Challenges

Large impact on performance and cost

Targeted Metrics for the roadmap

(Efficiency improvements and cost reductions)

Metrics	Current State of Art		Proposed Targets		Cost Reduction (W_{PDC})
	Laboratory	Commercial	Laboratory	Commercial	
Enhance efficiency (%)	20.00	12.00	22.00	>16.00	
V_{OC} (volts)	0.70	0.60	0.75	0.70	$0.12
J_{SC} (mA/cm^2)	35.40	30.00	36.50	34.00	$0.07
FF	0.80	0.66	0.80	0.70	$0.04
Subtotal (efficiency-related reductions)					**$0.23**
Rapid CIGS growth		0.15 µm/min		0.50 µm/min	$0.12
Alternative buffer	70-nm wet CdS & ZnS	70-nm wet CdS	20-nm CdS; 70-nm sputtered ZnS	20-nm CdS; 70-nm sputtered ZnS	$0.05
Subtotal (area-related cost reductions)					**$0.17**
Total (area- and efficiency-related cost benefits)					**$0.40**

V_{OC} = open-circuit voltage; J_{SC} = short-circuit current density; FF = fill factor; W_{PDC} = Watt peak direct current

Higher efficiency through higher photovoltage

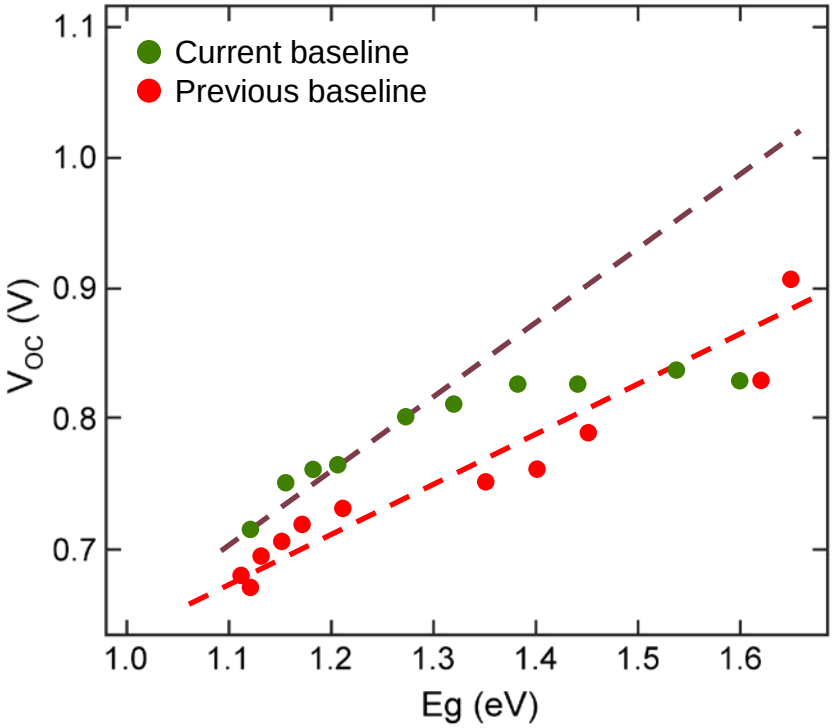
Goal: Demonstrate V_{oc} between 0.75 and 1.0 V for Ga content between 30 and 100% with efficiencies higher than the state of the art.

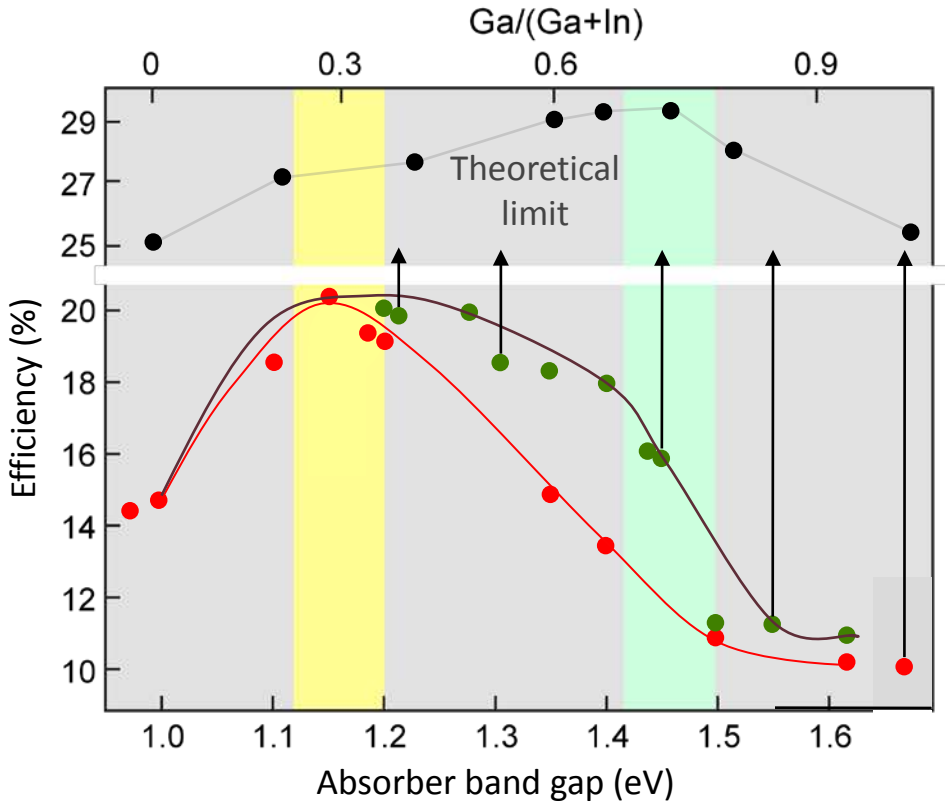
Relevance: Being able to maintain high efficiency (>20% as in low Ga cells) while raising the Ga content of the cell relative to In content, allows progress toward higher theoretical efficiency.

The cost reduction opportunity is about $0.12/W

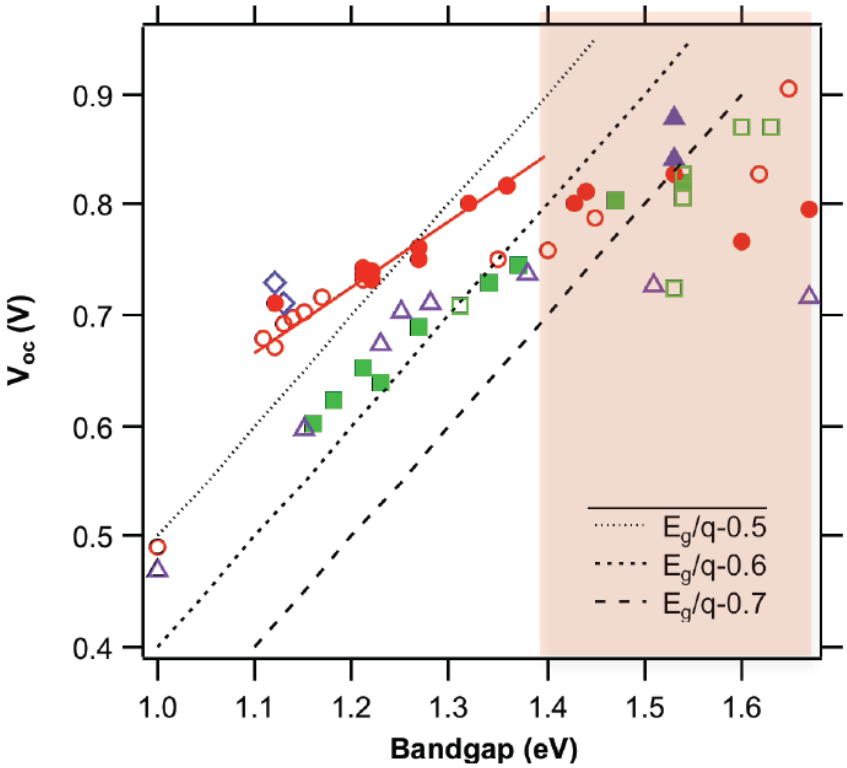
Efficiency / V_{OC} vs Band-gap / Composition

The Challenge: High Efficiency Across the Whole Composition Range



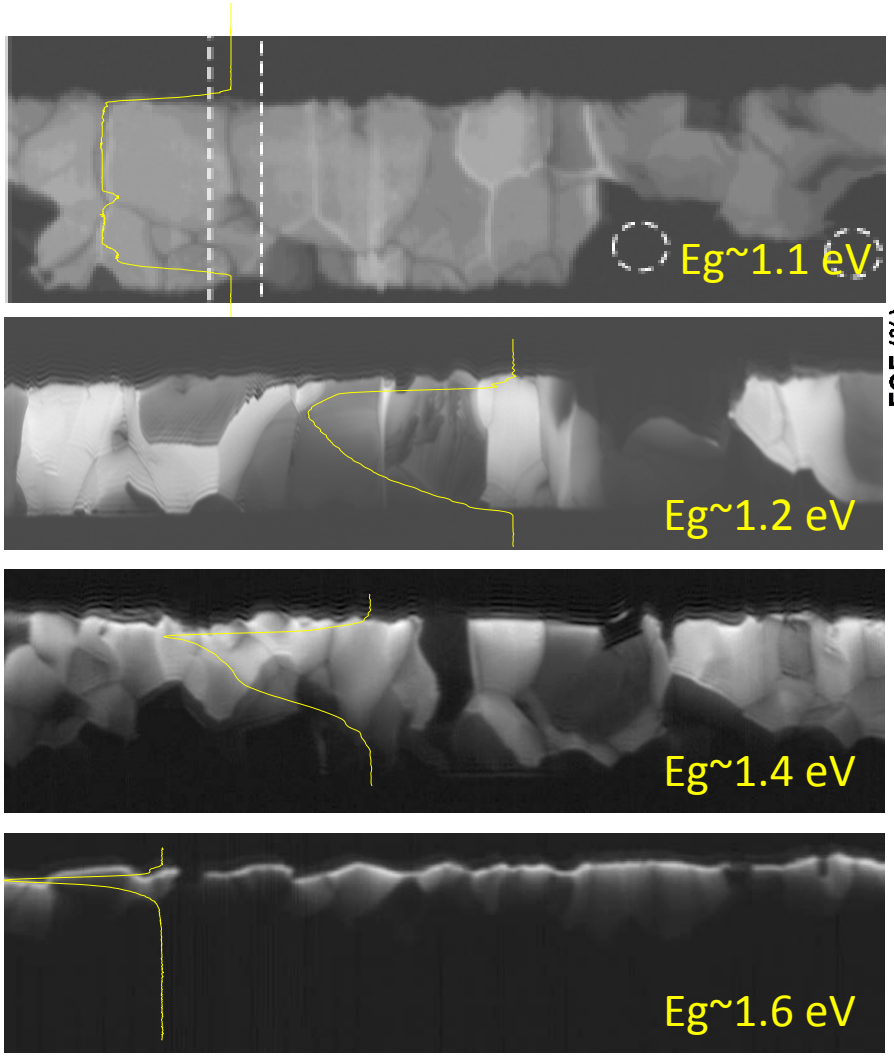


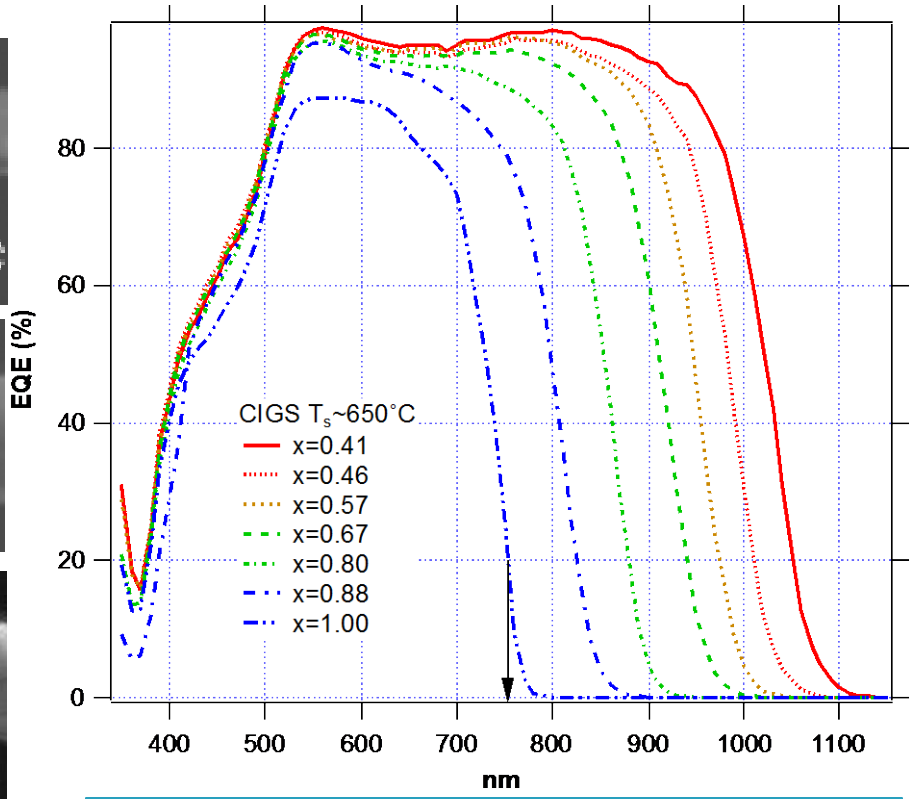
Voc is limited to a certain value



V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	E_g (eV)
0.743	31.9	78.75	18.7	1.21
0.752	31.2	77.73	18.3	1.27
0.801	28.5	77.21	17.7	1.32
0.817	27.5	76.65	17.2	1.38
0.801	24.4	75.55	14.8	1.43
0.813	26.9	72.17	15.8	1.44
0.829	20.2	65.32	11.0	1.53
0.766	20.9	71.02	11.4	1.60
0.795	16.4	69.22	9.0	1.67

Results: EBIC/EQE





•as the Ga content is increased, the overall collection of the cells decreases predominantly for the longer wavelengths (diff. length)

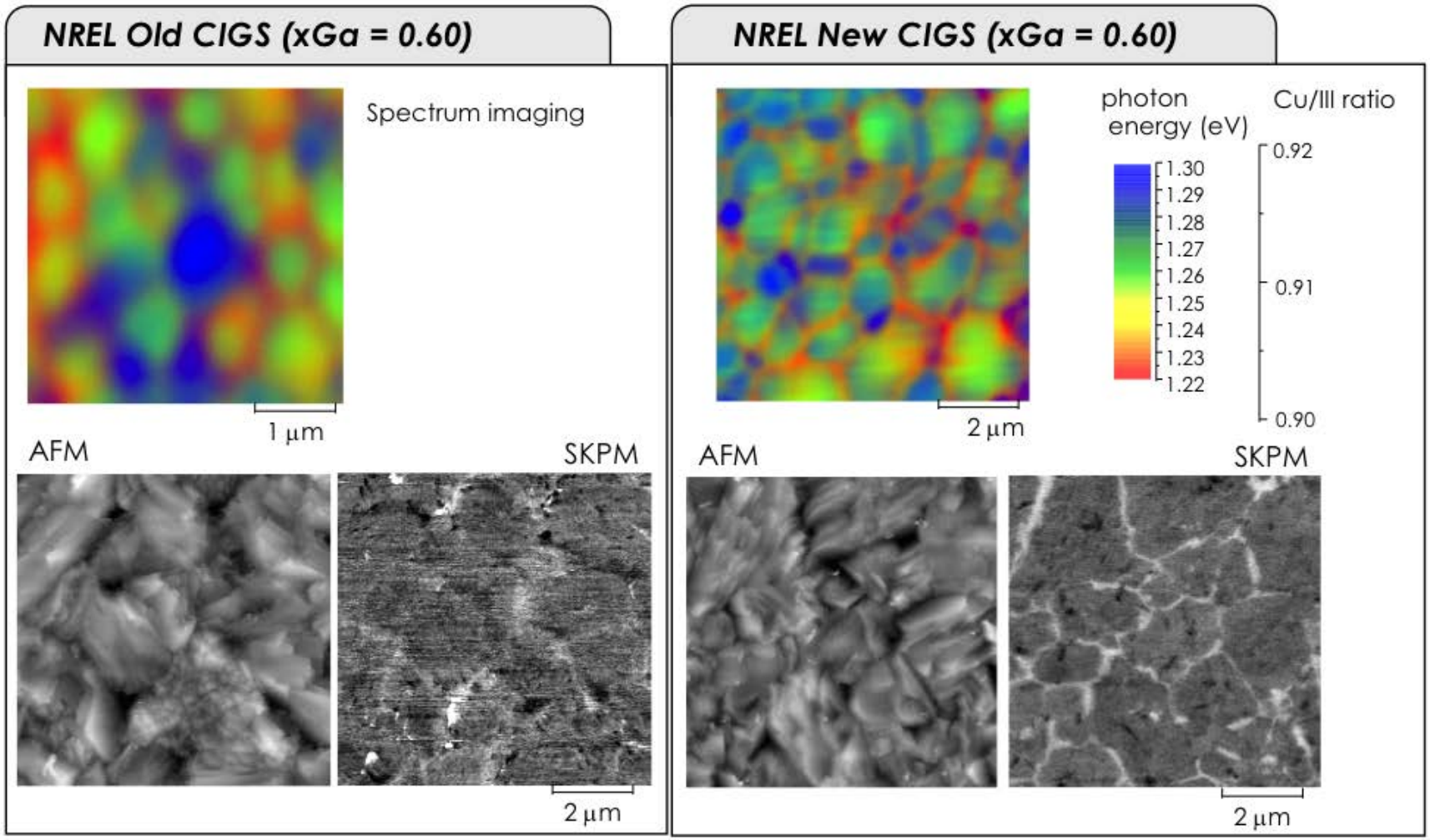
• highest bandgap materials, such as the $CuGaSe_2$ case, also show an overall lower collection efficiency (<90%) in the visible wavelengths, an indication additional recombination is further limiting the performance of such cells (interface recombination?)

Key findings: (a) loss of collection efficiency as Ga is increased

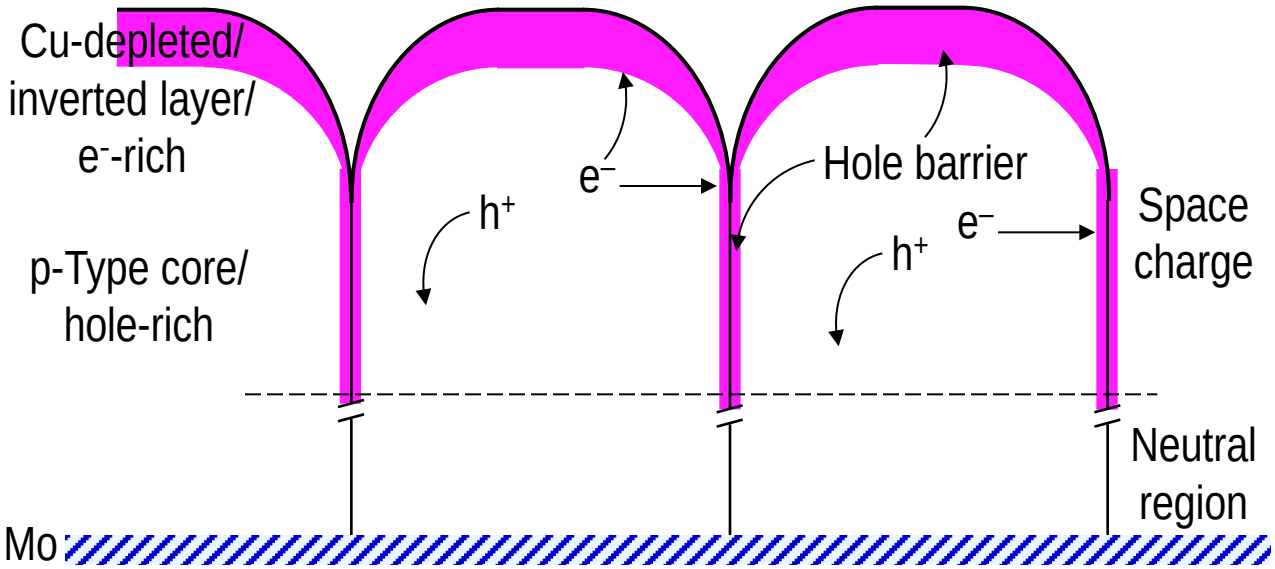
(b) Existence of random and discrete electronically inactive grains in carrier generation/collection

ANALYTICAL MICROSCOPY GROUP: origin of inactive grains and/or interfaces (chemical, structural, optoelectronic studies of grains and grain boundary)

Electronic Properties of Grain Boundaries in the Improved High-Ga CIGS Solar Cells



Grain/Grain Boundary Structure Model



Cu-poor Defect Layer

- A surface region (of finite thickness) including GBs exists which is Cu-deficient relative to the bulk of the grains
- Cu-vacancies result in decrease in p-d repulsion. The latter causes a lowering of the E_V maximum, and effectively an increase in E_g
  - See: Albin et al, *MRS Proc.*, 228, p. 267, 1992; Jaffe et al, *Phys. Rev.* B27, 5167 (1983); B29, 1882, (1984)
  - As a result, a barrier is created that repels holes from the surface and GBs.

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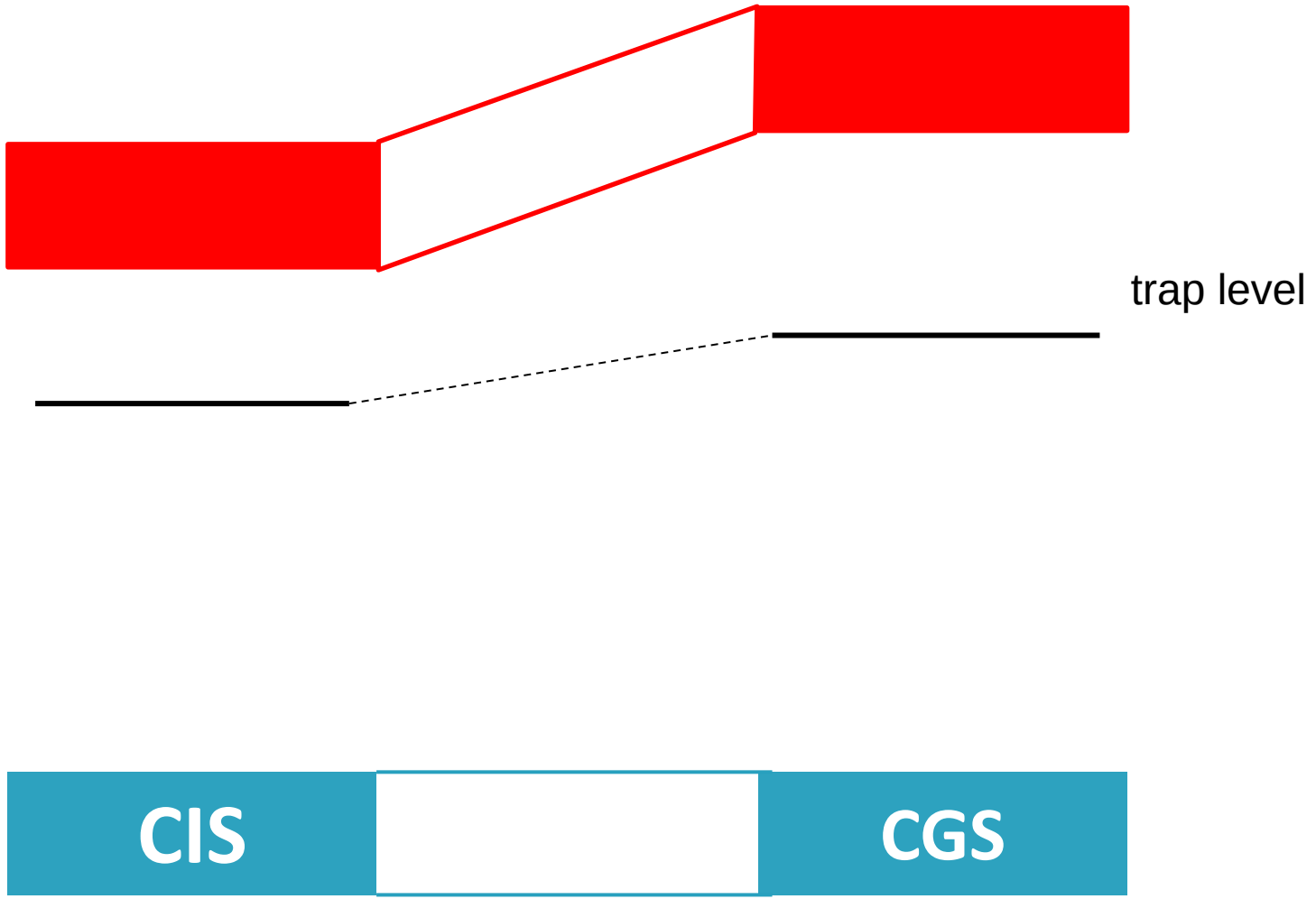
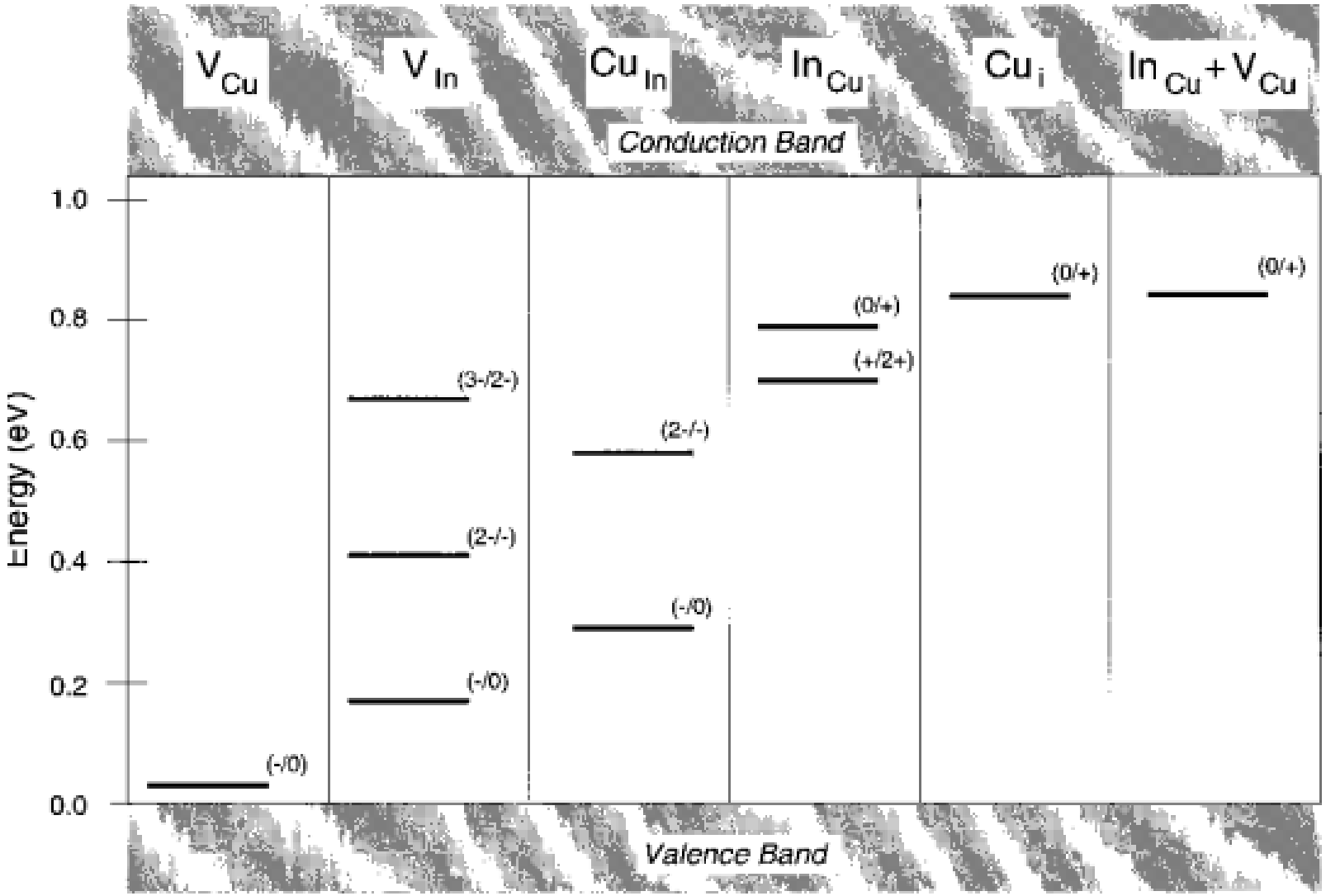
Possible physical origin—electronic issue



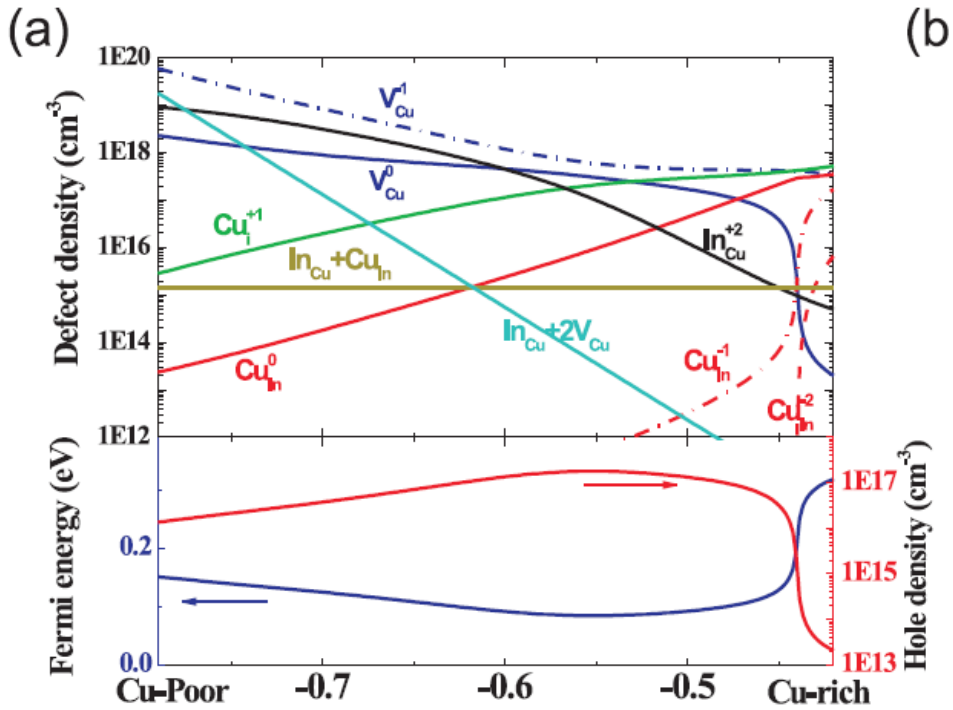
Previous defect calculations in CIS/CGS

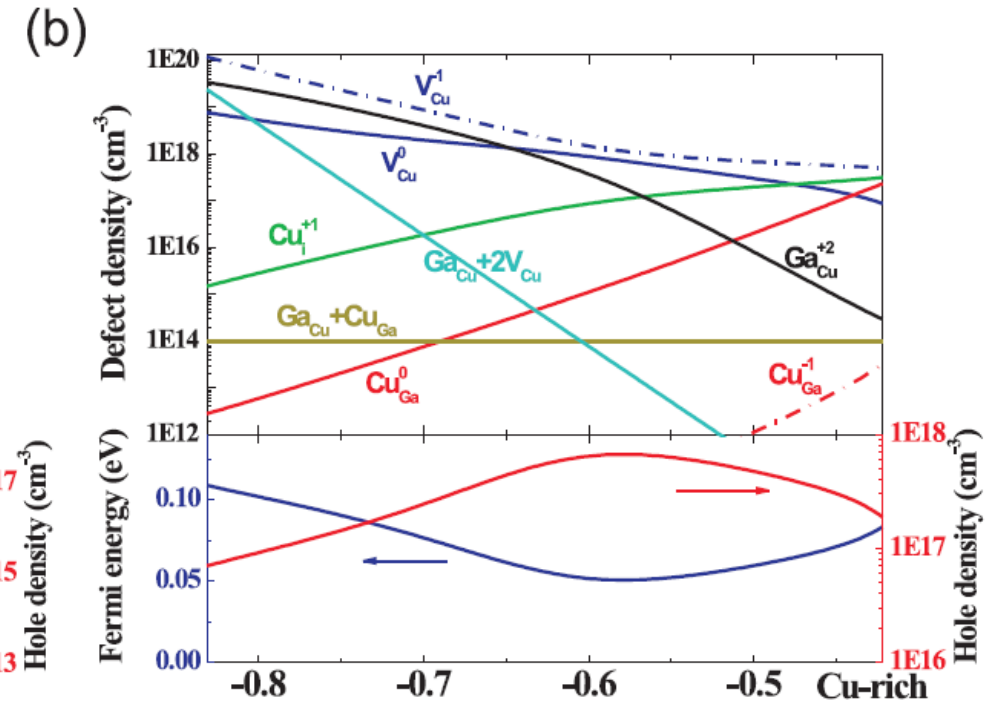


S. B. Zhang et al. 1998

CIS

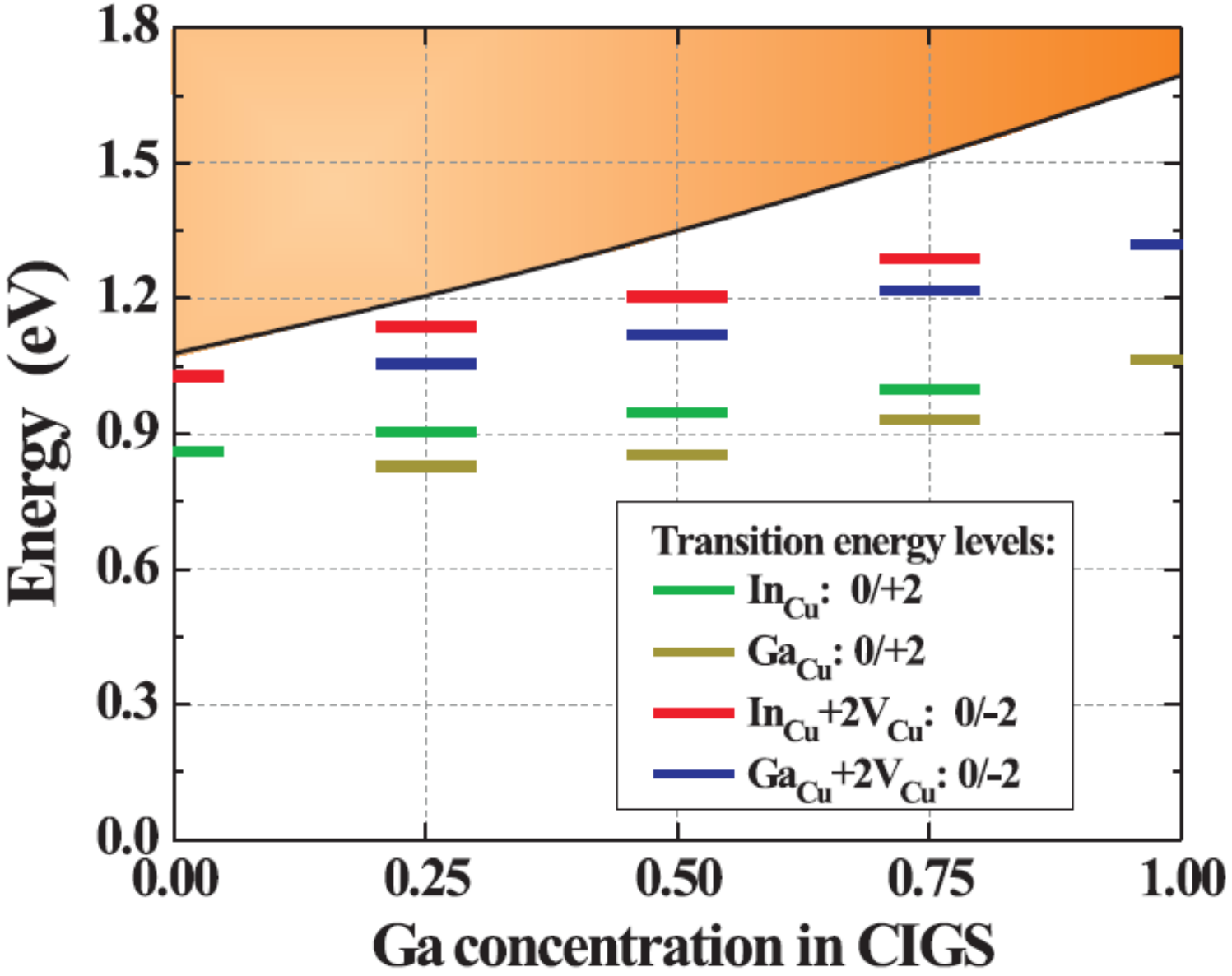
CGS



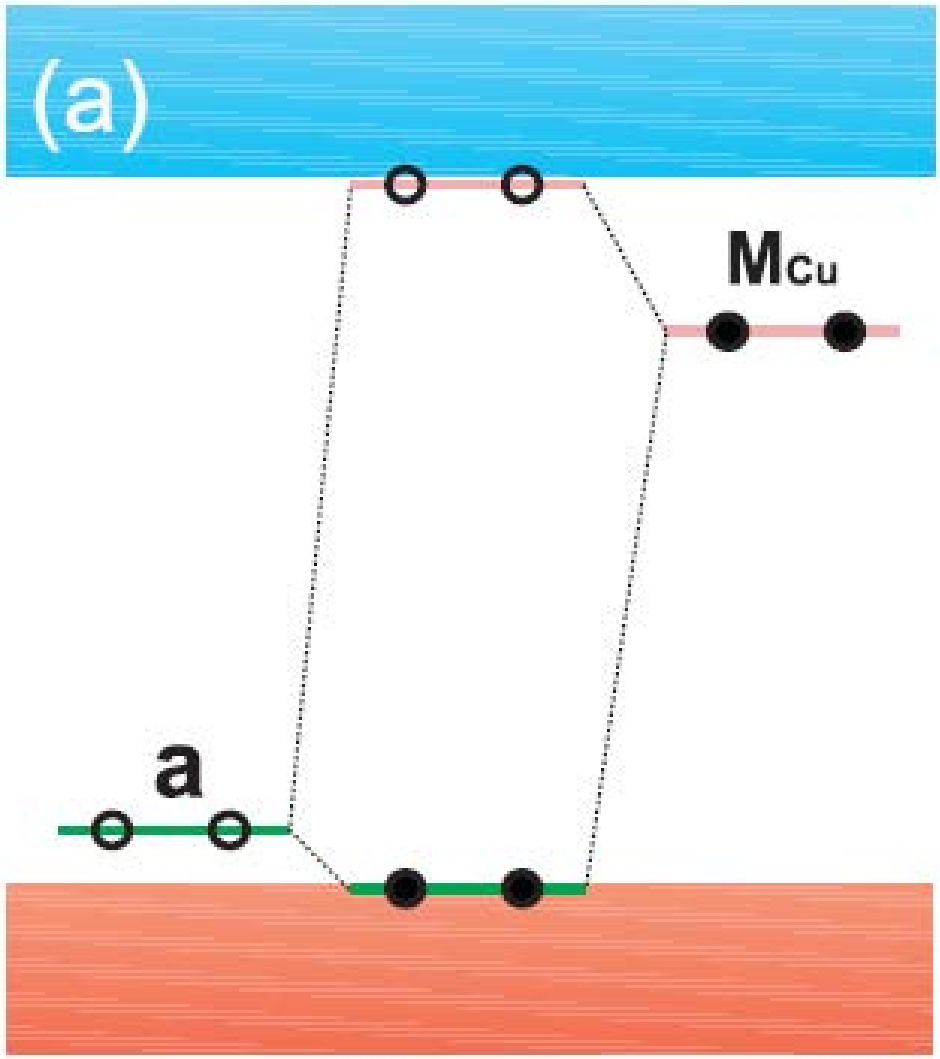


a) Cu vacancies are the main source of hole carrier density
b) Antistie defects like neutral Cu_{In} and In_{Cu} are the most important deep traps in CIS/CGS.
c) Mcu^{+2} is the most important deep traps that influences the Voc of CIGS.
d) Vse is not important.

$M_{Cu} + 2V_{Cu}$: benefit the CIGS with Ga<50%



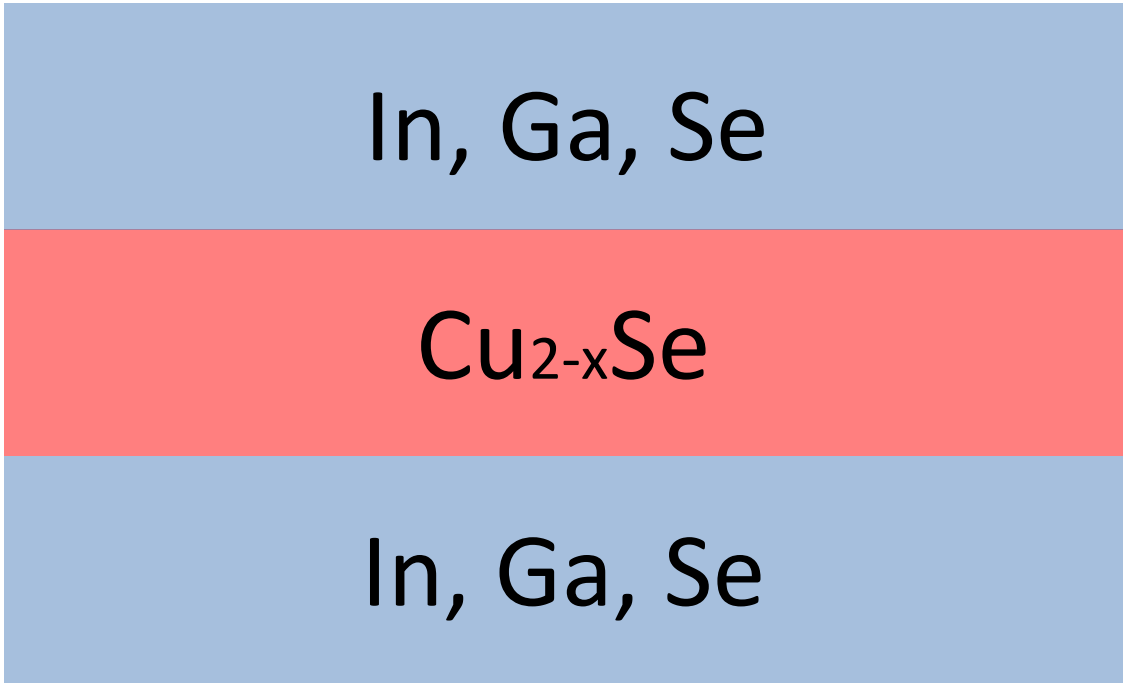
How to reduce the M_{Cu} density?



How to reduce the M_{Cu} density?

a) **Introducing $Cu_{2-x}Se$ during the growth process, which is naturally Cu poor.**

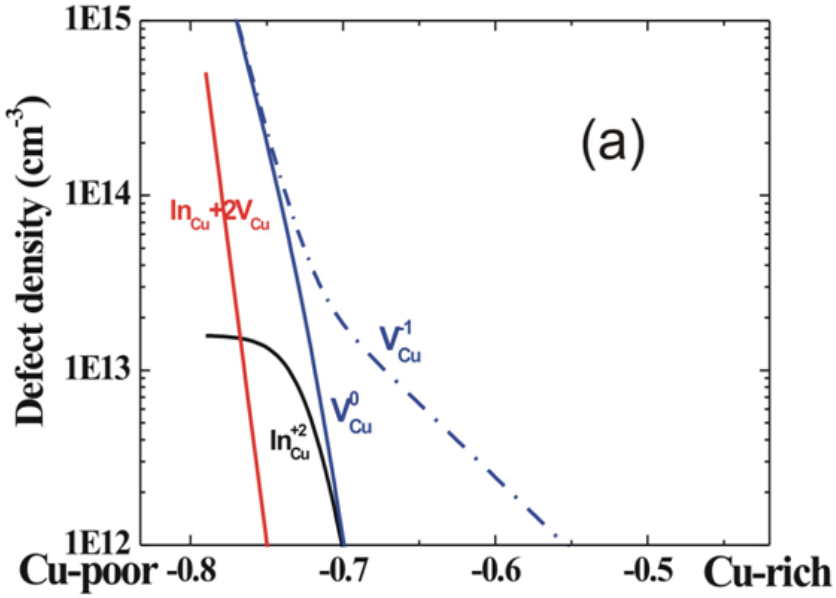
More M_{Cu} will be combined with V_{Cu} to form complexes.

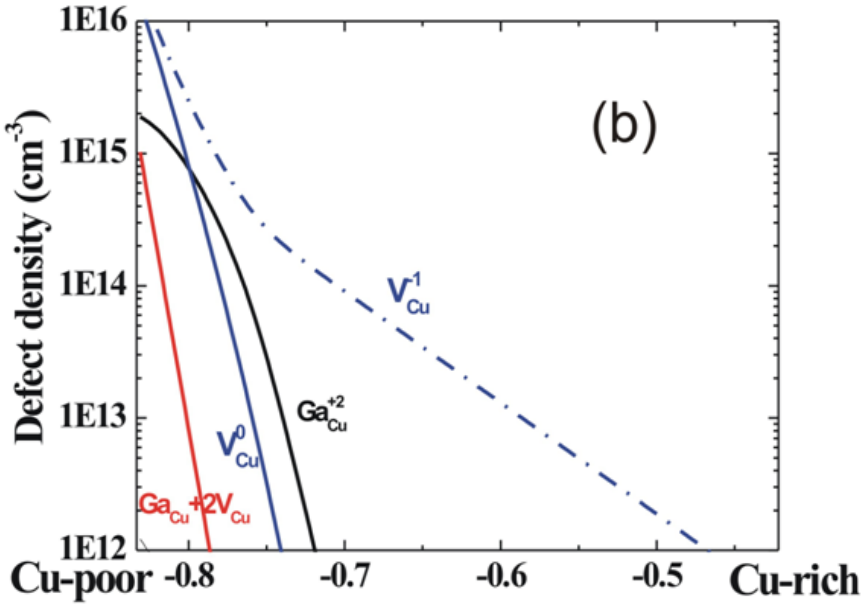


How to reduce the M_{Cu} density?

b) Lower the growth temperature (e.g., grow at 450 K, work at 300 K)

CIS **CGS**





1) The defect density of M_{Cu} is large reduced in a large range of Cu chemical potential.

2) More growth time is needed to reach thermal equilibrium.

Potential Benefits of High Eg CIGS

- High efficiency across the whole Ga range, Eg (1.1 to 1.7 eV) – easier composition control.
- A wide range of Voltage/Current combination modules.
- High band gap/high V_{oc} reduces Power Temperature co-efficient.
- Reduction of In by a factor of 2-3X.
- Open the door for a high efficiency top cell for two-junction cells.

Higher cell efficiency through higher photocurrent and lower cost through streamlined process

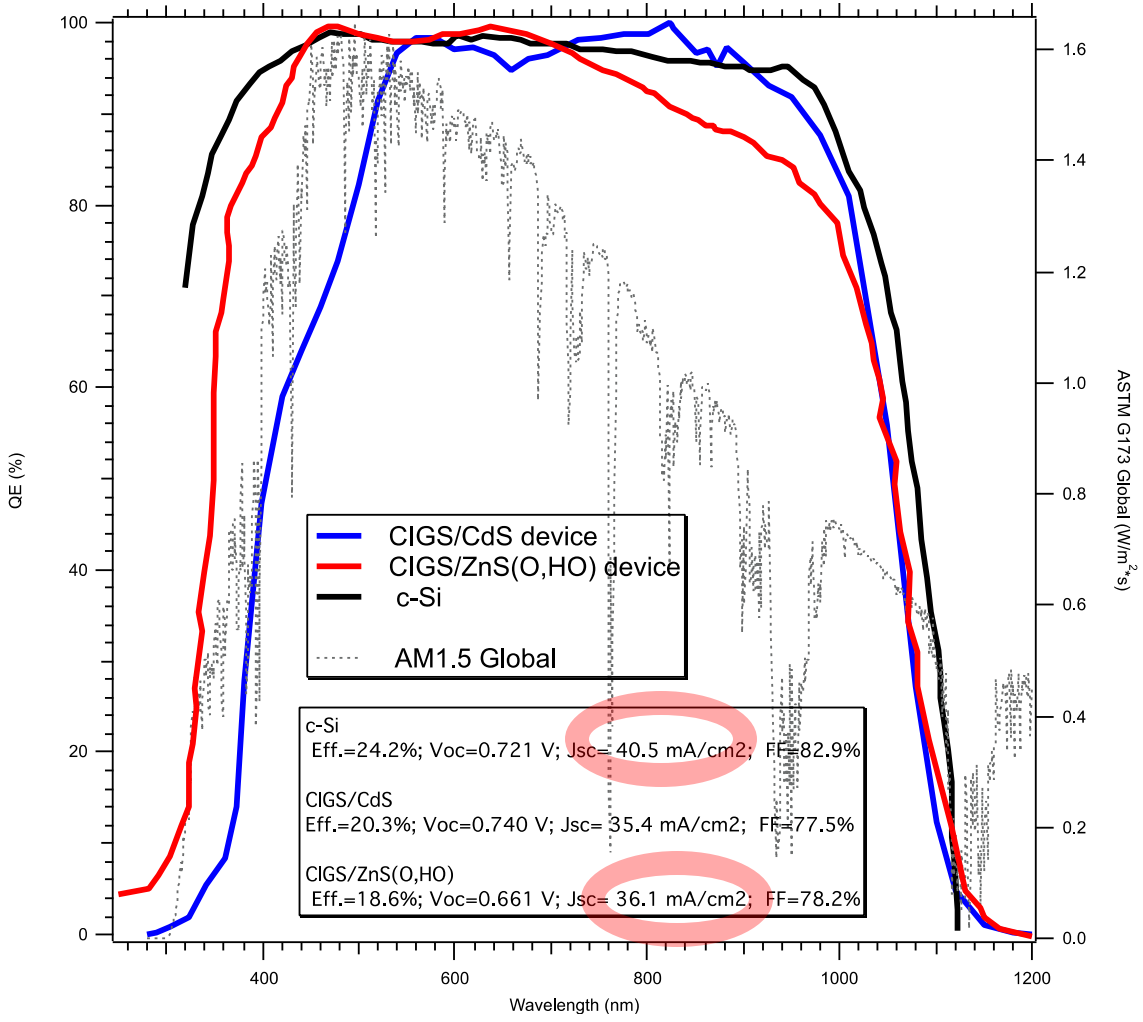
Goal: Demonstrate a >20% efficient CIGS device, using ZnO_xS_{1-x}

Relevance: The buffer/emitter layer in the CIGS device has been identified as high impact barrier for both efficiency and area related cost reduction.

Deposition methods: CBD, ALD, Sputter

The estimated cost reduction opportunity is about $0.13/W.

Higher Cell Efficiency through Higher Photo Current

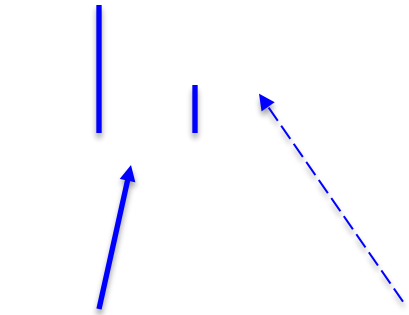


1. The best J_{sc} value obtained in the record CIGS solar cells is still quite lower than that achieved in Si (similar bandgap)
2. Great gains in efficiency could be attained if increased photocurrents are attained by maintaining V_{oc} and FF values
3. The window materials (TCOs and CdS) are responsible for the absorption of photns that otherwise could generate additional photocurrent

Best case scenario:
Potential for efficiency = 20.3% x (40.5/35.4) = 23.2%

Design of Junction Interface with ZnOS layers

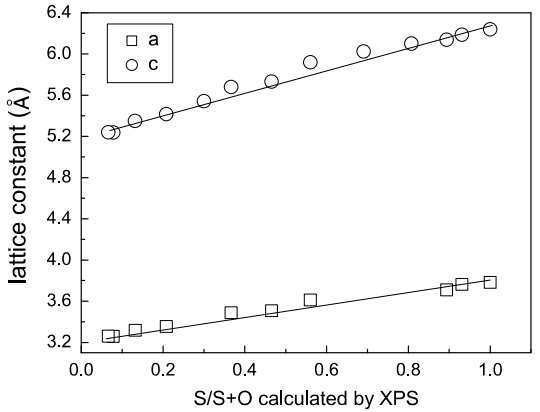
Optical Bowing in ZnOS system



Targeted range

Amorphous two-phase region

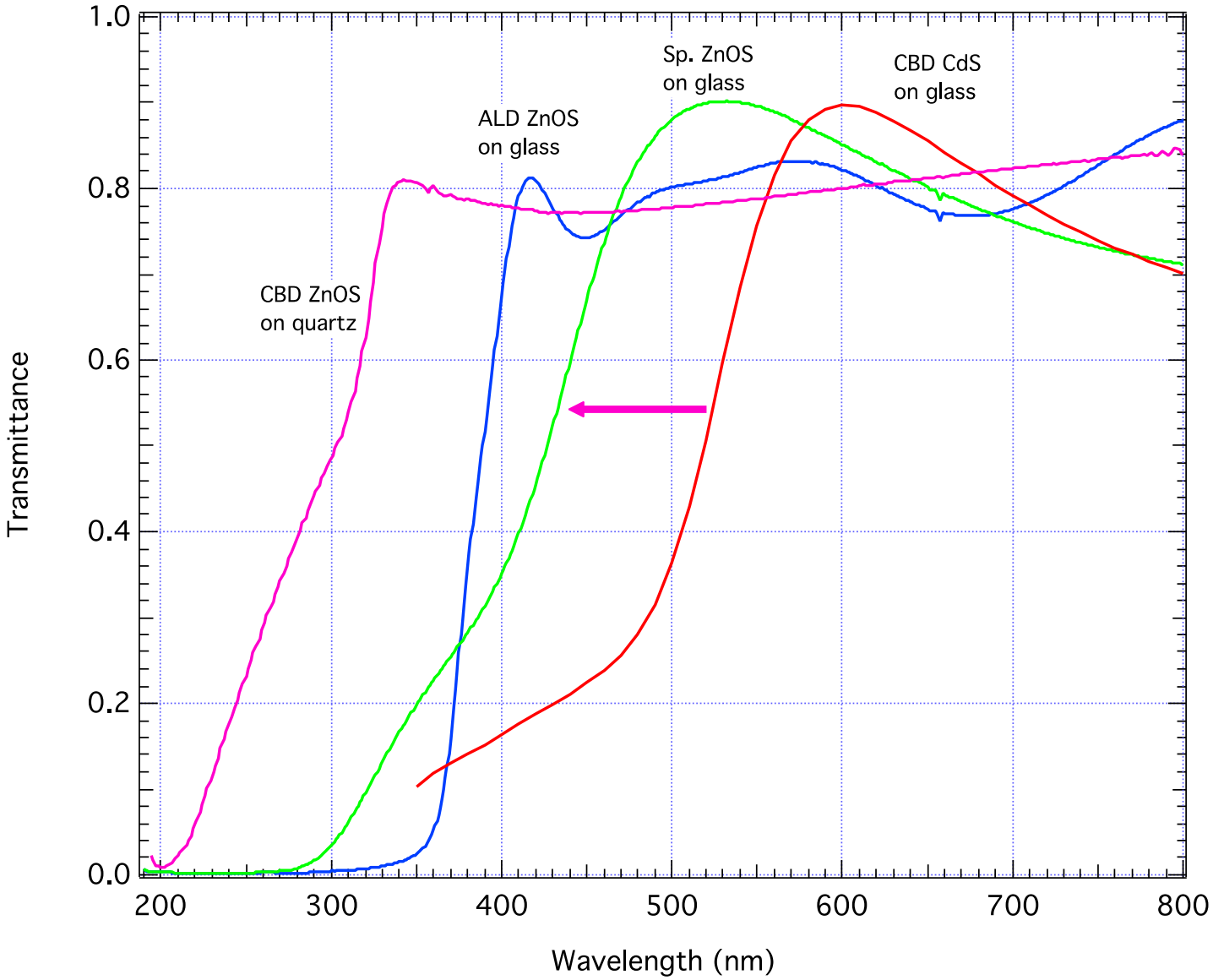
Data from sputtering, substrate temperature 200C
Grimm, et. al., Thin Solid Films 520 (2011) 1330



From published reports, we understand that:

- Pure ZnS layer blocks the photocurrent (> 1 eV conduction band spike).
- Pure ZnO layer presents a cliff and increased interface recombination.
- Optimum band gap and band offset (efficiency) can be obtained by careful choice of the alloy composition.

Transmission of ZnOS films



Approach to making efficient cells using CBD ZnOS

Build on the understanding of CdS CBD model interface.

- Simplify device structure, if possible
- Eliminate need for long heat treatments, light soaking
- Demonstrate stable, higher performing cells with higher photocurrent

Comparison of our work with two leading groups

Process step	This work	Aoyama, Japan	ZSW, Germany
ZnOS thickness	20 nm	100 nm, Repeat coating	20-50 nm
Post heating	None	30 min to hours	30 min to hours
Light soaking	None	30 min to hours	30 min to hours
i-ZnO	None	None	Need special ZnMgO
Best cell	18.5%	18.5%	19.0%

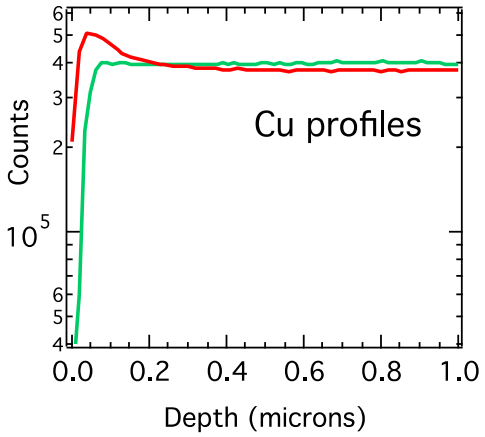
Key steps in CBD progress

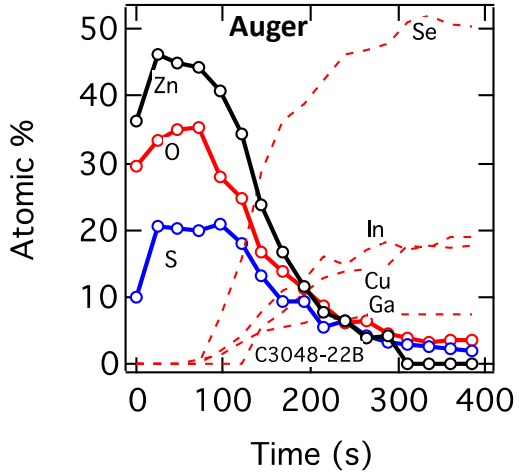
Understand absorber, control surface properties

Measure and characterize ZnOS

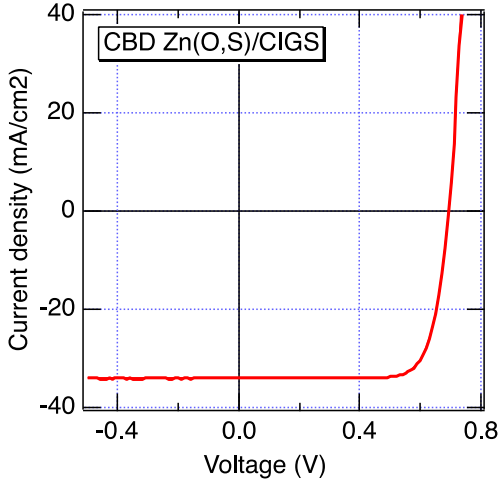
Identify key drivers

Optimize cell process





Eff (%)



V_{oc} = 0.692 V

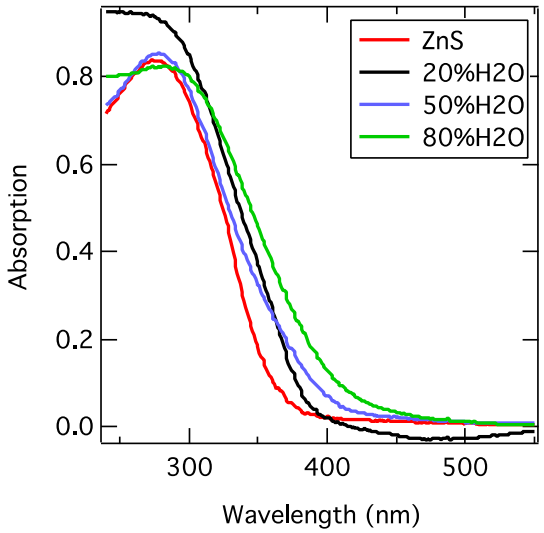
J_{sc} = 34.07 mA/cm^2

FF = 78.5%

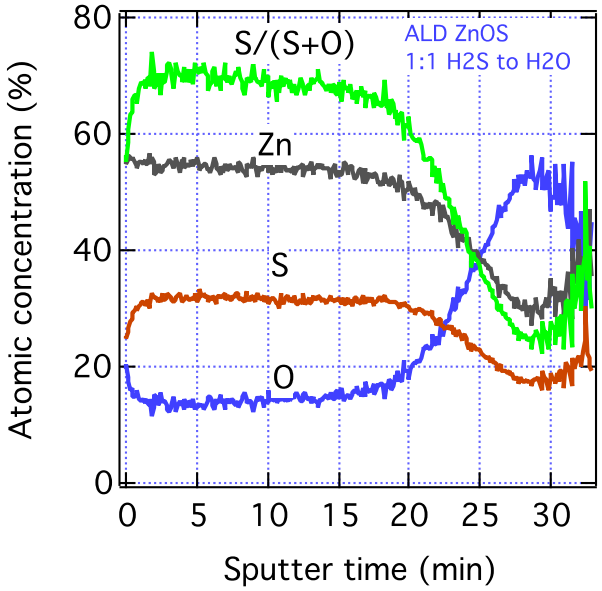
Eff = 18.5%

ALD Zn(O,S) junctions

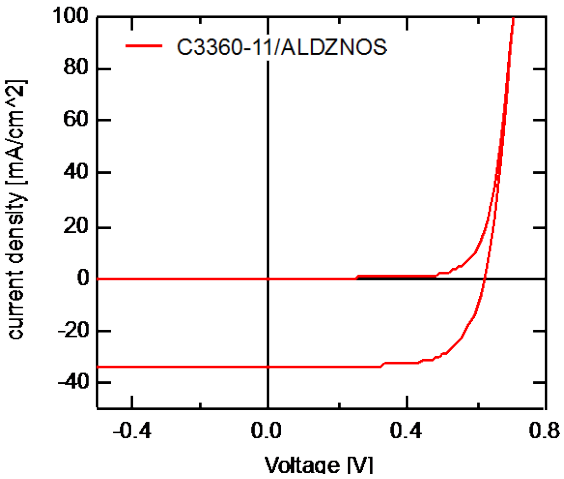
Permits precise, atomic level control of composition, grading and thickness.
Ideally suited for depositing coherent, covering, thin buffer layers.



Band gap variation
in ZnOS films



Composition

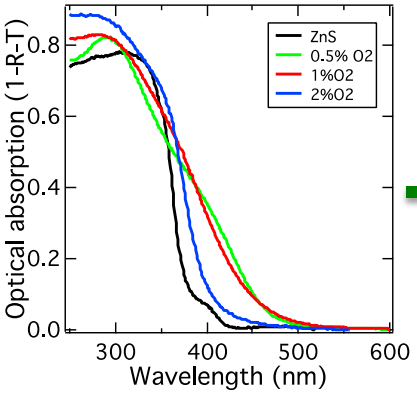


Best cell ~14.7%
No AR coat

Process optimization under way. Stretch goal: demonstrate 19% without surface treatments.

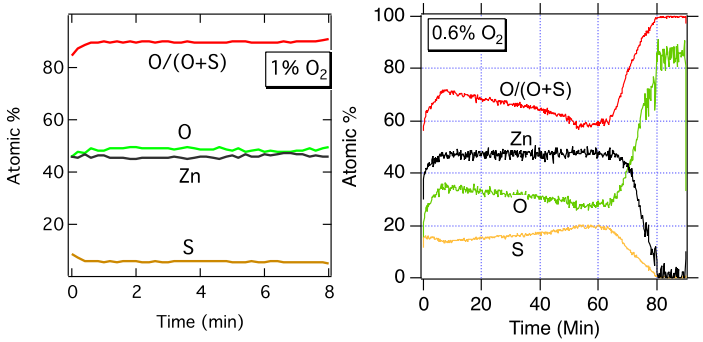
Sputter Zn(O,S) junctions

Reactive sputtering of ZnS in Ar/O_2



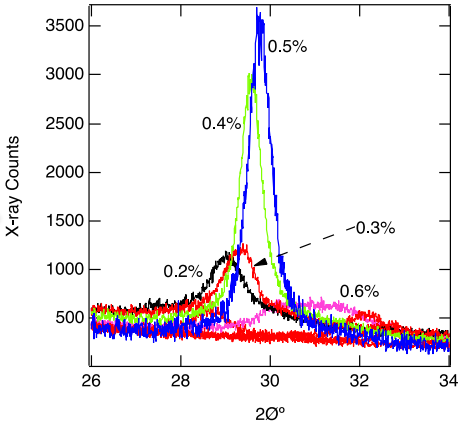
Key: Change band gap and conduction band offset with S/O ratio

Measure S/O ratio



Optimize cell performance (sputter parameters, O_2 etc)

XRD

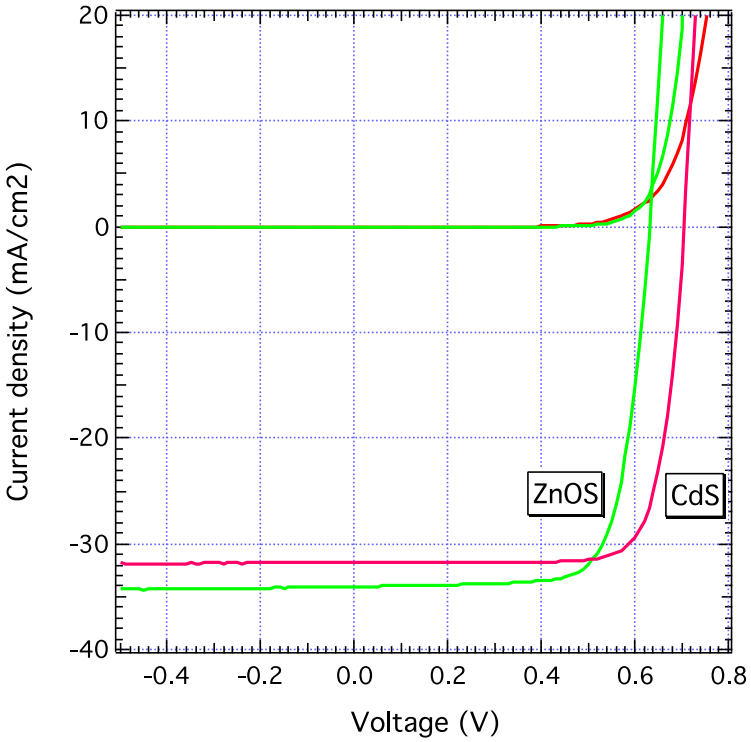


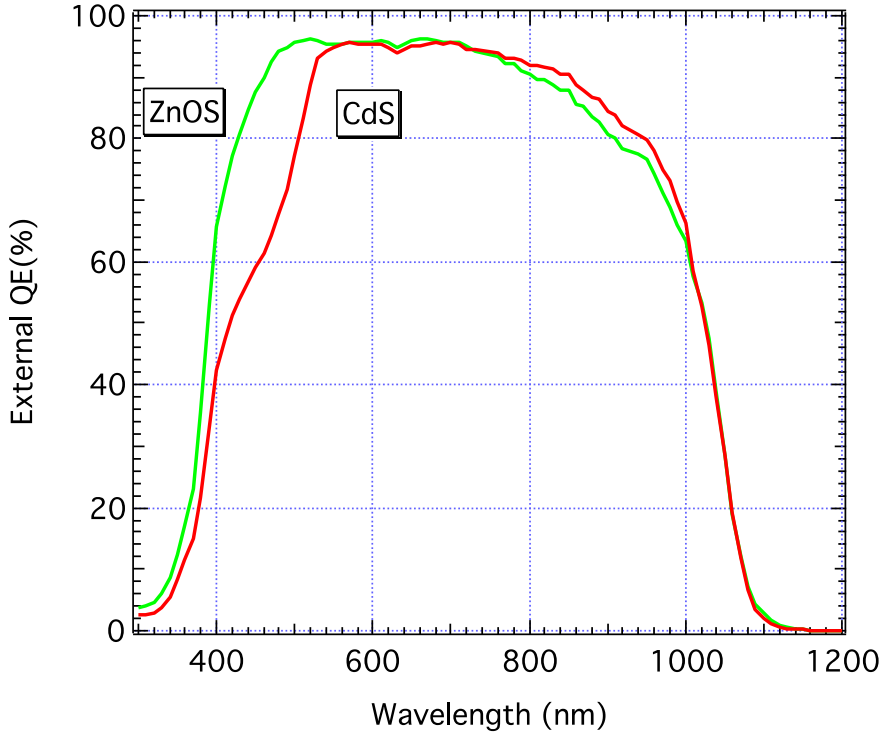
Intensity, FWHM correlate with efficiency

Eff(%)

Advanced characterization
Interface: UNLV, NREL
Cell: Colorado State

Best result from sputtering





Emitter	V_{oc} (V)	J_{sc} (mA/cm^2)	FF(%)	Eff(%)
CBD CdS C3272-21-6	0.706	31.8	78.6	17.65
Sputter ZnOS C3272-22-6	0.666	34.3	73	16.6

Achieved expected current gain of > 2 mA/cm^2

Opportunities

Efficiency Opportunities - CIGS

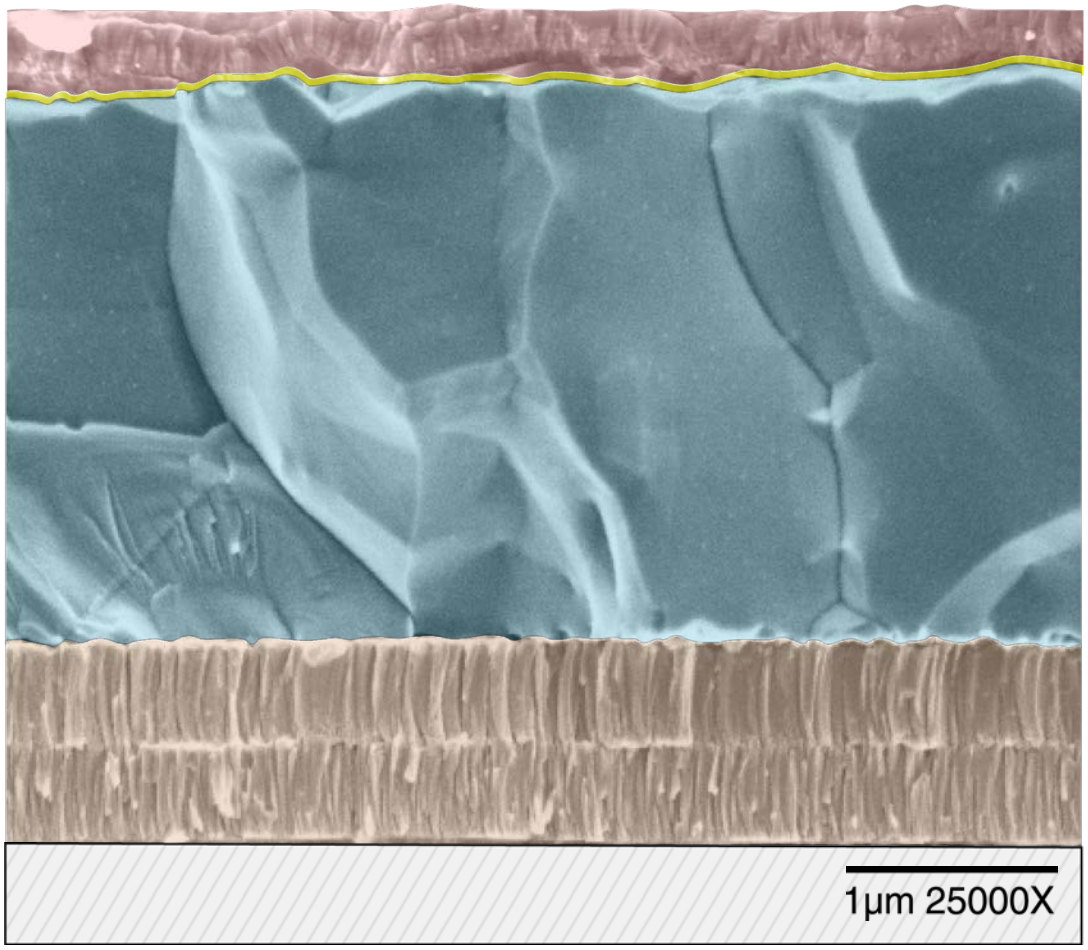
	Short Circuit Current (mA/cm^2)	Open Circuit Voltage (volts/cell)	Fill Factor	Efficiency (%)
Practical Potential[+]	30.0 - 39.0	0.75 - 0.95	0.83	25.0
Best laboratory cell	35.4	0.74	0.78	20.4
Commercial cells[*]	30 (32.5)	0.60 (0.69)	0.70 (0.73)	13 (15.7)

[+] Ranges reflect variation in bandgap (i.e., Ga/In ratio)

[*] Values in parentheses are from hero modules

Future Opportunities and Challenges

Today	Front Contact Grid	Forward
	• Screen Print Ag	• Reduce shadowing • Faster application
ZnO, ITO (2500 Å) • Sputter		Hardened TCO (moisture barrier)
CdS (700 Å) • Chemical Bath Deposition • Sputter		Cd-free; dry, eliminate
CIGS (1-2.5 µm) • Multiple methods (coevaporation, sputtering, printing, electrodeposition)		Increase Ga-%, Reduce thickness, Rapid deposition Uniformity (composition, temp., thickness)
Mo (0.5-1 µm) • Sputter		Na dosing
Glass, Metal Foil, Plastics		High temp. glass Metal foils: smooth, flex-dielectric (monolith.)



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Pathways to increase CIGS Open Circuit Voltage from commercial (0.63 V) to best lab cell (0.80 V)

Action	Potential Voltage Increase (V)	Technical Risk	Pathways
Improve the absorber carrier lifetime and concentration	0.05	Medium	Implement in-situ quality control at minimal additional cost
Increase the Ga/In ratio in CIGS by a factor of 2 to 3	0.1	Medium	Increase CIGS deposition temperature via higher temperature glass substrates or alternative stable substrates.

Pathways to increase CIGS Short Circuit Current Density from commercial (30 mA/cm^2) to best lab cell (36 mA/cm^2)

Action	Potential Current Increase (mA/cm^2)	Technical Risk	Pathways
Reduce CdS window layer thickness	1.5	Medium	Develop 20 nm thick continuous CdS layer without shunting.
Larger band gap junction partner	2.5	Medium	Replace CdS (e.g. 2.5 eV) with wide bandgap emitter (i.e., ZnS (3.4 eV))
Improved TCO	1.5	Medium	Develop TCO with high conductivity, transparency, environmental stability (i.e., a-InZnO)
Improved monolithic integration	1	Low	Reduce line width of laser/mechanical scribing
Minimize reflection off CIG surface	1.5	Medium	Develop a suitable low cost anti-reflection coating

Pathways to increase CIGS fill factor from commercial (0.69) to best lab cell (0.82)

Action	Potential FF Increase	Technical Risk	Pathways
Reduce contact resistance	0.07	Low	Improved TCO and contact grid combination
Reduce parasitic leakage current	0.10	Low	Improve the density, phase, and crystallinity of the absorber

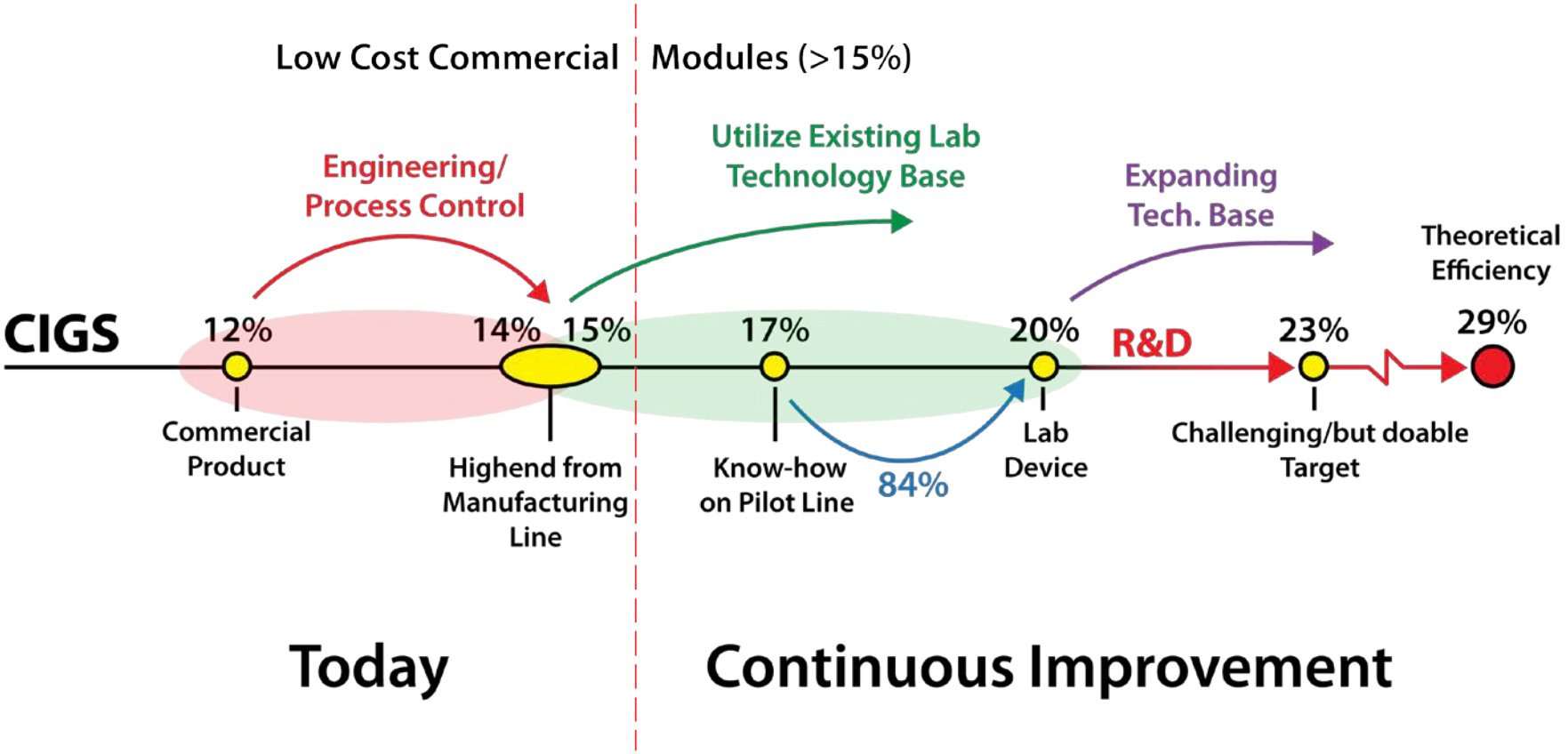
Cost drivers per area - CIGS

Drivers	Cost Reduction Potential	Technical Risk	Pathways
Materials cost and availability (Indium, selenium, cadmium)	High	Medium	Thinner layers or replacement with Earth abundant and benign materials (e.g., CZTS, ZnS, …)
Transparent Conductors	High	Low	ITO alternative materials and/or deposition methodologies
Glass and/or Encapsulants	Medium	Medium	Flexible low-cost front and backsheets with low WVTR (i.e., ultrabarriers, glass replacement)
Operational costs of selenization ovens	Medium	Medium	Eliminate batch selenization, alternative deposition methodologies (e.g., atmospheric deposition).
Large scale spatial uniformity and improved throughput with same or lower cost of capital	High	Medium	Improved In-situ metrology, thermal control, and elimination of chemical bath CdS

Potential

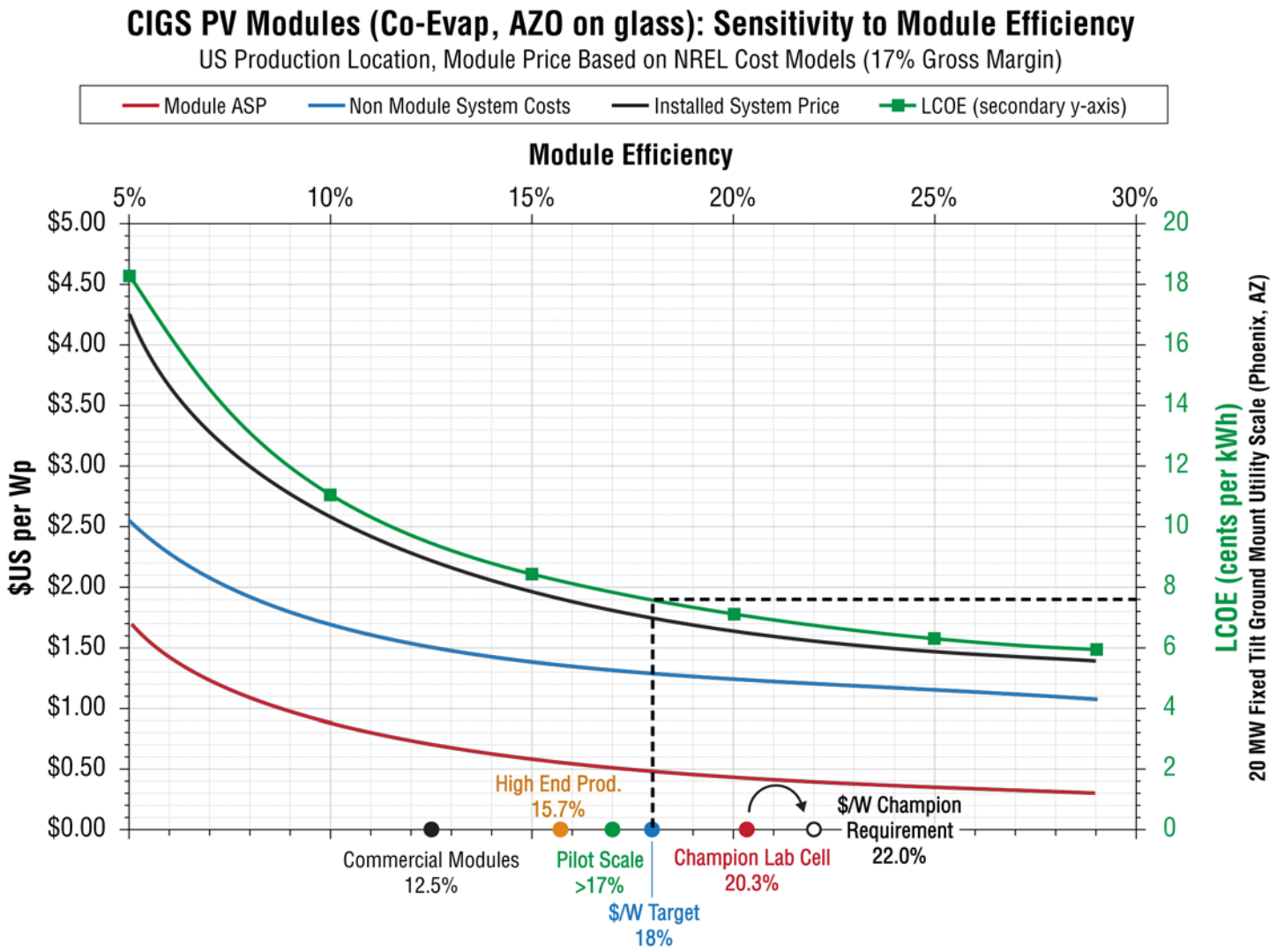
Closing the Gap between Laboratory Cells and Modules

Future commercial module performance target: Module/Cell Ratio >80%



Primary Focus: Utilizing Lab Technology base to translate results to manufacturing

The Value Proposition for High Efficiency CIGS

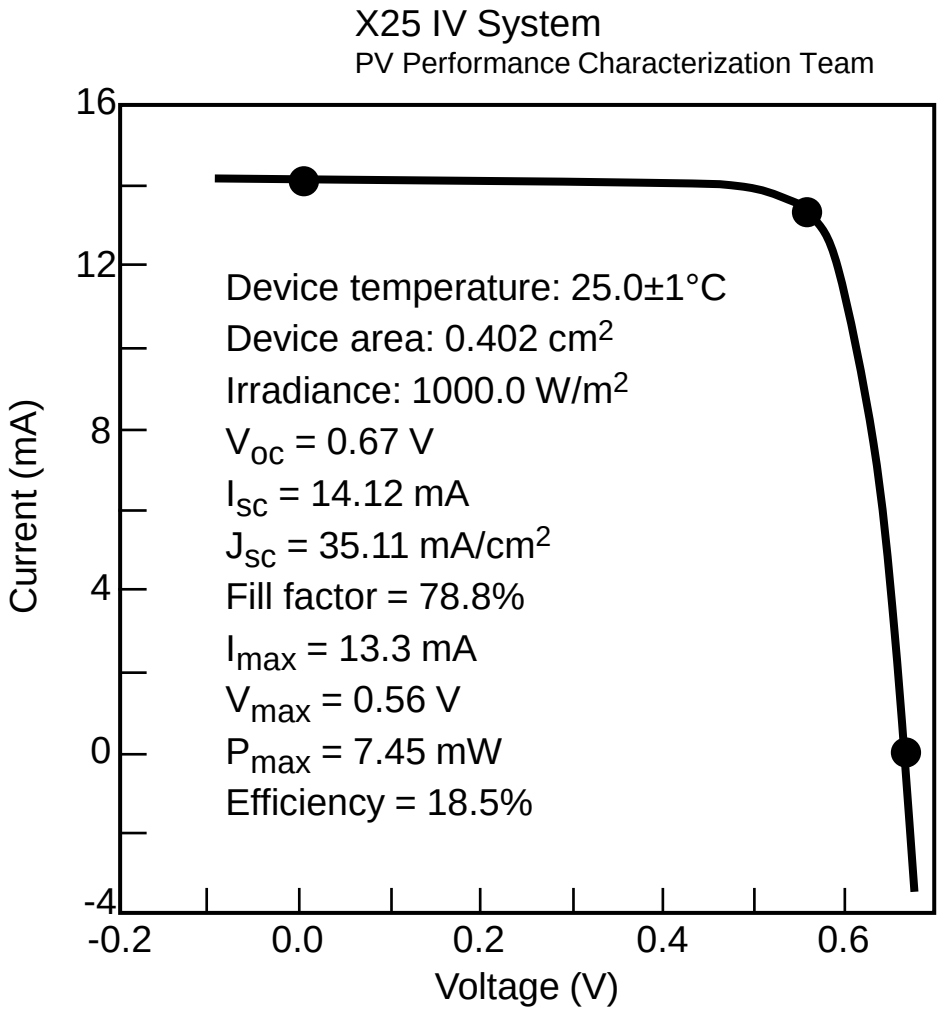


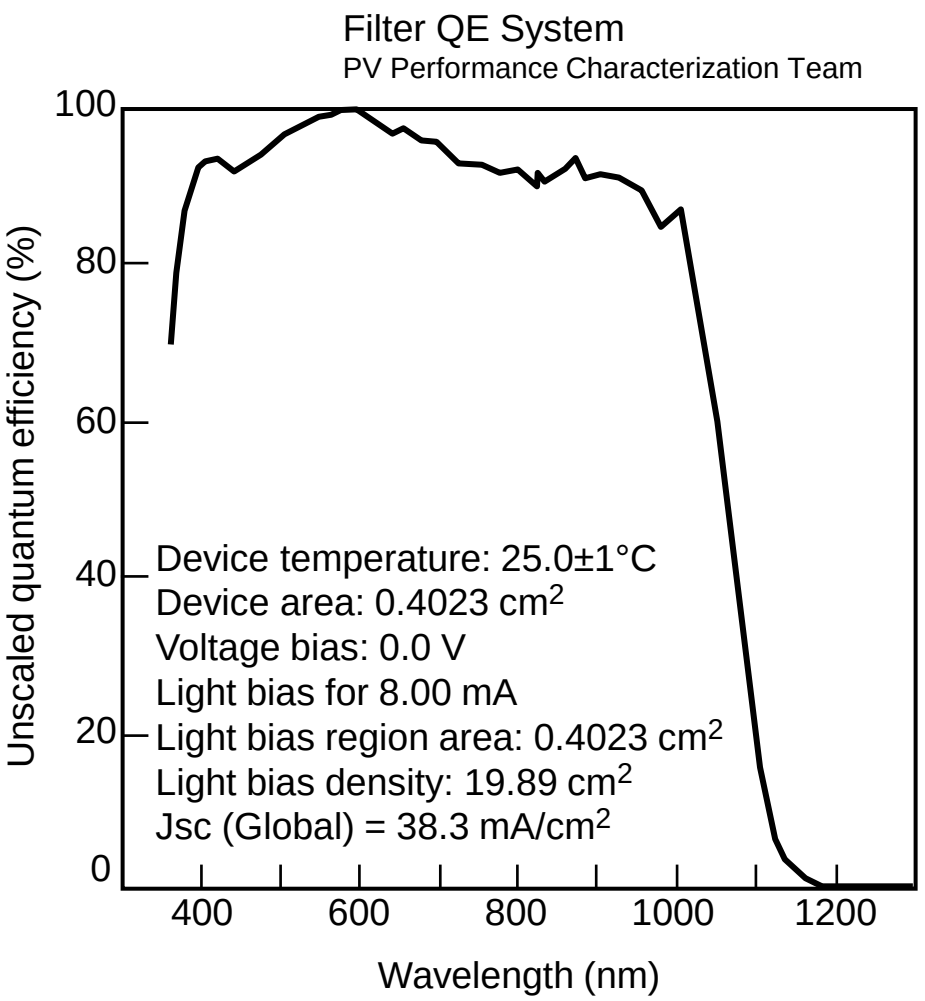
- At no added cost ($/m^2), 17.5% CIGS module = ~$0.50/Wp module ASP target
- New champion lab cell efficiency (≥22%), BoS improvements are required

END

Happy to share the presentation with you

18.5% Device using NREL's Single Layer CBD ZnOS

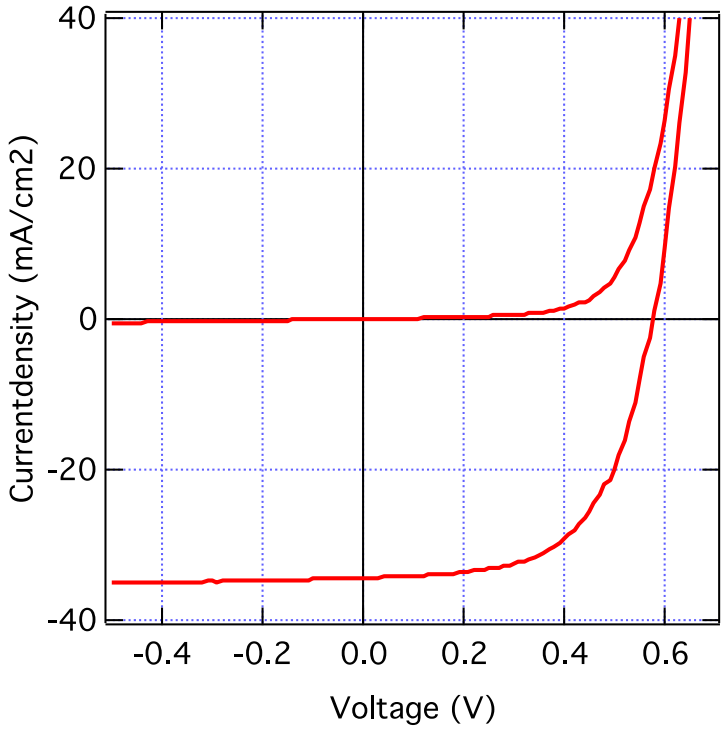




Expected effects: A tactical approach

Junction process	*Surface condition/ changes (chemical)*	*Surface condition/ electronic*	*Work to be done*
CBD	Etching, native oxide removal	N-type doping by Cd or Zn	Good model, but effects must be quantified to serve as a basis for other devices
ALD	Does it occur? Can it be induced?	Can we control the n-type doping?	Can we use ALD to tailor interfaces in wide gap CIGS?
Sputtering	Diffusion of elements, mixing at interface? Abrupt or graded interface?	Additional defect states because of ion bombardment? Oxygen induced surface states?	Suspected effects need to be verified. Solutions for performance improvements demonstrated.

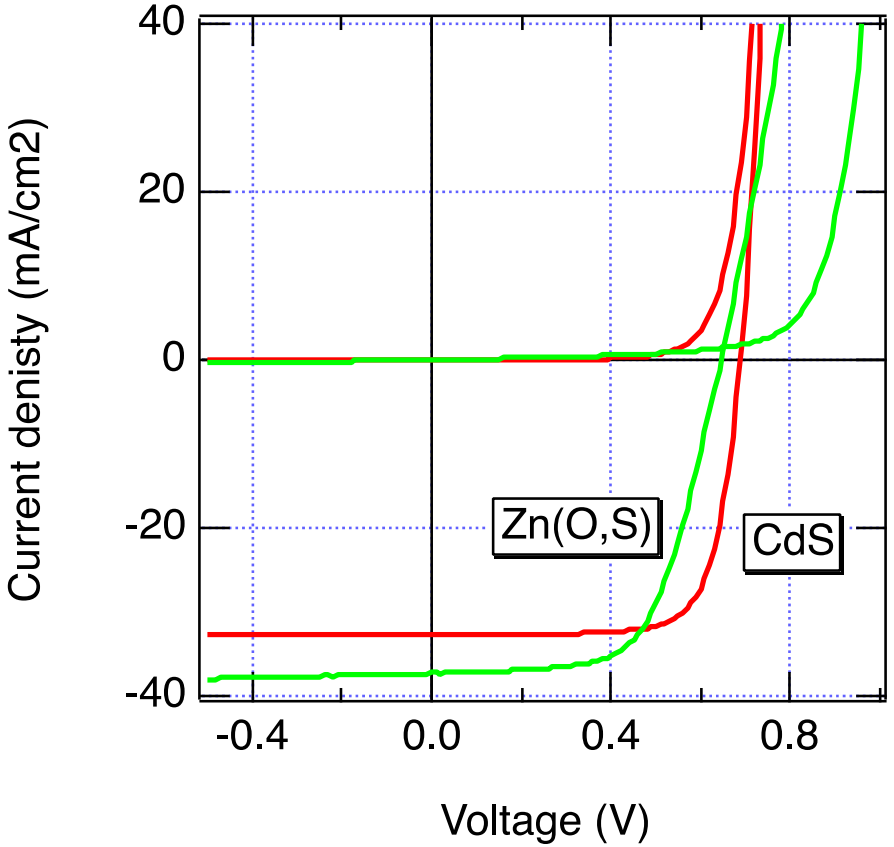
Best ALD result to date

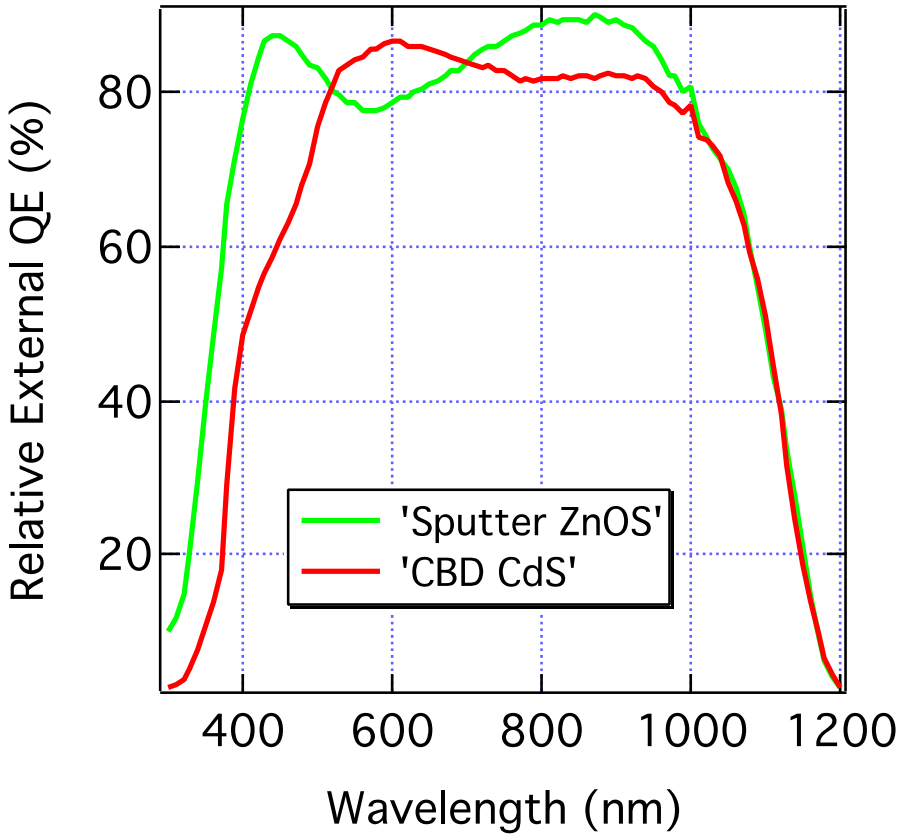


Buffer type	CBD CdS	ALD ZnOS
V_{oc} (V)	0.681	0.581
J_{sc} (mA/cm^2)	32	34.38
Fill factor	0.745	0.59
Efficiency (%)	16.2%	11.8%

- ~ 12% cells, early stages of process development and optimization
- Need to perform loss analysis and address interface issues.

Best result to date with sputtering





Zn(O,S) cells ~ 14 to 15% range, within 1% of CBD CdS cells. V_{oc} loss: 50 mV, FF loss: 10 abs %.

Superior response in 400 -500 nm (CdS region)
Better transmission of TCO in Zn(O,S) cell, AZO only.
Red response is also good.

Summary

We have made rapid strides in the development of ZnOS based junctions using three vastly different approaches: CBD, ALD and sputter.

Process robustness and sources of variability are under investigation. Direct impact to industry expected.

Focus is on the electronic properties of critical interfaces as affected by the specific process.

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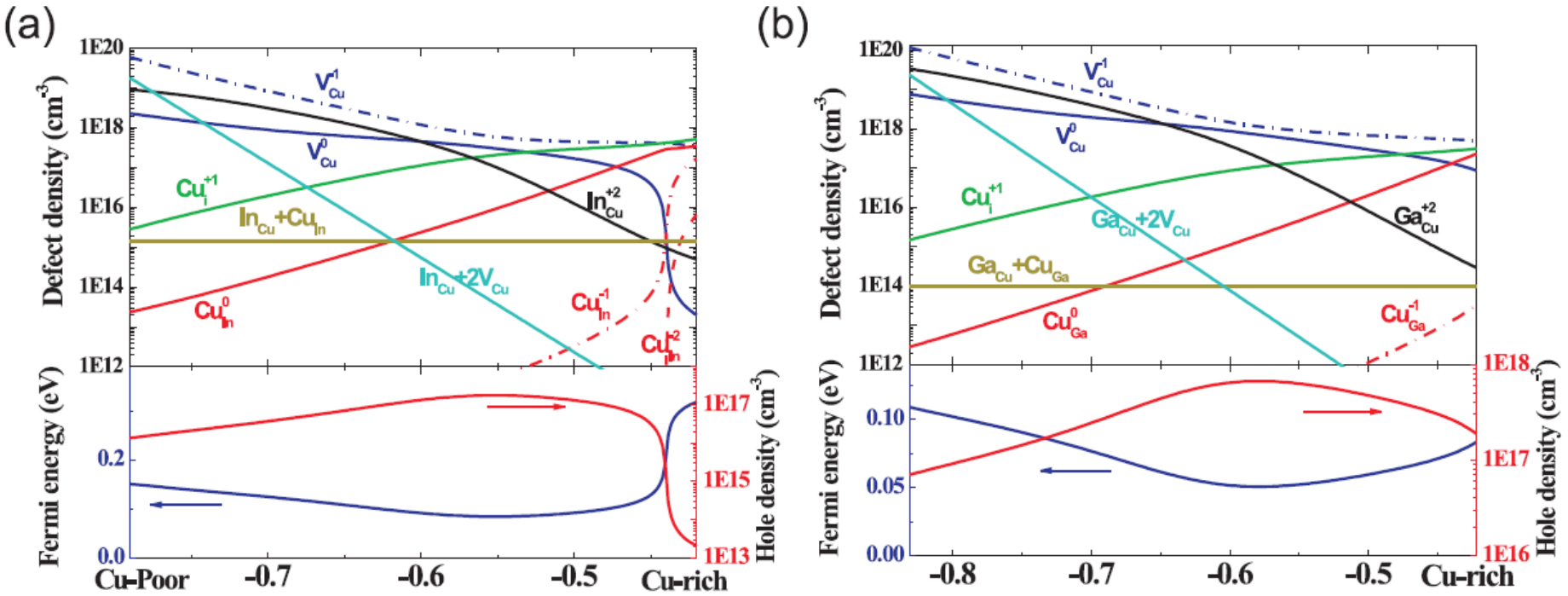
Origin of Reduced Efficiency in Cu(In,Ga)Se2 Solar Cells with High Ga Concentration

Hybrid functional method may be necessary to reexamine the defect properties in CIGS

Previous calculations suggest that HSE can describe the band gap of most semiconductors well (*not good for surface and low-dimensional materials, Louie at al 2011*)

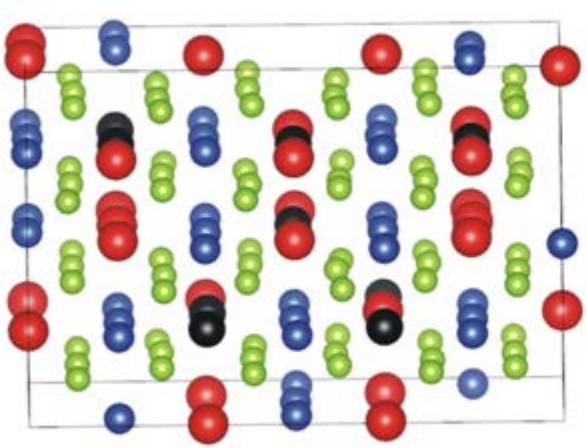


Under equilibrium condition, the density of M_{Cu} is quite high and can not be largely converted into the netural defect complex.

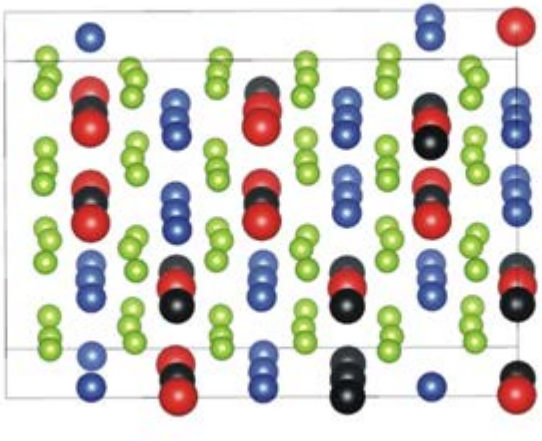
How to deal with it?

The trend of M_{Cu} in CIGS: SQS

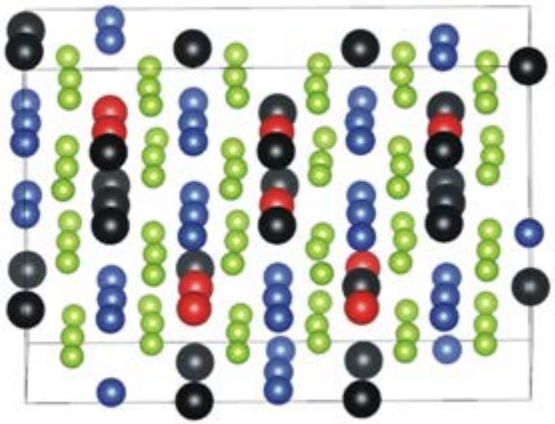
In/Ga



In/Ga



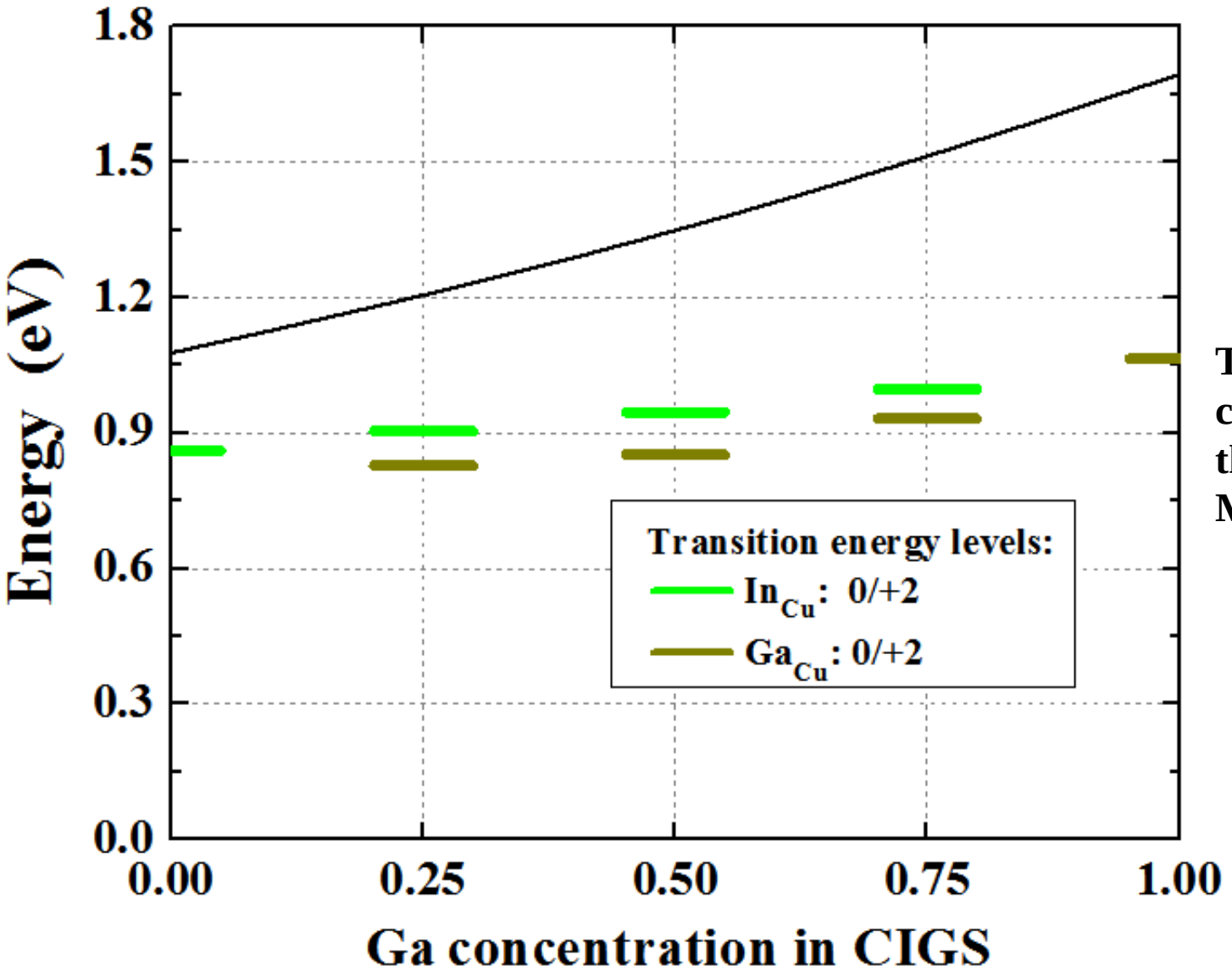
In/Ga



Ga concentration:

0.25 **0.50** **0.75**

The trend of Mcu in CIGS: 0/+2



The more the Ga concentration, the deeper the M_{Cu} level.

Rapid two-step Selenization of CIGS films

Goal: Demonstrate the fabrication of a >20% solar cell by the two-step selenization with reaction time <10 minutes as compared to hours (practiced by industry).

Relevance: This task represents a medium cost reduction potential opportunity on area-related basis with low technical risk. The cost reduction estimate is about $\$24/m^2$ to $\$14/m^2$.

Rapid Two-step Selenization of CIGS Films

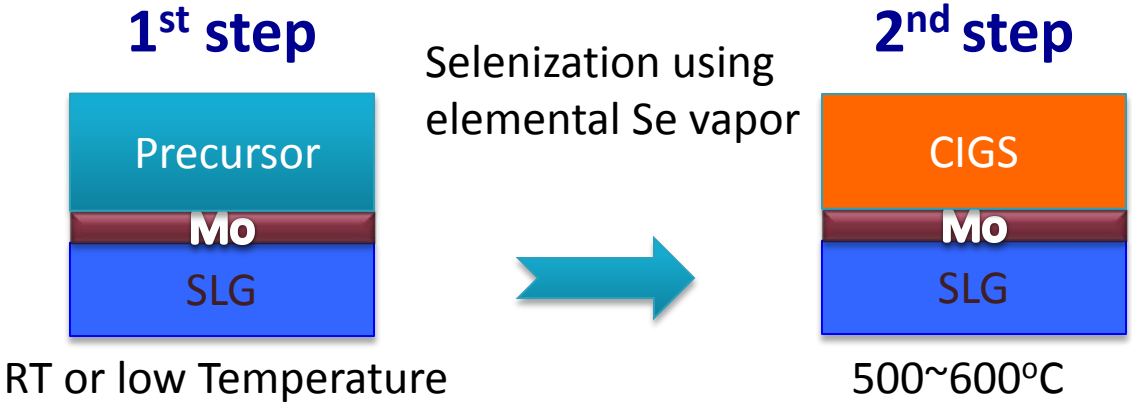
1. Two typical questions are usually asked by industry.
   a. What is the best precursor structure and morphology for the selenization reaction?
   b. What is the best selenization reaction pathway to form the CIGS film such that the Ga profile is flat and hence the film is homogeneous?
2. To answer both interdependent questions, we propose to study the reaction pathway to rapid selenization of the Cu/In/Ga stack in Se vapor to understand the reaction diffusion kinetics, from which we can specify the conditions for thorough inter-diffusion resulting in homogeneous films.
3. The major change involves reducing the reaction time to < 10 minutes and replacing the H_2Se/H2S gases with elemental Se.

Goal: Demonstrate the fabrication of a >20% solar cell by the two-step selenization with reaction time < 10 minutes

Approach

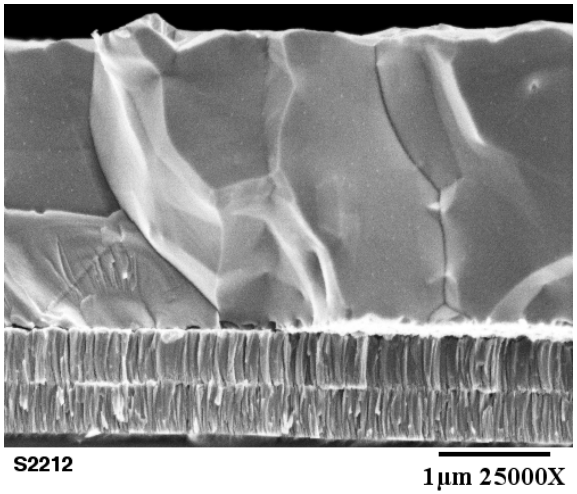
Simple, fast, and high-efficiency

- Concepts of the new two-step process in this study
  - Industrially applicable fast and high-efficiency CIGS processing
  - No use of H_2Se & H_2S gases. Only Se vapor
  - To understand the reaction kinetics in order to find the best precursor structure & the optimal selenization conditions

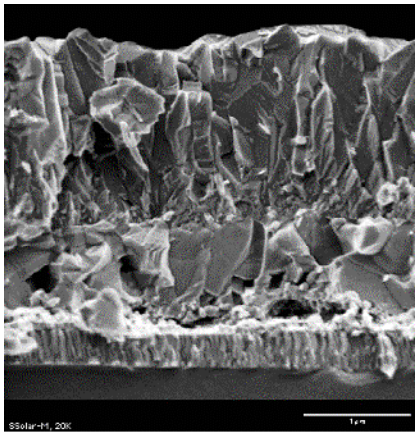


Ultimate goal⇒ High cell efficiency (>20%), Short reaction time (<10 min.)

Comparison of NREL and Commercial CIGS films made by two-step selenization

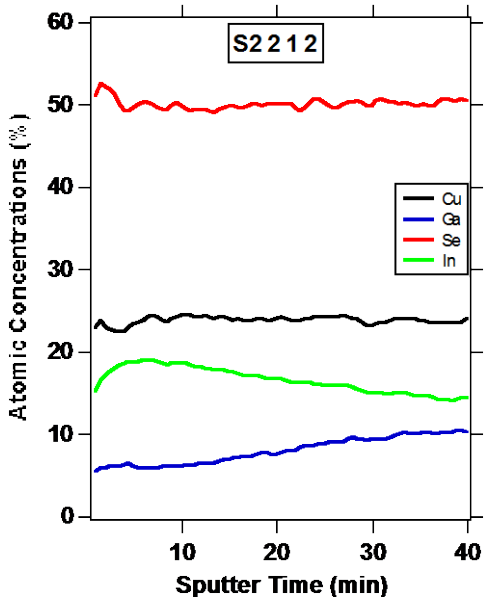


Transform



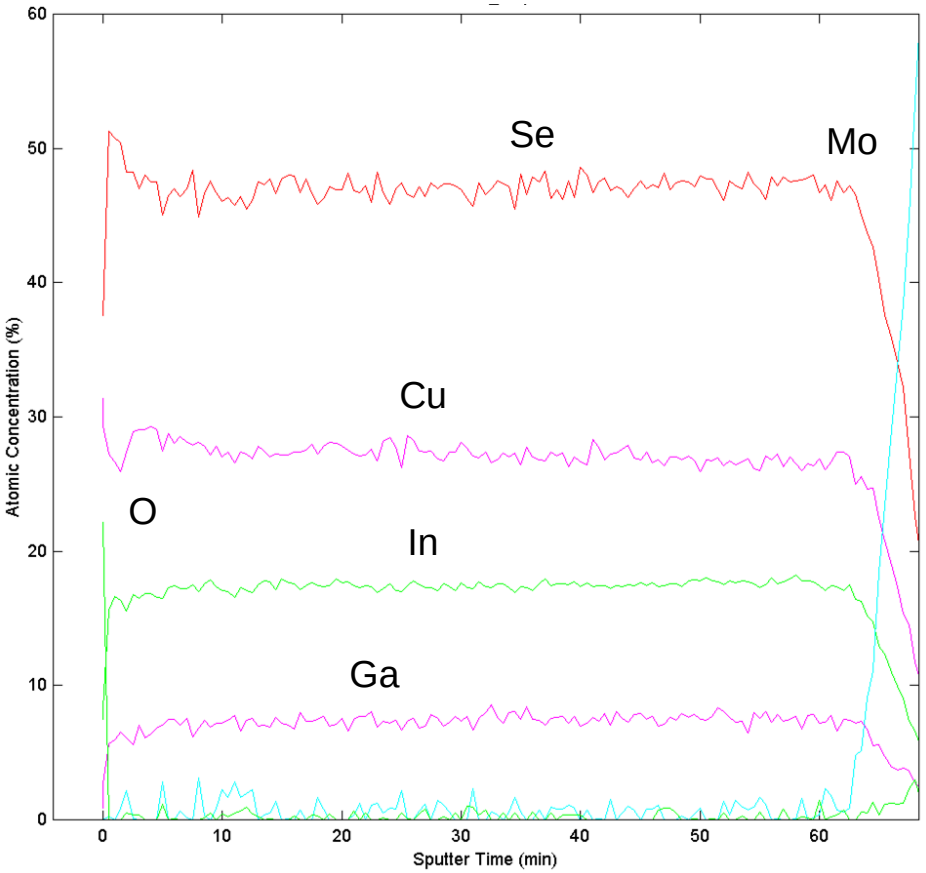
ZnO

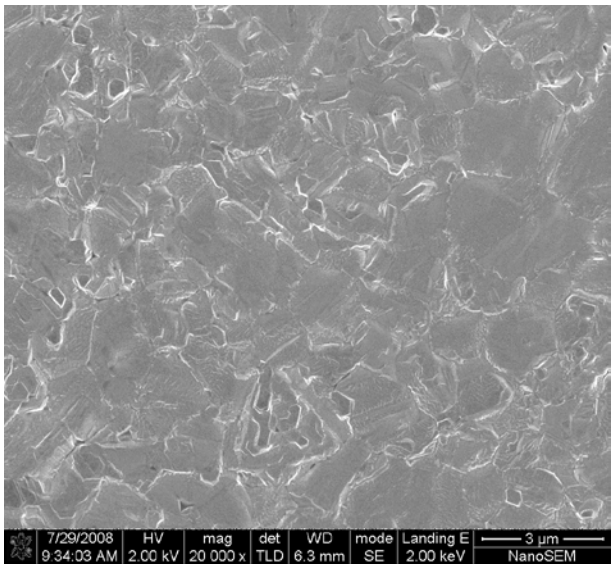
CIGSeS

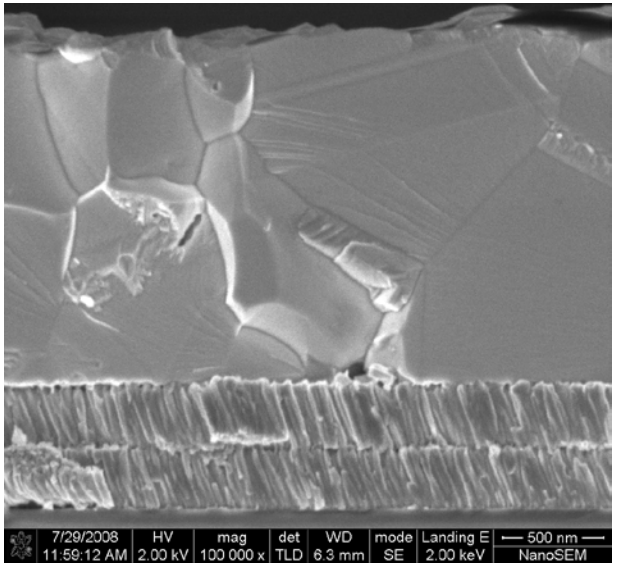


Transform

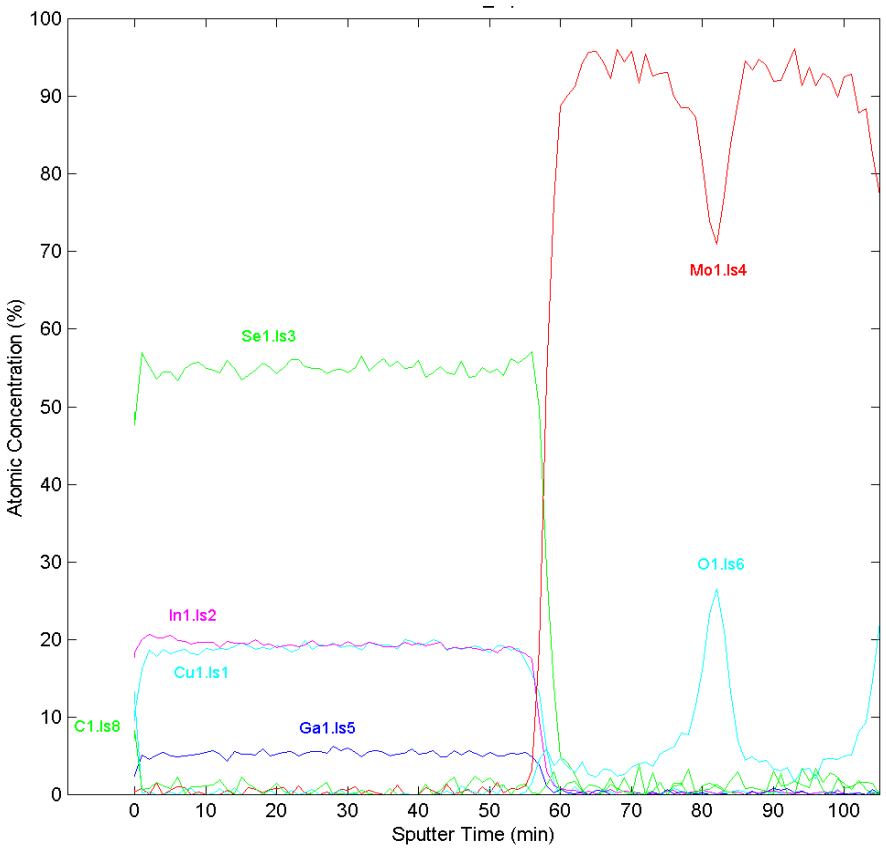
Dynamics of Growth Pathway

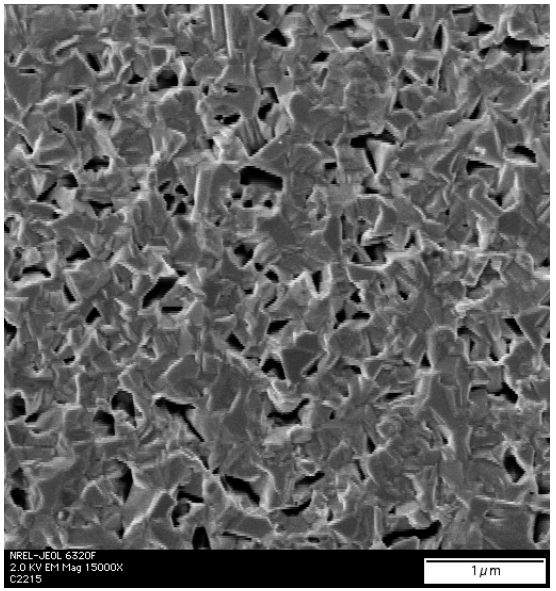


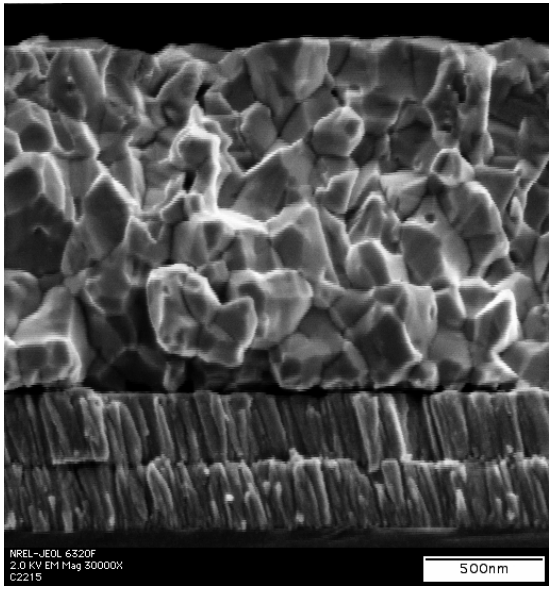




Dynamics of Growth Pathway



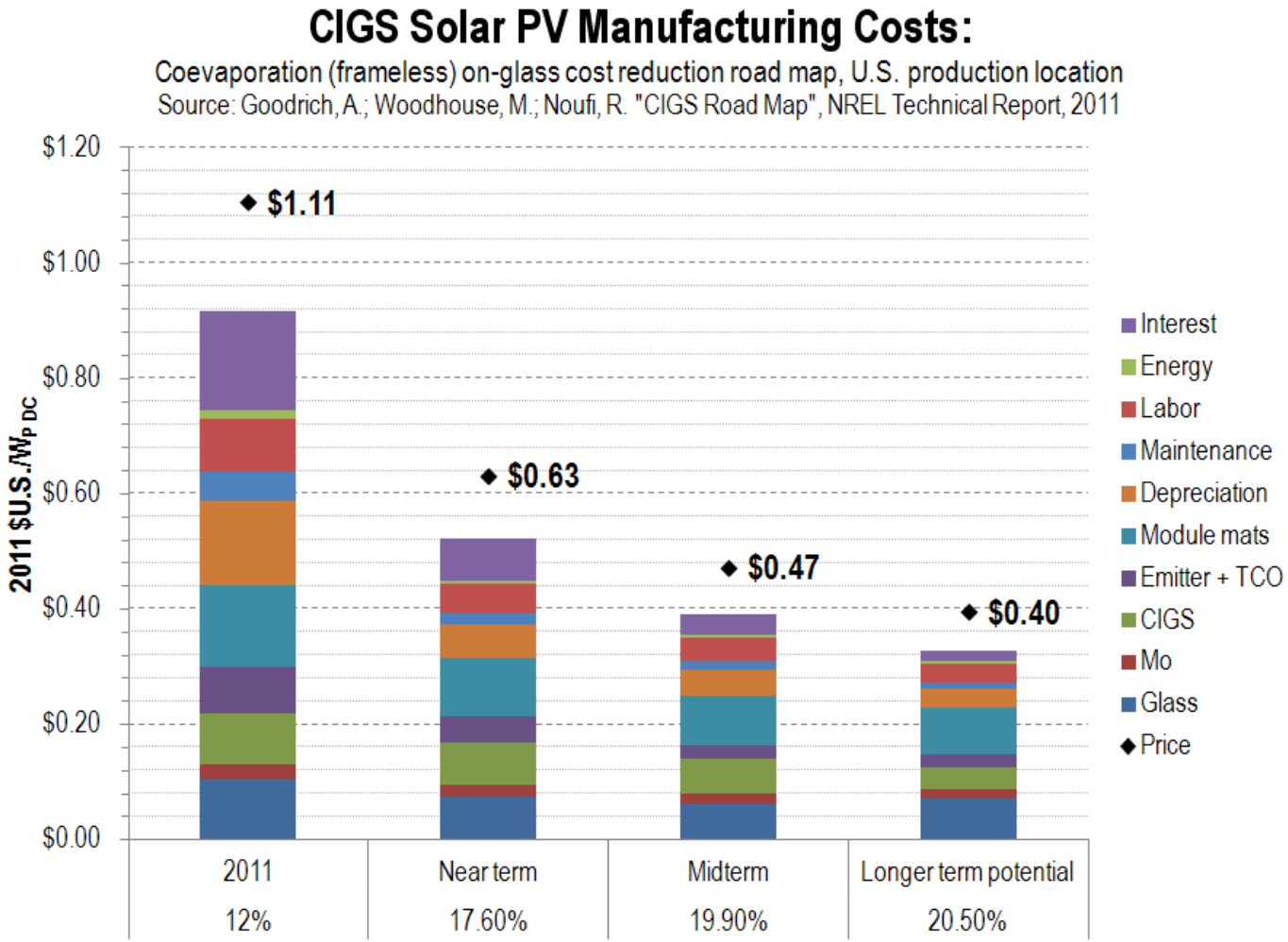




Voc=0.6 V, Jsc = 35.0%, FF = 72%

Efficiency = 15.1%

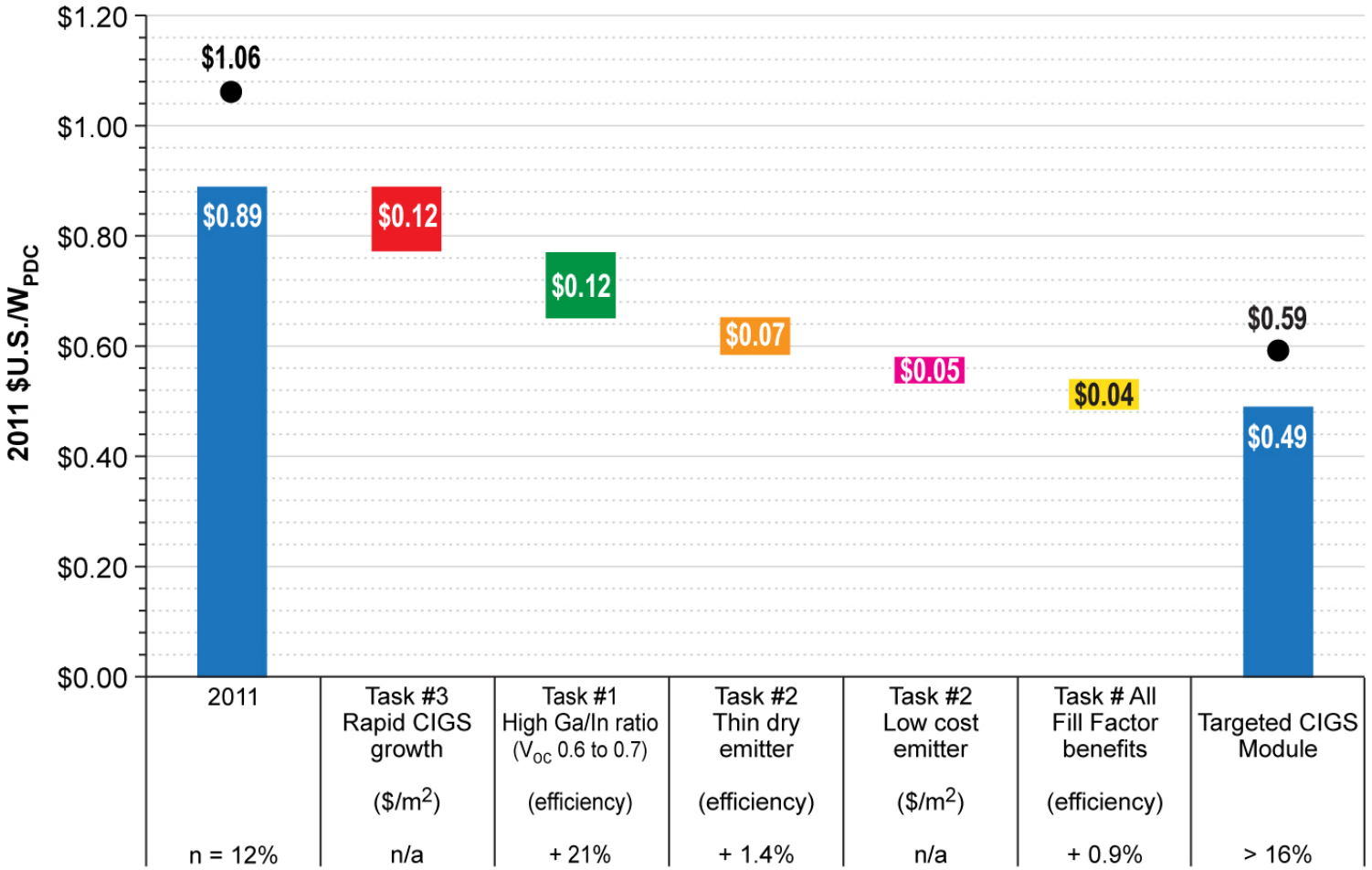
Coevaporated CIGS (on glass): Road Map



- Assumes (2011) In and Ga prices (historic highs)

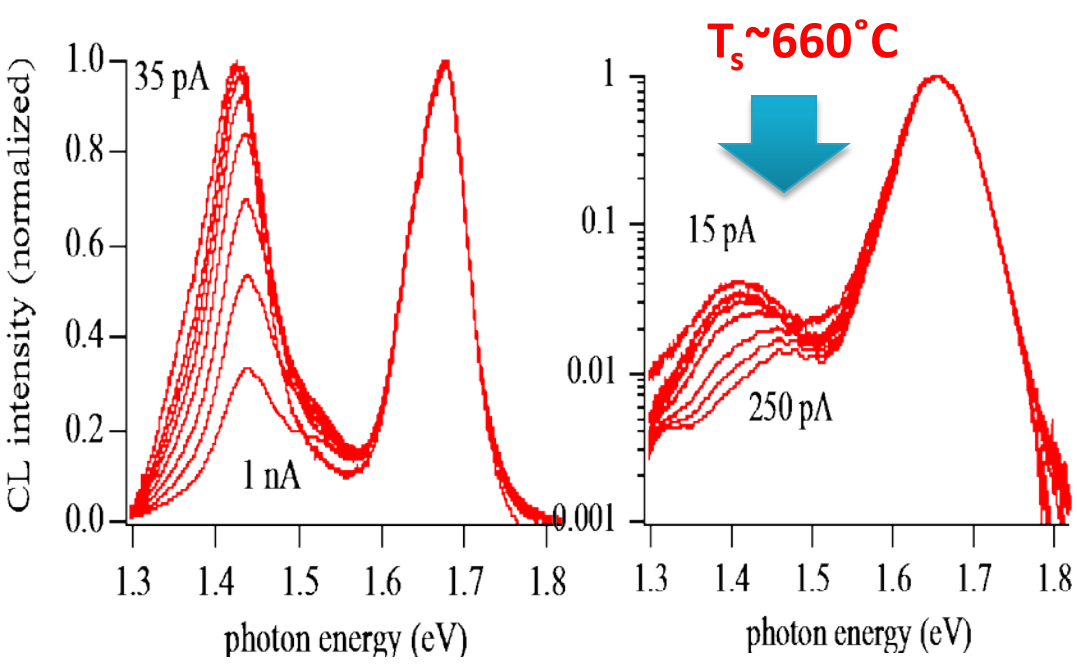
CIGS Solar PV Module Manufacturing Cost/Price

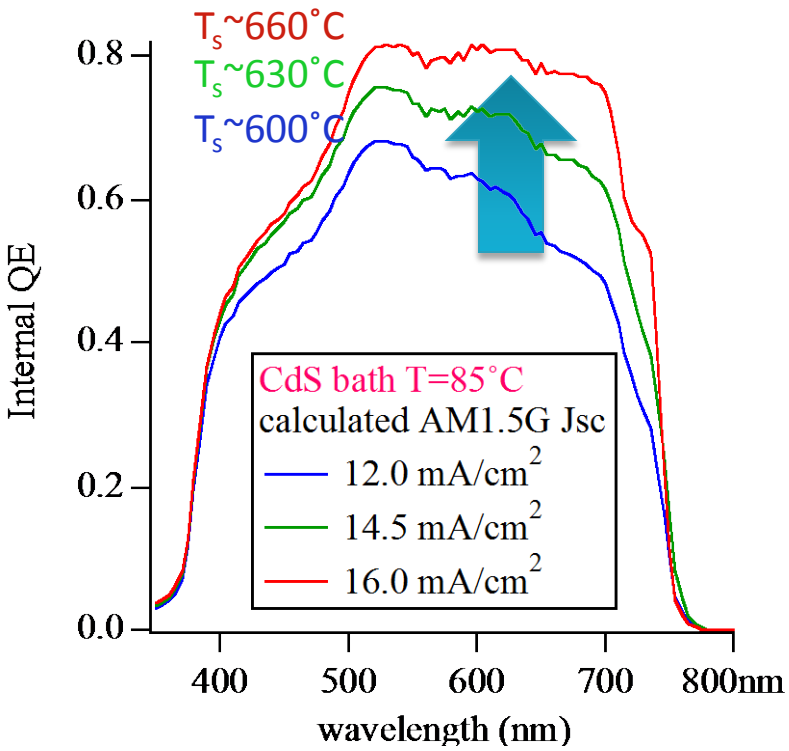
Coevaporation, U.S. production location (price: 15% gross margin)



Source: Goodrich, A; Woodhouse, M; Noufi, R. "CIGS Road Map", NREL Technical Report (in preparation), 2011

Technical Approach/past experience lessons





- Deep level DAP => 0.220 eV < $E_A + E_D$ < 0.280 eV
- Emission decreases with increased Ts

- Improved band-edge SR with increased T_s
- Effect of T_s on SR ΔJ_{sc} ~4 mA/cm^2

***Key finding**: higher (than std) processing temperatures lead to a reduction of recombination centers located deep within the gap of CGS*

OPTIMIZATION OF $CuGaSe_2$ FOR WIDE-BANDGAP SOLAR CELLS, Miguel A. Contreras, M. Romero, and D. Young
Proceedings of the 3rd World Conference in Photovoltaic Energy Conversion, Osaka, Japan 2003,