Innovative Device Structures and New Materials for Scaling Nano-CMOS Logic Transistors to the Limit

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Intel Fellow and Director,

Transistor Technology and Integration,

Intel Corporation

Key Messages

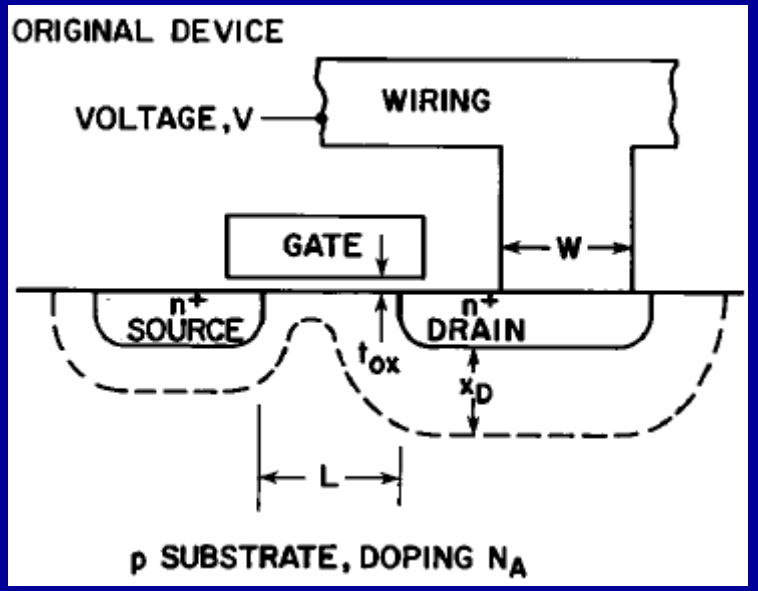
- End of traditional dimensional scaling era
- New and rapid innovations in transistor structure and materials are now key to sustaining Moore's Law: **Uniaxial strained silicon and HiK + Metal Gate**
- **Power Limited Era:** New Transistor Architectures are needed to meet the performance improvements while keeping within power budget
- **Nanoscale Design Rule Regime:** Dimensional scaling does not mean better transistor performance.
- This is the most exciting time to be doing transistor research and development

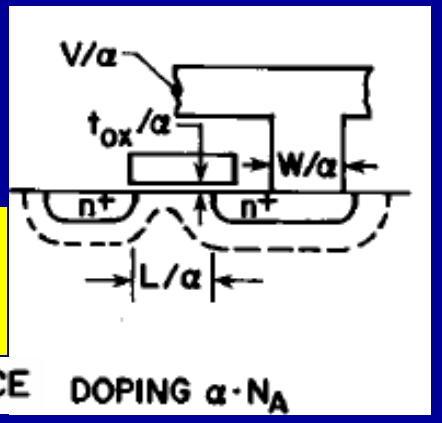
Outline

- **End of Traditional Scaling Era**
  - Traditional scaling limiters and implications
- **Intel's Response**
  - Uniaxial Strain (90nm and 65nm Nodes)
  - HiK + Metal Gate + Strain (45nm Node)
- **Challenges and Solutions Beyond 45nm Node**
  - **Uniaxial Strain:** Ultimate limit of silicon mobility enhancement
  - **Power Limitation:** Implications on future transistor structures
  - **Parasitics Dominated Era:** How to address increasing negative impact of parasitics?
  - **New Channel Materials:** III-V QW FET's at Vcc~0.5-0.7V Key requirements for implementing III-V channels into mainstream?

Geometric Dimensional Scaling Era

- **Gate Oxide Thickness Scaling**
  - Key enabler for Lgate scaling
- **Junction Scaling**
  - Another enabler for Lgate scaling
  - Improved abruptness (R_{EXT} reduction)
- **Vcc Scaling**
  - Reduce X_{DEP} (improve SCE)
  - However, did not follow const E field



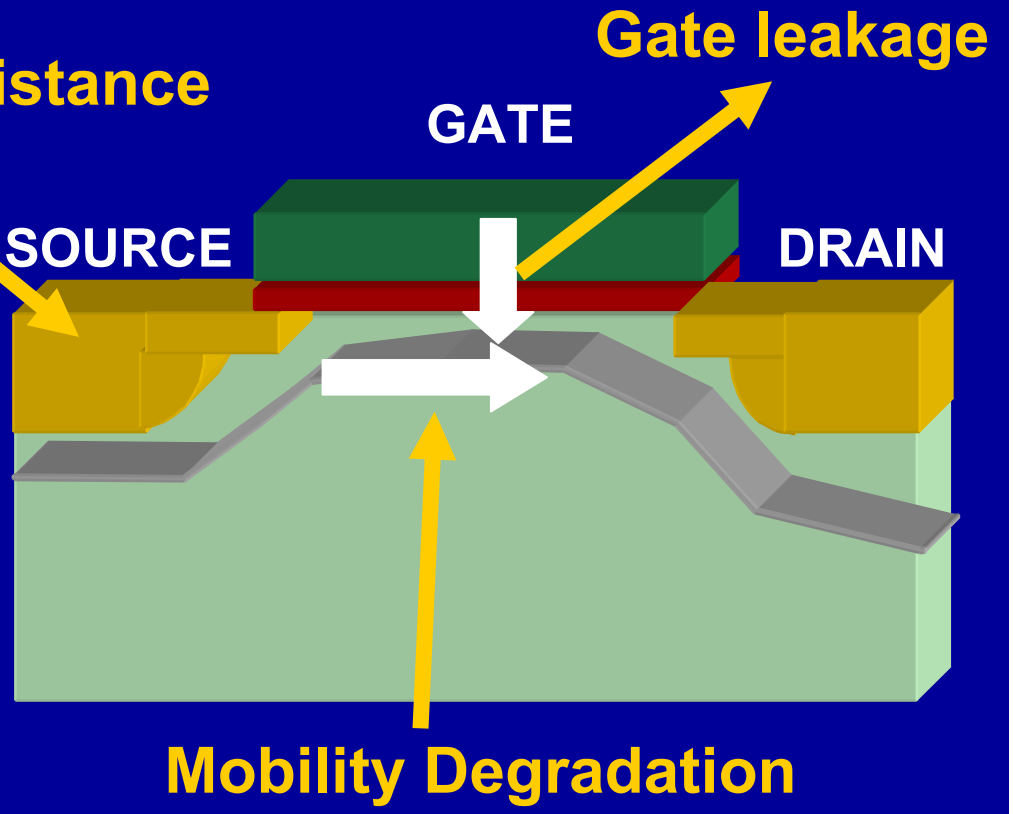


R. Dennard et.al.
IEEE JSSC, 1974

1990's: Golden Era of Scaling
Dramatic Vcc, Tox & Lg scaling. Increasing Idsat

Top Traditional Scaling Limiters

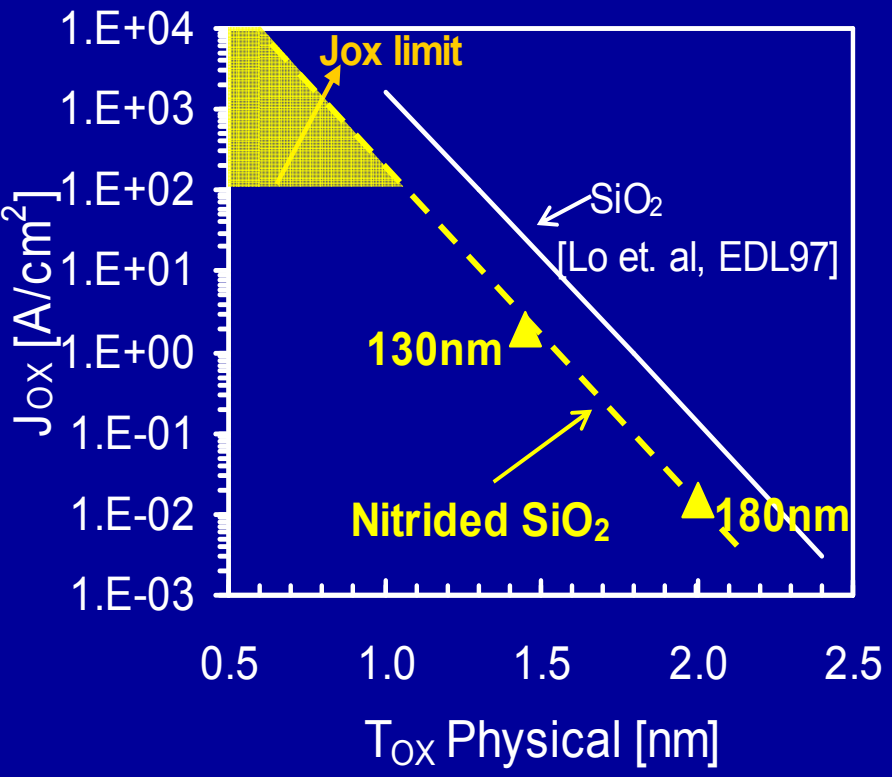
- Gate Leakage
- Mobility Degradation
- Parasitic Resistance

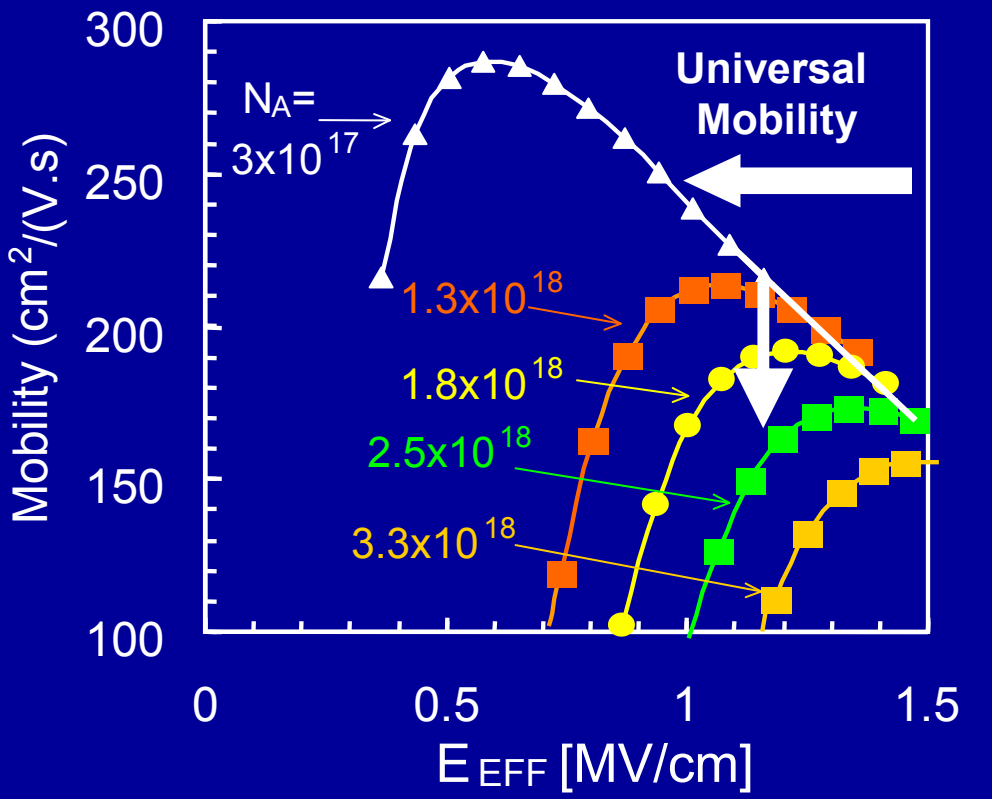


Top Scaling Challenges faced by Intel's 90nm CMOS Research Team in 2000

SiO_2 Scaling and Mobility Reduction Trend

T. Ghani et. al. VLSI Symp. 2000





Gate Oxide Leakage: Direct tunneling limited.

Running out of Atoms

Significant mobility reduction due to channel ionized impurity scattering

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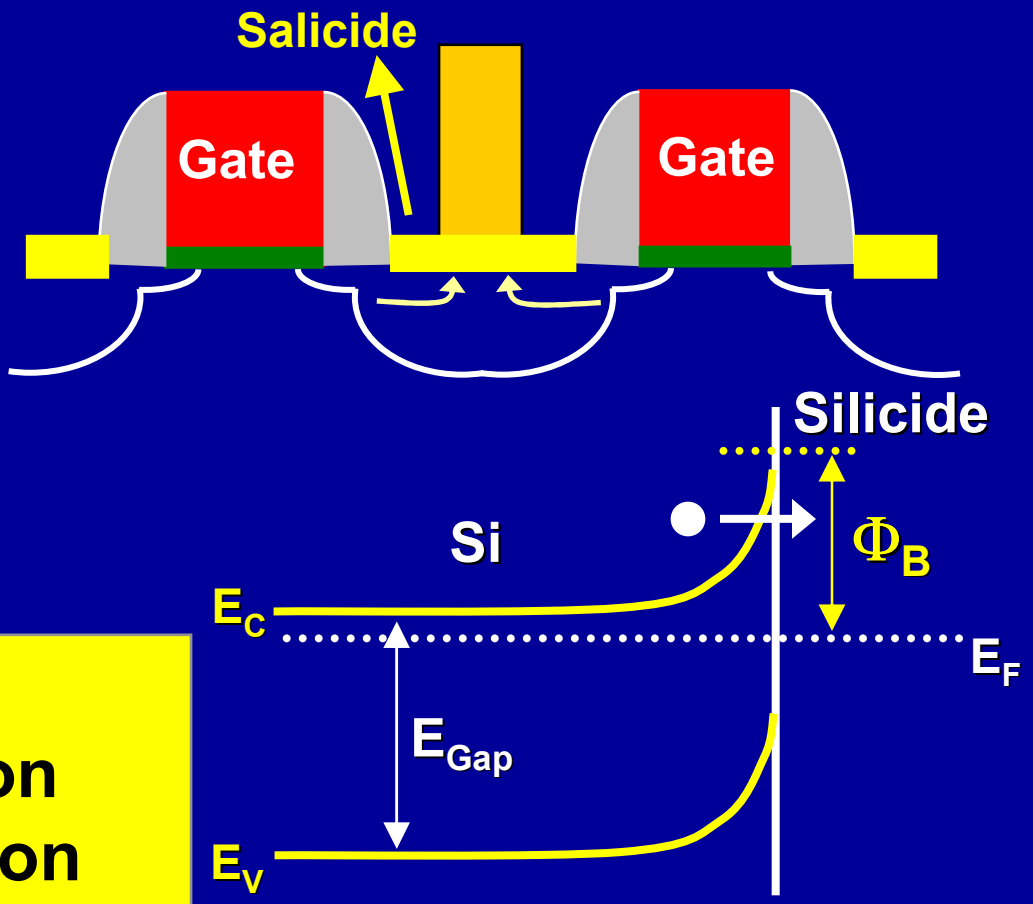
Parasitic Resistance Impact

- Salicide interface resistance becoming a significant component of R_{EXT} due to salicide area scaling
- S/D doping close to solid solubility in Si (N_{surf})



Solutions:

- **Barrier height reduction**
- **Higher dopant activation** (Exceeding solid solubility ☹)

$$\rho_c \propto \exp\left(\frac{4\pi\Phi_B}{qh}\sqrt{\frac{m^*\varepsilon}{N_{surf}}}\right)$$

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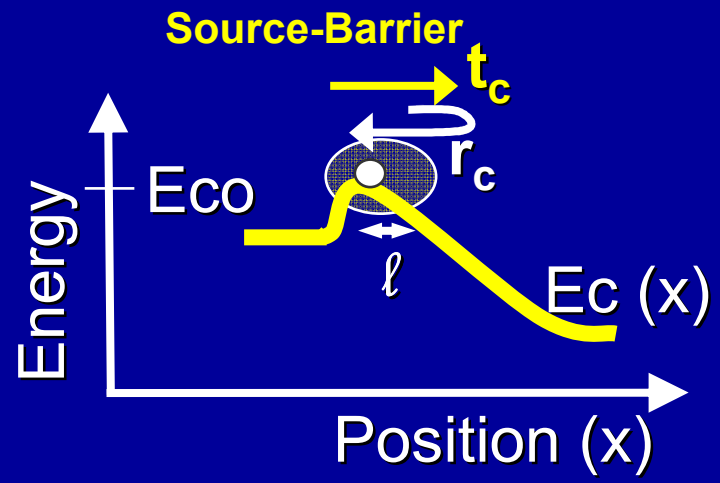
  - **Power Limitation:** Implications on future transistor structures
  - **Parasitics Dominated Era:** How to address increasing negative impact of parasitics?
  - **New Channel Materials:** III-V QW channels at Vcc~0.5-0.7V

Innovations Introduced by Intel to Overcome Traditional Scaling Barriers

- Uniaxial process induced strain innovations for dramatic mobility enhancement starting at 90nm CMOS node
  - **Epitaxial SiGe S/D**
  - **SiN Capping Layers**
- HiK gate insulator being introduced at 45nm CMOS node to replace SiO_2 to help address gate leakage
- Metal Gate being introduced at 45nm CMOS node to replace poly-silicon gate to enable Tox(e) scaling

Why is Low Field Mobility Important for Nanoscale Transistors?

M. Lundstrom et. al., EDL 1997



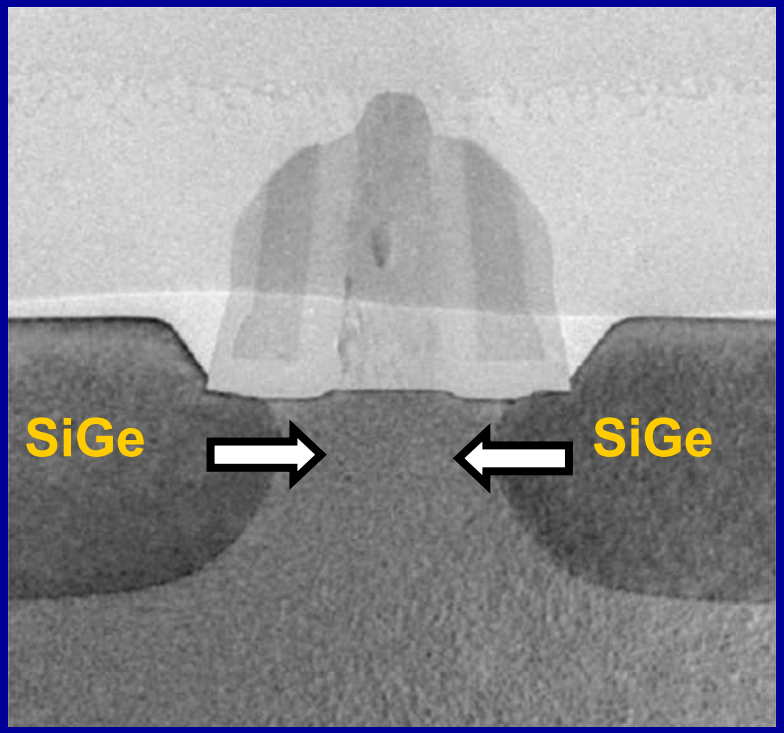
$$I_{DSAT} = W\left[C_G\left(V_{GS} - V_T\right)\right]\upsilon_S(0)$$

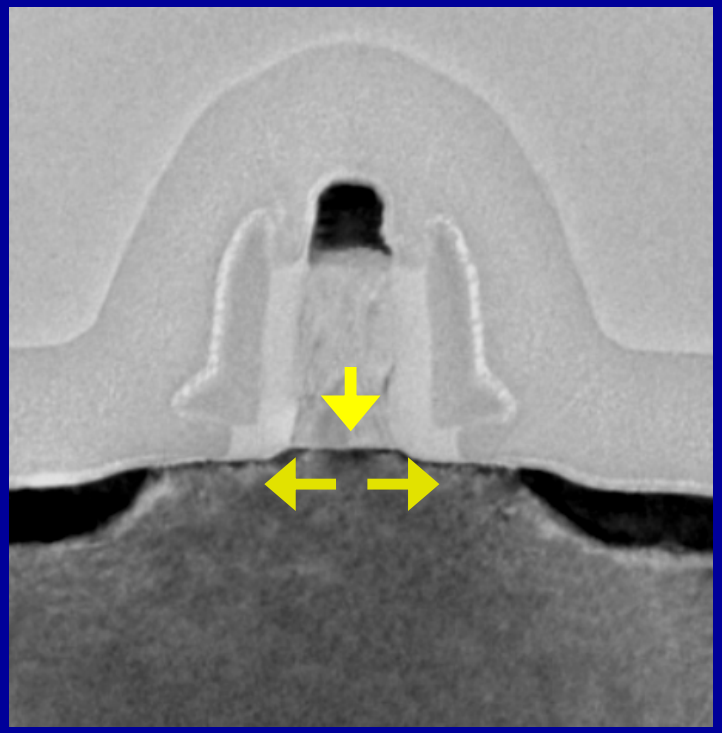
$$\frac{1}{\upsilon_S(0)} = \frac{1}{\upsilon_{inj}} + \frac{1}{\mu_{eff}E(0^+)}$$

- Conventional theory assumes infinite supply of carriers at the source
- $\upsilon_s(0)$ and I_{DSAT} limited by lower of the two velocity term ➔ Ultimately limited by thermal injection from source to channel (ballistic)
- Best devices in production today are ~ 60% ballistic
  ➔ Equal contributions by ballistic and mobility terms
- **Low field mobility important to nano-MOS transport**

Uniaxial Strain Silicon Transistors
Intel: IEDM 2003

PMOS T. Ghani et. al. IEDM, 2003 **NMOS**



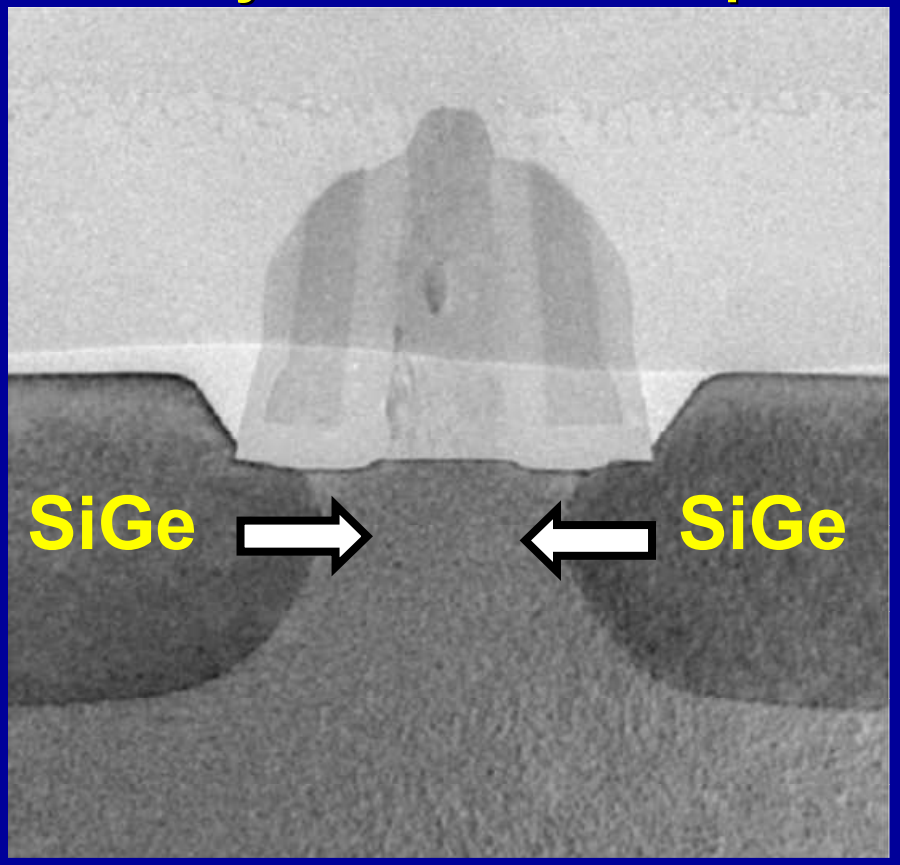


These transistor structures introduced first at Intel's 90nm CMOS node. These structures have now become industry standard for strain implementation

PMOS Strain Implementation

- SiGe epitaxial S/D
  Formed by Si recess etch and selective Strained SiGe epi growth
- Strained SiGe induces large lateral compression in channel
  - ➔ Valence bands warpage and LH-HH splitting
  - ➔ Dramatic mobility gain
- SiGe S/D also improves parasitic resistance by reducing salicide interface resistance

Uniaxially Strained SiGe Epi S/D



Lateral compression in channel

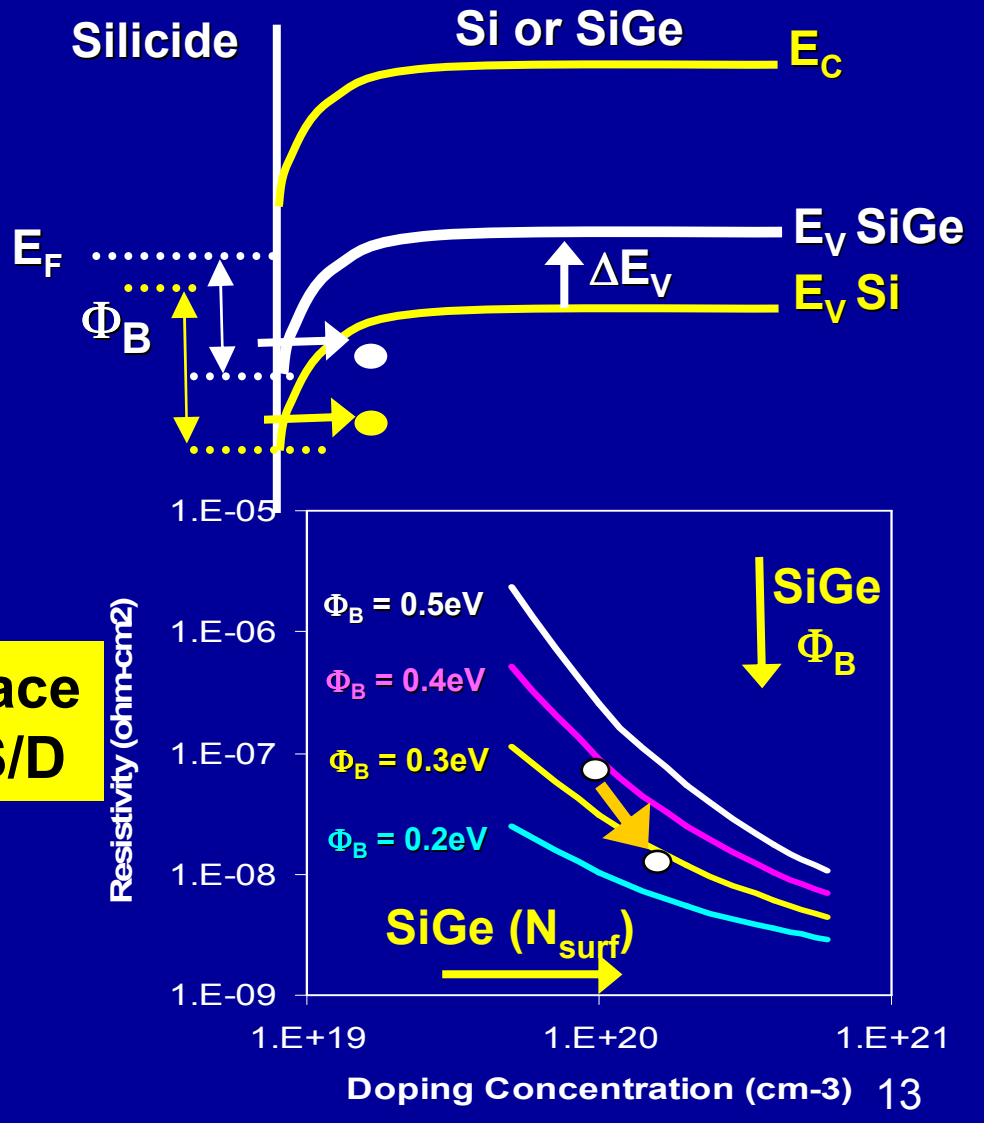
T. Ghani et. al. IEDM, 2003

Strained SiGe S/D Reduces Salicide Interface Resistance

- Strained SiGe has smaller Eg
  ➔ Smaller hole barrier height at silicide interface
- Exponential reduction of interface resistance on Φ_B
- Higher boron activation in SiGe relative to Si (↑N_{surf})

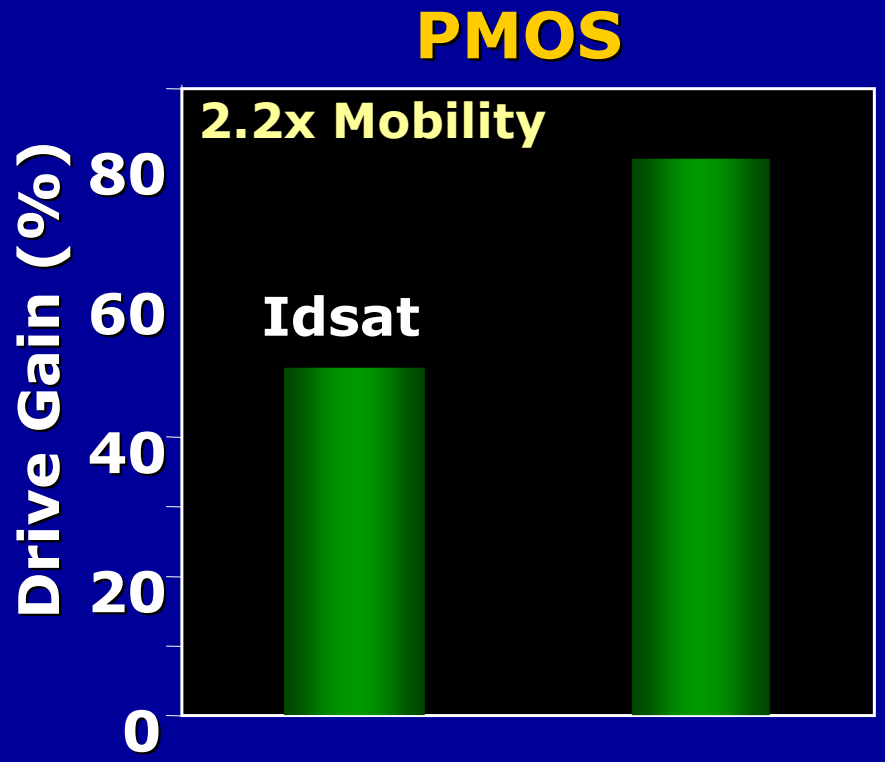
Dramatic reduction in sal interface resistance with strained SiGe S/D

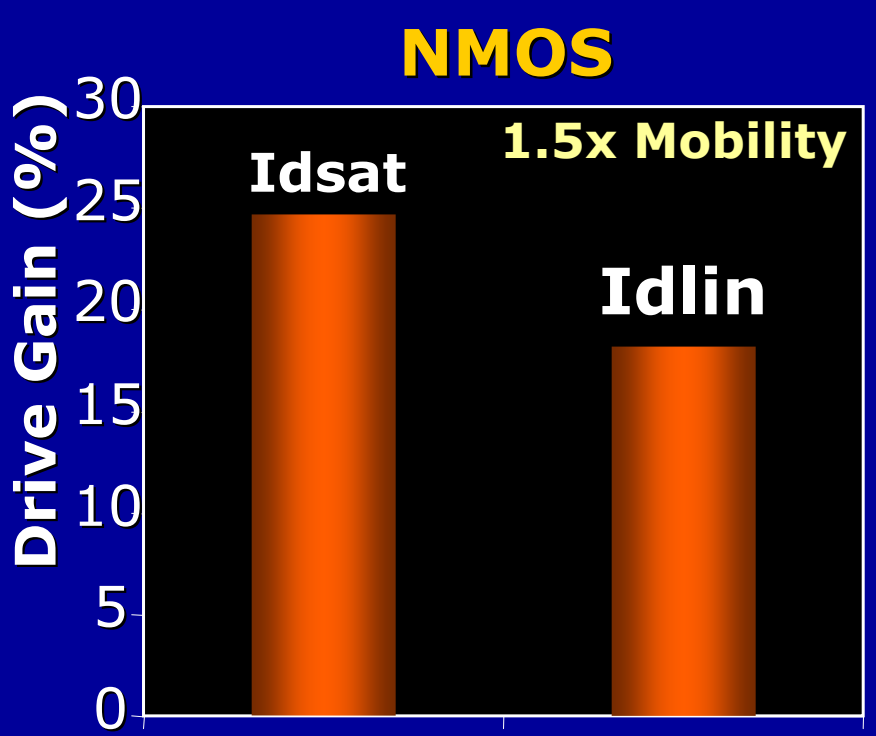
$$\rho_c \propto \exp\left(\frac{4\pi\Phi_B}{qh}\sqrt{\frac{m^*\varepsilon}{N_{surf}}}\right)$$



Uniaxial Strain Performance Gain (Intel) 65nm CMOS Node

Ref: Unstrained Silicon





Uniaxial strain has demonstrated dramatic PMOS and NMOS performance improvement on 90nm & 65nm CMOS nodes

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Innovations Introduced by Intel to Overcome Traditional Scaling Barriers

- Uniaxial process induced strain innovations for dramatic mobility enhancement starting at 90nm CMOS node
  - Epitaxial SiGe S/D
  - SiN Capping Layers
- **HiK gate insulator being introduced at 45nm CMOS node to reduce gate leakage**
- **Metal Gate being introduced at 45nm CMOS node to replace poly-silicon gate to eliminate poly depletion: Scale Tox(e)**

Thermal Oxidation and Poly Silicon Gate: KEY TO MICROELECTRONIC REVOLUTION

JOURNAL OF APPLIED PHYSICS VOLUME 36, NUMBER 12 DECEMBER 1965

General Relationship for the Thermal Oxidation of Silicon

B. E. Deal and A. S. Grove
Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation, Palo Alto, California

(Received 10 May 1965; in final form 9 September 1965)

IEEE Spectrum October, 1969

Silicon-gate technology

Low-cost, large-scale integrated electronics based on metal-oxide-semiconductor design benefits from the application of silicon-gate technology

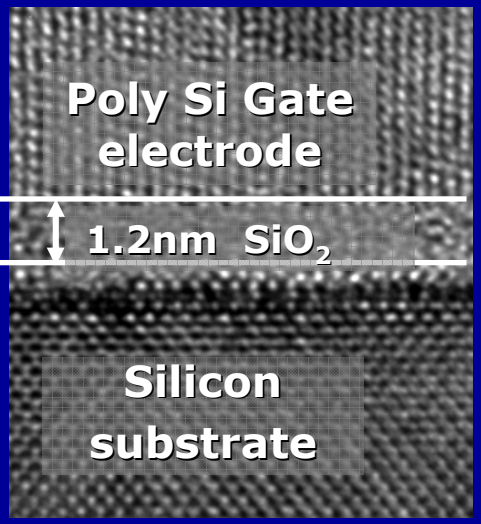
L. L. Vadasz, A. S. Grove, T. A. Rowe, G. E. Moore Intel Corporation

SiO_2 Growth Technology: Enabled MOS transistor to become a reality
Poly Silicon Gate: Key to Self Alignment ➔ Device Scaling

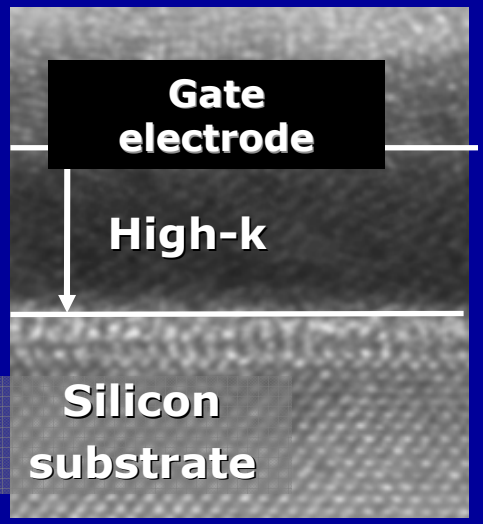
Poly /SiO_2 gate stack was the foundation on which IT revolution has been built. Served well for 40y BUT…

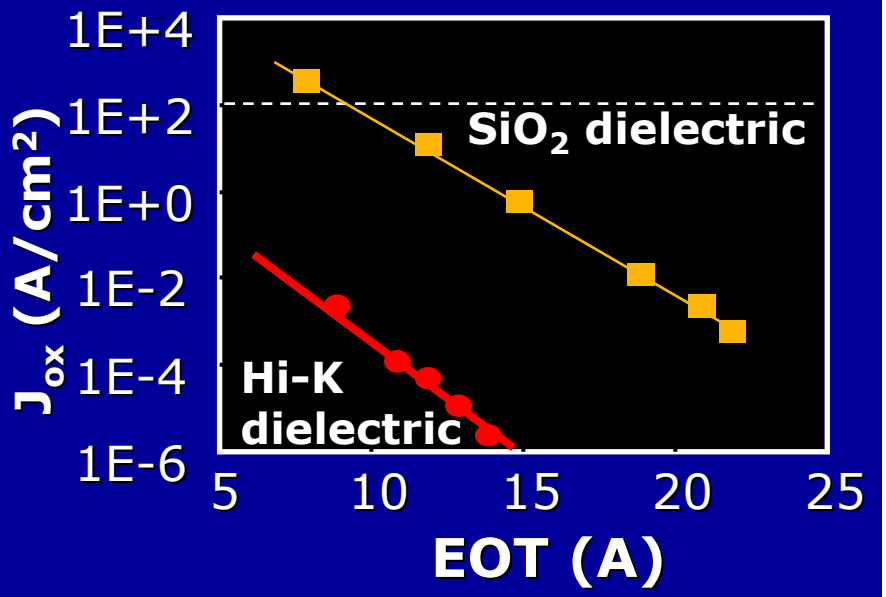
Gate Leakage Reduction with HiK

Intel 65nm Node



HiK Gate Dielectric

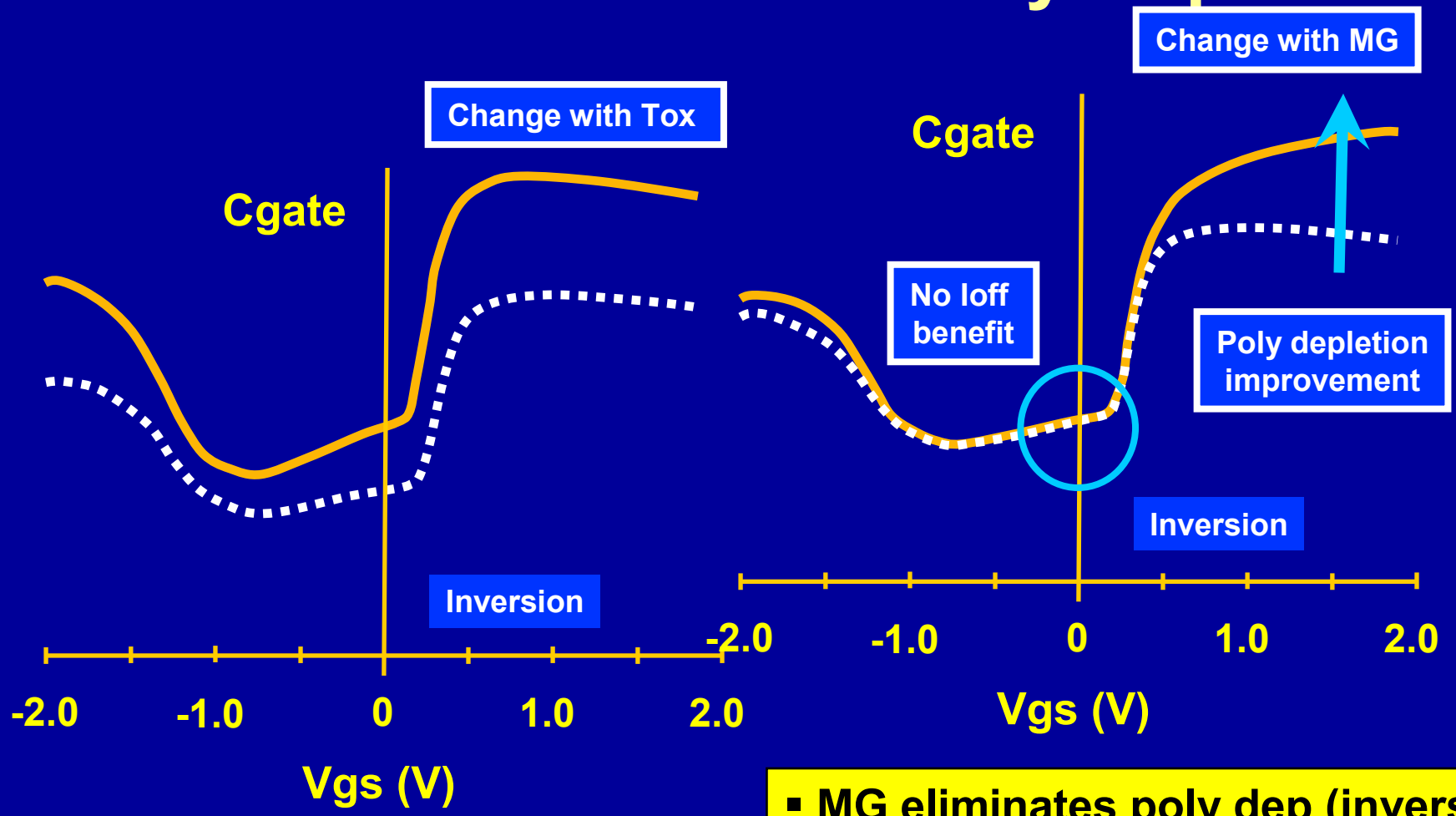




	SiO2	High-k
Capacitance:	1.0x	1.6x
Leakage:	1.0x	< 0.01x

BENEFIT:
Significant gate leakage reduction at a given EOT

Metal Gate Eliminates Poly Depletion

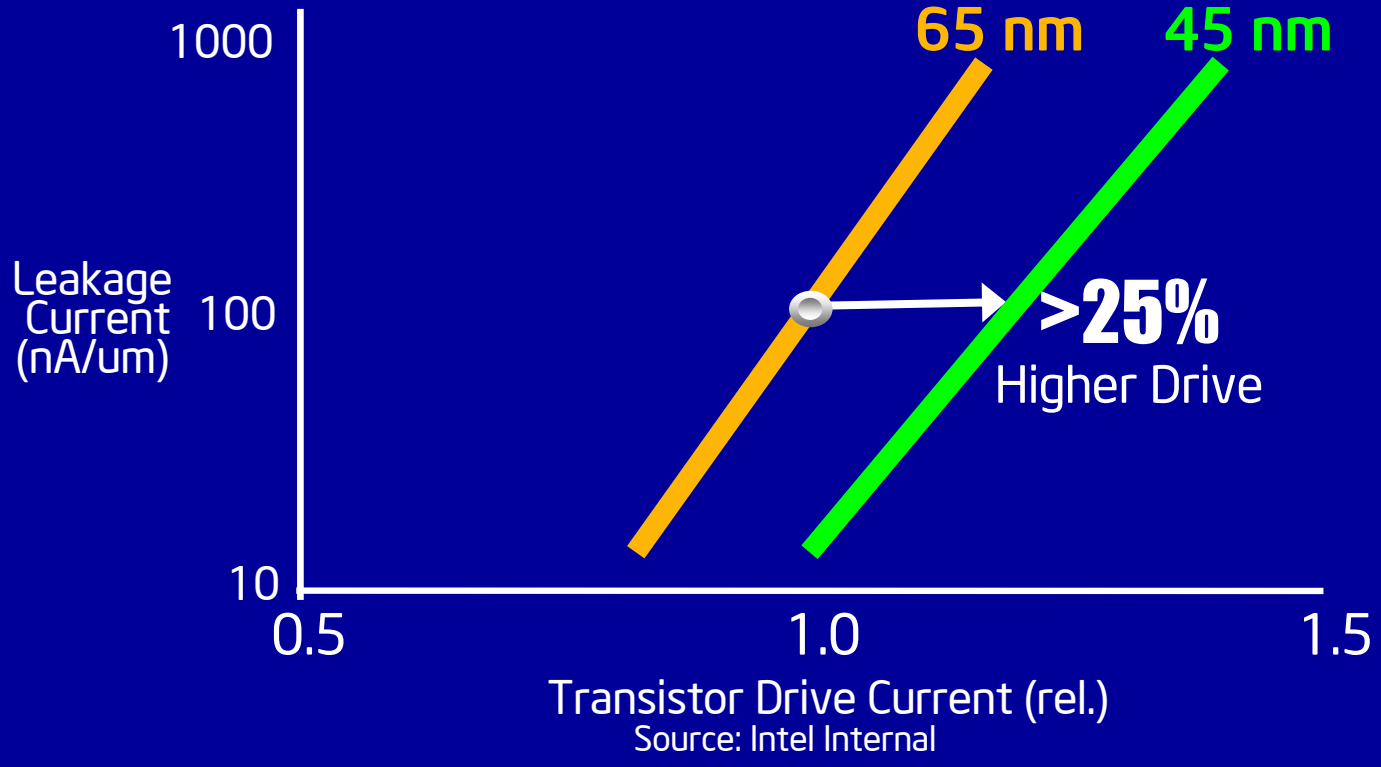


True "Tox" change
Capacitance benefit everywhere
Both Idsat and SCE improve

- **MG eliminates poly dep (inversion)**
  - ➔ ***Increases gate E-field***
  - ➔ ***Larger Qinv ➔ High Idsat***
- **Tox (inv) scales significantly**
- **BUT! Tox(e) does not impact SCE**

High-k+Metal Gate Performance / Power Benefits

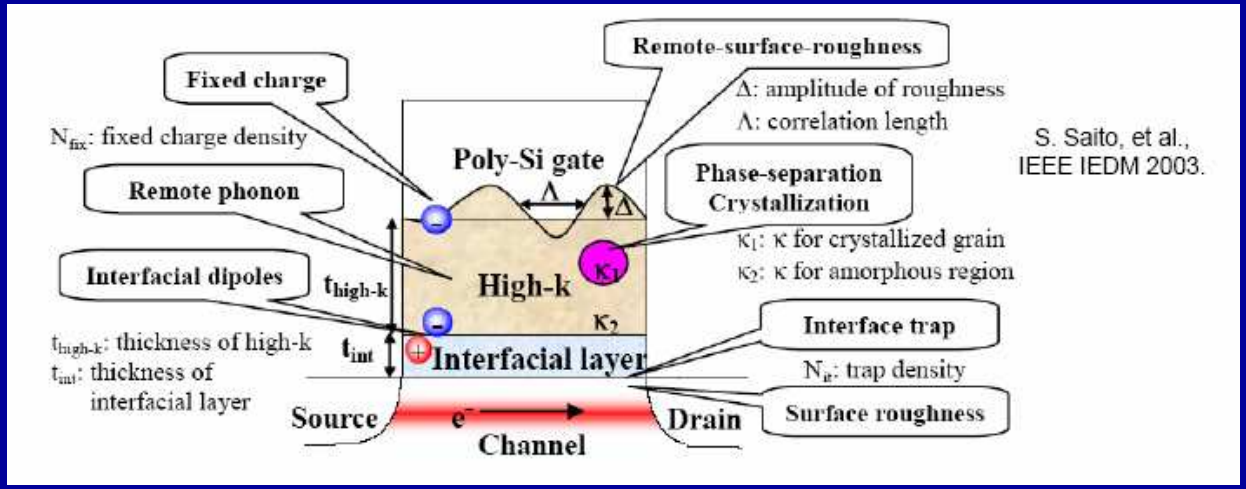
Transistor Performance vs. S/D Leakage



Source: Intel Internal

>25% Idsat gain demonstrated for 45nm CMOS vs. 65nm CMOS at fixed Ioff

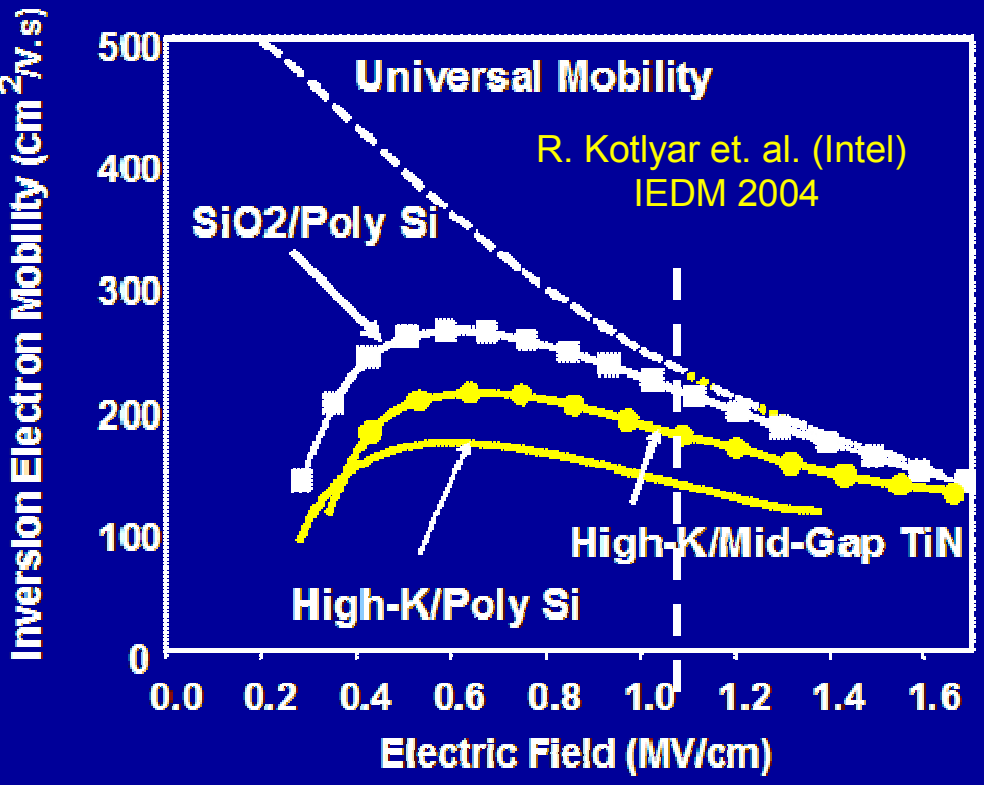
Top Issues with Hi-k + Metal Gate CMOS Technology



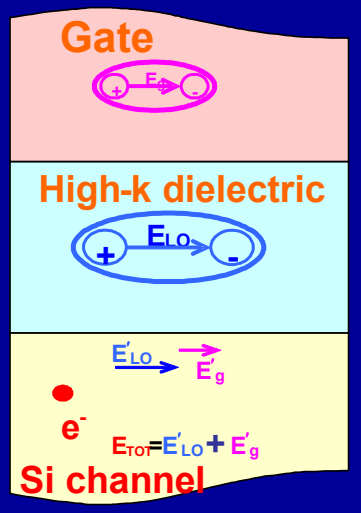
- Right Metal Gate ϕ_{MS} electrodes which are HiK compatible
- Bulk & interface traps:
  Poor reliability (Need better than SiO2 reliabilty due to higher E)
- New scattering modes:
  Poor mobility
- Technology Integration
- Yield / Manufacturability

Extensive R&D done at Intel to successfully address the significant Material, Integration and Manufacturing challenges in implementing HiK + Metal Gate CMOS Technology.

HiK Mobility Challenge



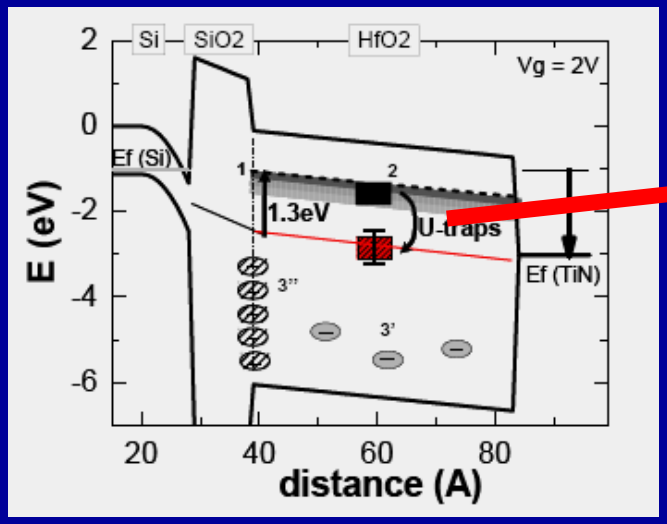
- NMOS mobility with high-k degrades ~ 40% from SiO_2 / poly stack
- Model: High-k dipoles vibrate !! Mobility degradation due to to scattering with soft optical vibrational modes of dielectric
- Very high charge density of MG screens dipole vibrations.



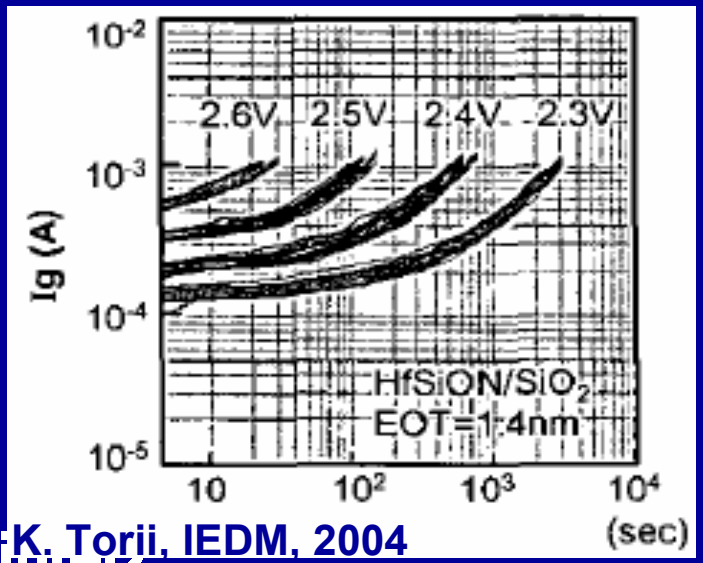
Metal Gate recovers ~50% of the degradation. Further stack optimization is required for mobility improvement

M. Fischetti et. al. J App Phys, 2001

High-K Reliability Challenge



J. Mitard, IRPS, 2006



K. Torii, IEDM, 2004

- Metal-Hf based Oxide system susceptible to oxygen vacancy sites → Efficient electron traps located in upper half of HfO_2 bandgap: Well documented in literature
- These traps are responsible for NMOS hysteresis, BT and TDDB
- Key to reliability is passivating Vo sites
- HiK/Metal Gate intrinsic reliability requirement more stringent than best SiO2 because they need to withstand higher E-Field

Effective Solutions to Bias-Temp and TDDB are Key to "HiK + Metal Gate" Implementation

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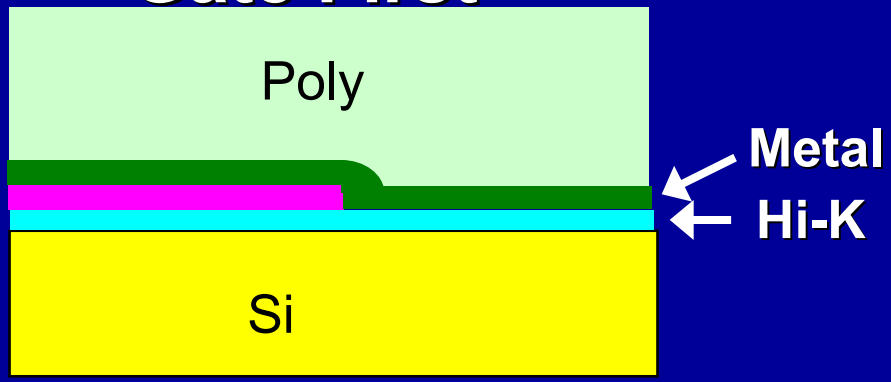
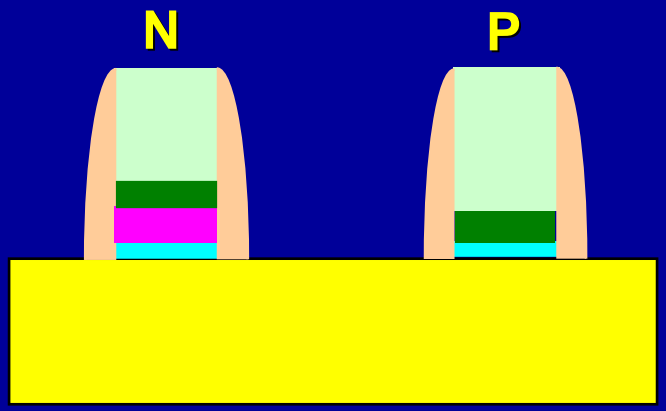
HiK - Dual Metal Gate Integration

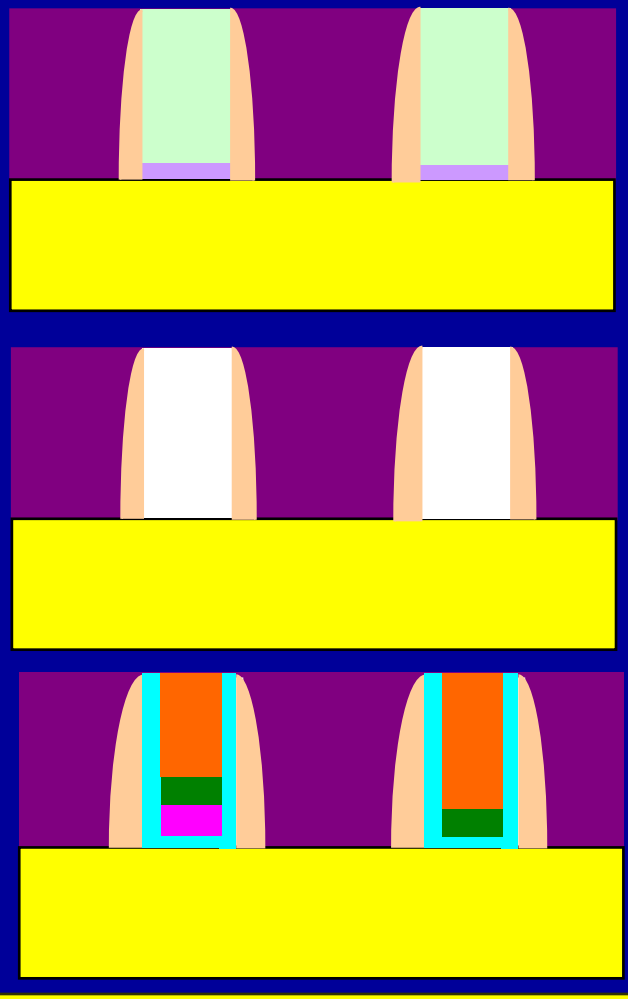
Gate First





- Stability → Right Φ_{MS} N & P metals which survive high thermal anneal
- Dual metal gate stack patterning
+ Standard process flow

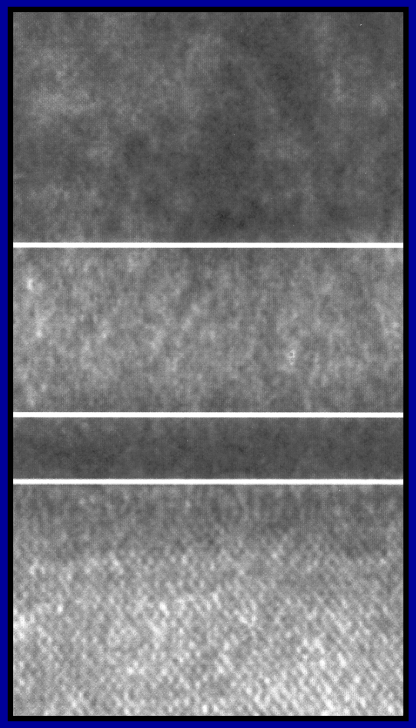
Gate Last



+ Metals deposited after high Dt → More MG options
- Non-std process flow

Intel's 45nm Node HiK/MG Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

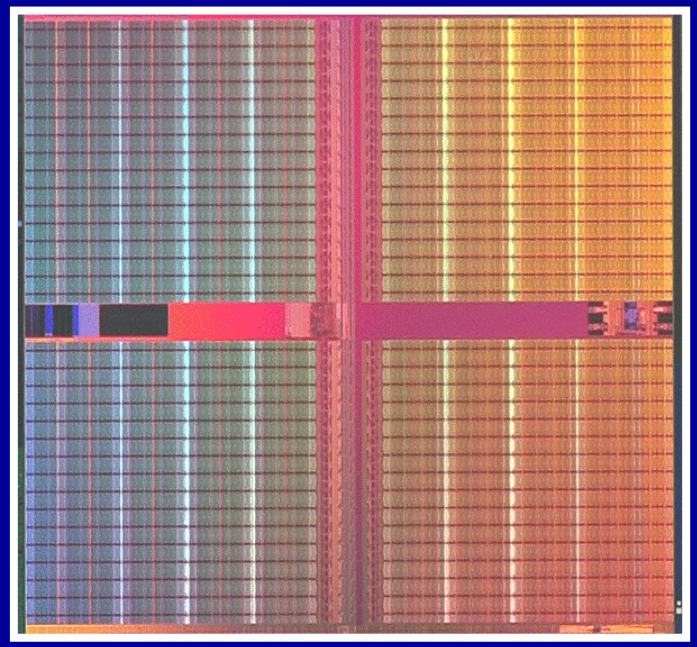
Silicon Substrate

45nm "HiK + Metal Gate" CMOS technology meets meets performance, yield and reliability goals

"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s." — Gordon Moore

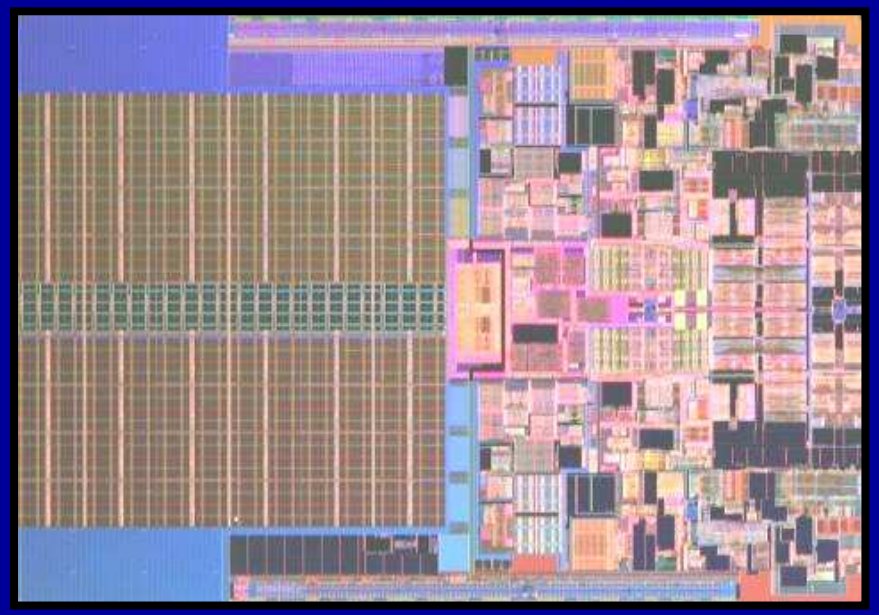
World's First Working 45 nm CPU with HiK + Metal Gate

45nm SRAM Test Vehicle
Jan' 2006



> 1 Billion Transistors

Intel® Penryn: 45nm CPU
Jan' 2007



World's first working 45 nm CPU

- **45nm SRAM Test Vehicle has >1B transistors**
- **On track to ship 45nm CPU's in 2007**

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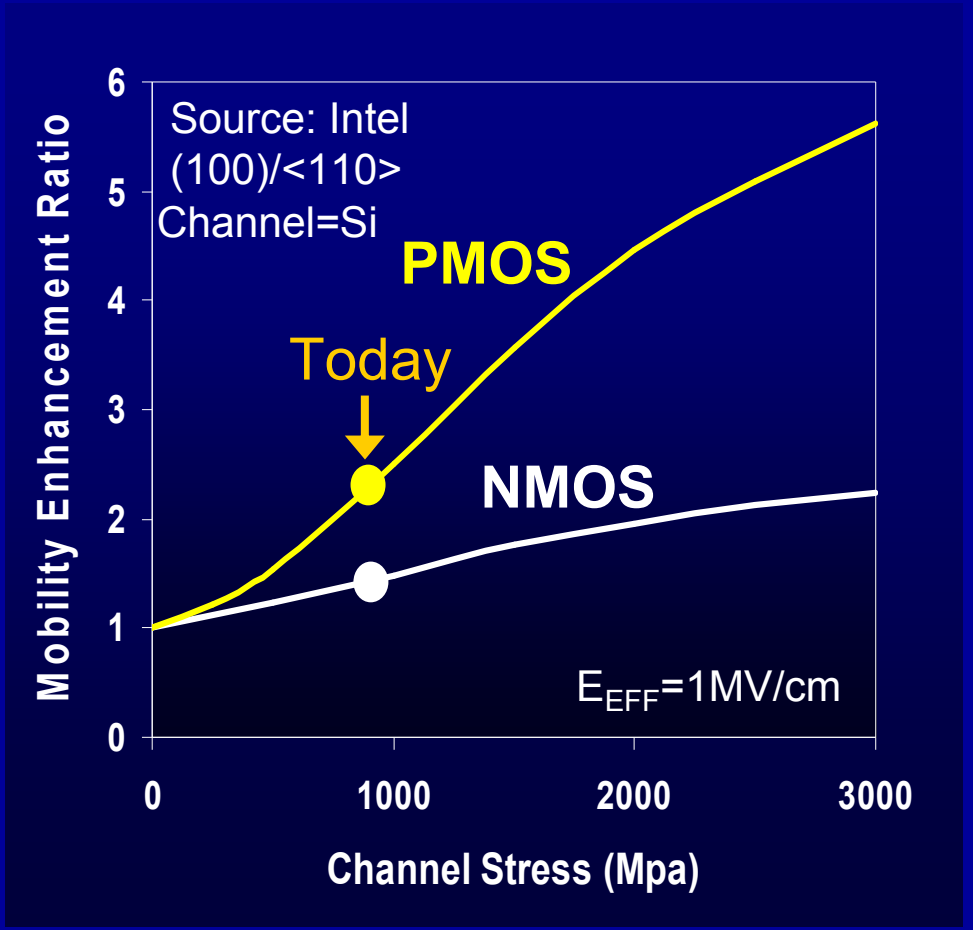
How Far Can Uniaxial Strain Extend Si Performance Gains?

- **Significant headroom left to increase PMOS mobility in future (> 5x)**

  Mobility gain driven by hole m_{eff} reduction due to band warpage !

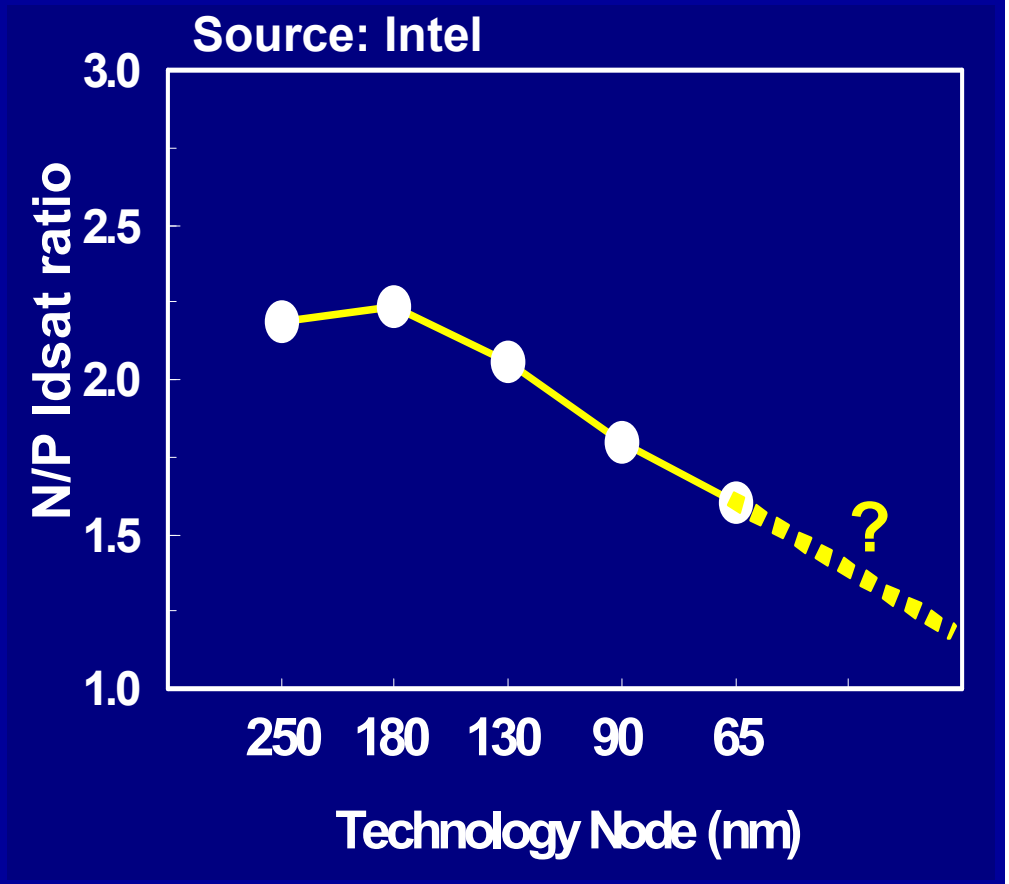
- **Limited Max Mobility Gain for NMOS (~ 2x).**

  Maximum gain limited by fundamental physics



Implications of Significantly Higher PMOS Mobility Enhancement

- Expect NMOS and PMOS mobility values to approach each other
- PMOS device drive strength to approach NMOS in future
- N/P ~ 1 ➔ N/P Symmetry
  - *Device sizing in circuits*
  - *Device usage model*



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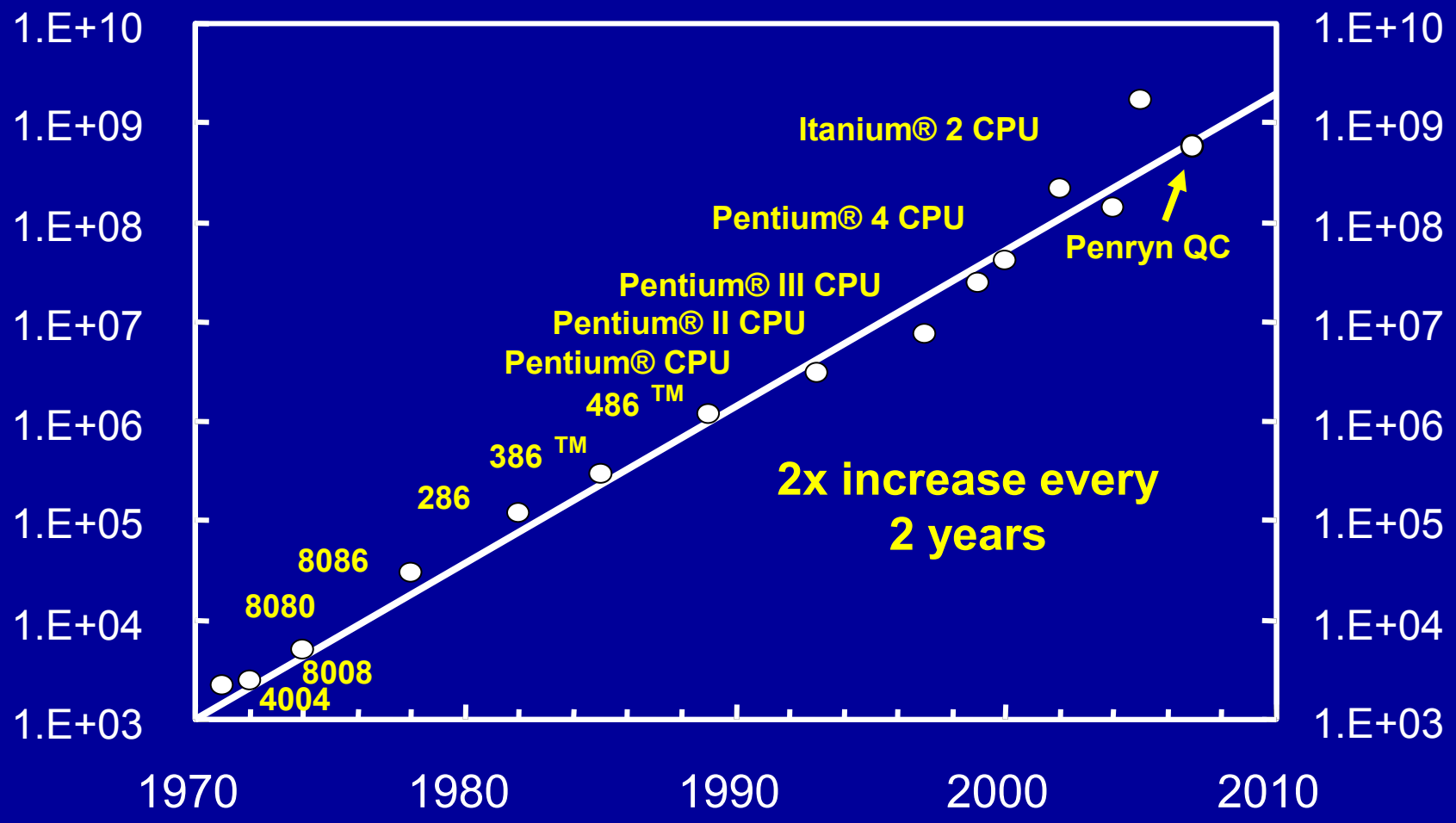
CPU Transistor Count Trend



2x Transistors Every 2 Years
➔ In Line with Moore's Law

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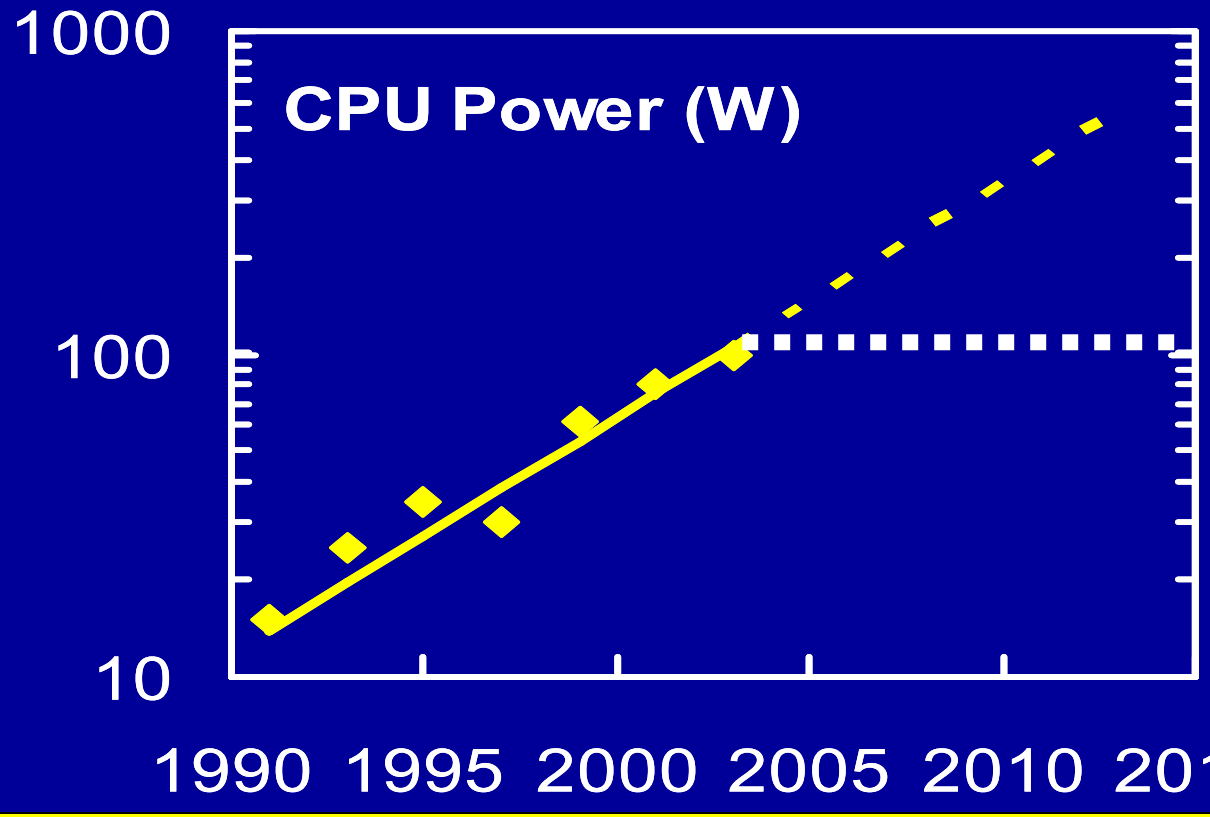
Negative Consequence of CPU Transistor Count Trend



Right Hand Turn: Power Dissipation Limited to ~100W

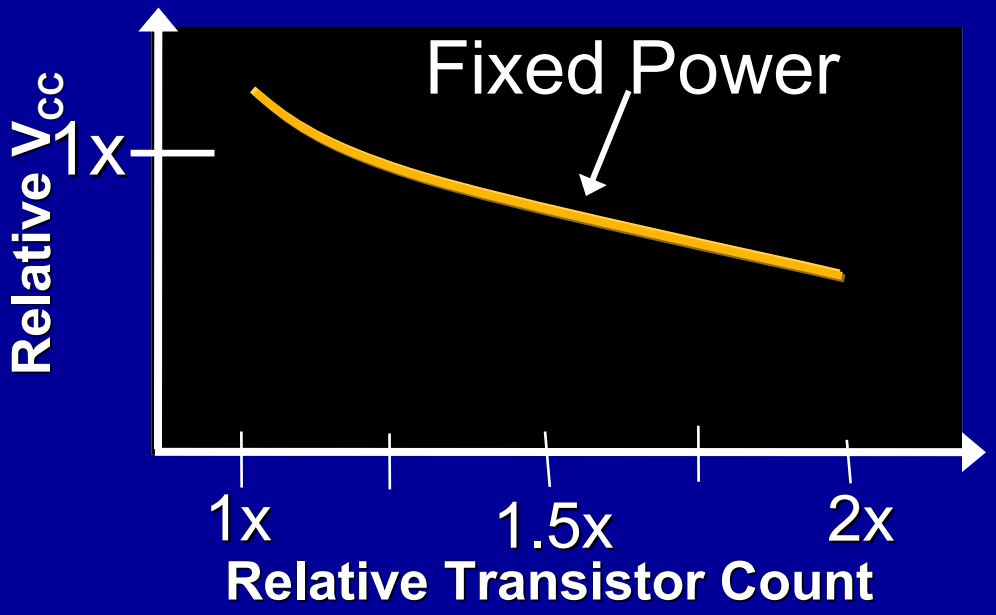
BUT increased transistor count needed in Multi-Core CPU Era !!!

Multi-Core CPU Power Limited Era

P = Switching Power + Leakage Power + ..

$$\sim (fC_{gate}V_{CC}^{2}\alpha) * N$$

Constant

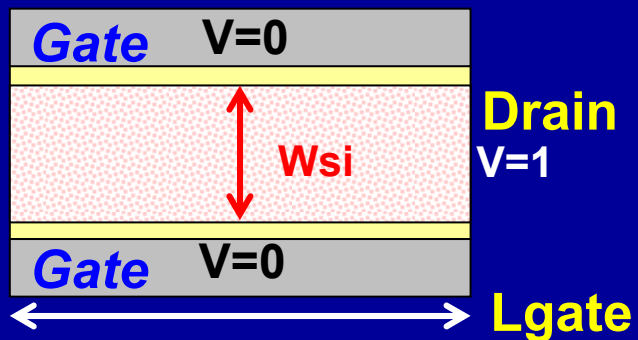


- **V_{CC} scaling required for continued increase in transistor count in power limited world**
- **Key Issue with Vcc Scaling: Performance loss !!!**

How to maintain high performance at scaled V_{CC}?

Multi-Gate Transistor Architecture

$$\frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}}$$

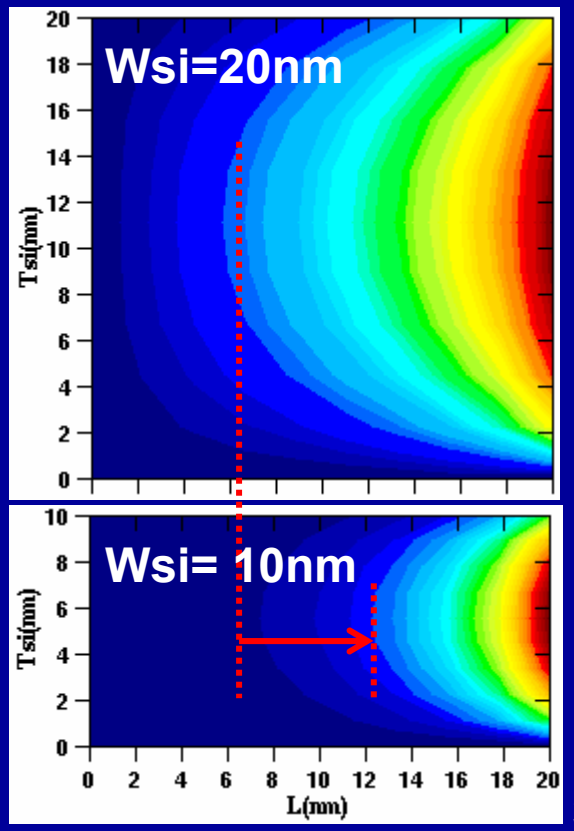


Multi-Gate Transistors have better SCE:

- + Gates in close proximity reduce spread of V_{drain}
- + Small W_{Si} desired to minimize SCE
- + At very thin W_{Si}, channel potential impervious to dopants

Mutigate transistors have higher mobility due to:

- + Lower channel doping
- + Lower E_{eff} in channel



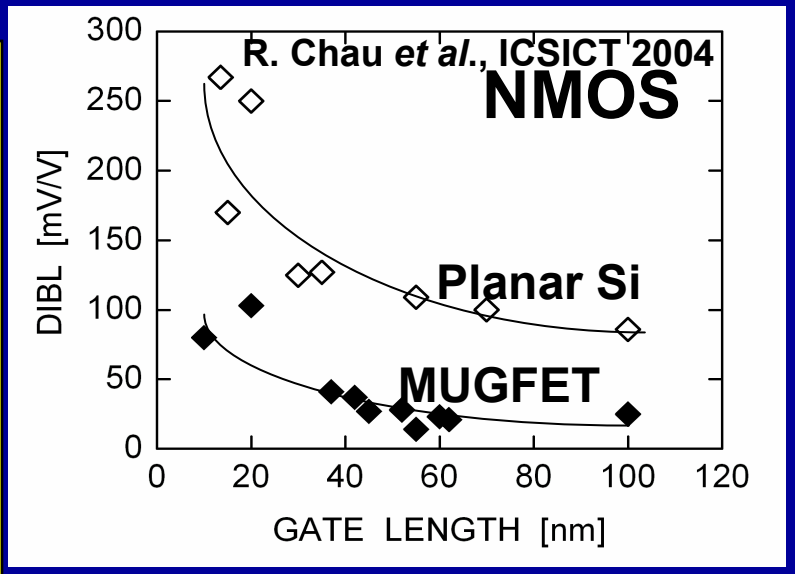
Multi-Gate Transistors Enable Vcc Reduction

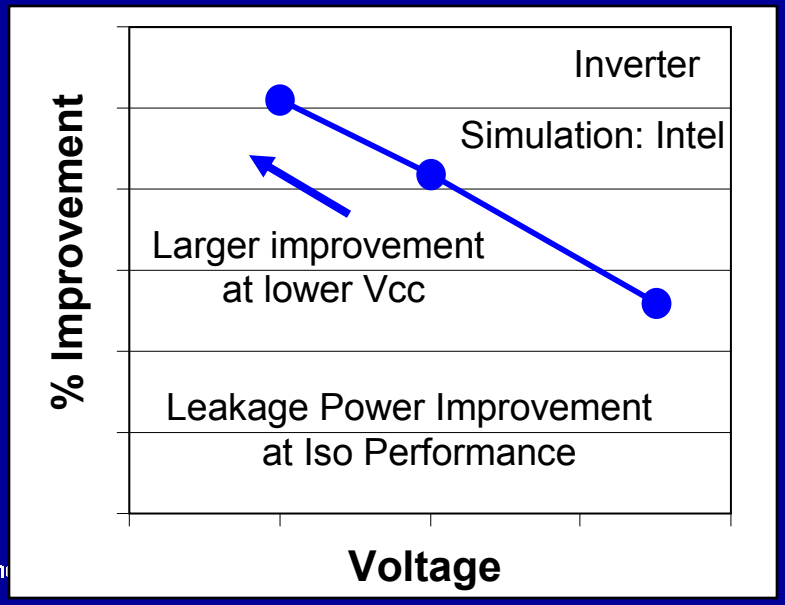
Multi-Gate Transistors show superior DIBL & Mobility:

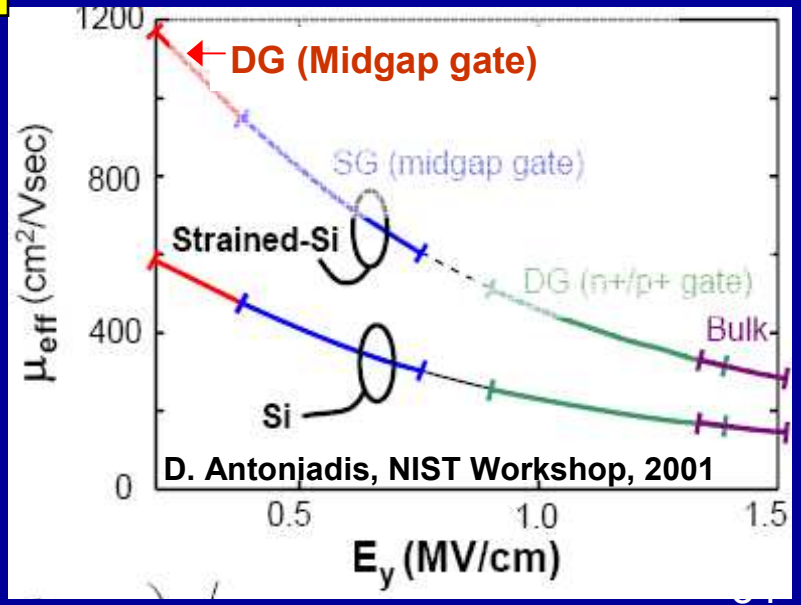
➔ Lower Vt at a given Ioff:
Better gate overdrive vs Vcc.

➔ Higher mobility vs Planar:
More so at lower lower Vcc

Power-performance tradeoff scales better (vs Planar) as Vcc is reduced





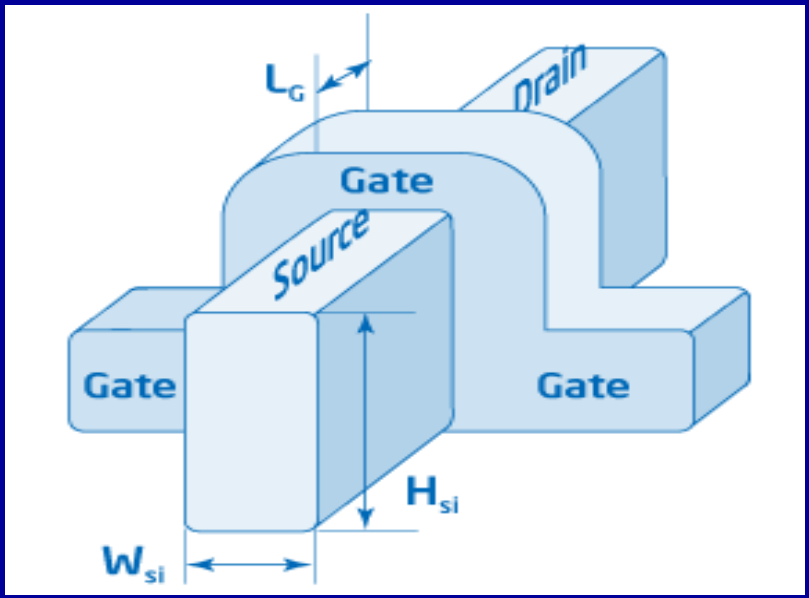


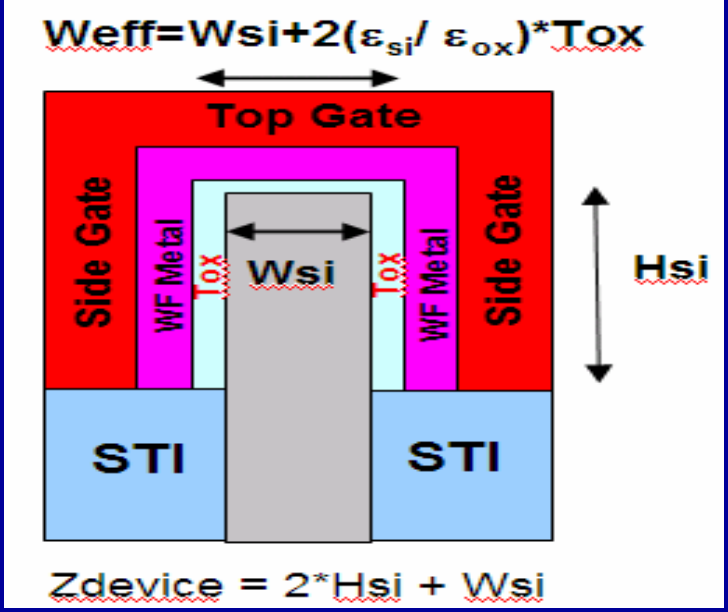
Multi-Gate Transistors: Implementation and Design

FinFET / Tri-Gate Transistor:

++ Self Aligned structure

-- Non-Planar structure





Tri-Gate Transistor

Tri-Gate / FinFET Value Proposition

Performance / Power:

+ Scale better at lower Vcc: *Better mobility & lower Vt*	**Reduce Active Power OR**
+ Operate at lower Leakage	**Reduce Standby Power**
+ Lower Channel Doping	**Lower BTBT: Lower $I_{JUNCTION}$** **Lower Cjp: Performance gain** **Reduce Standby Power**

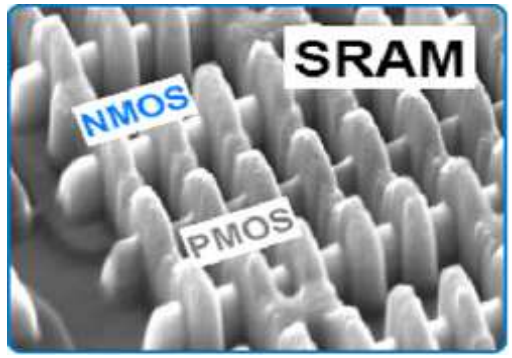
Random Dopant Fluctuation:

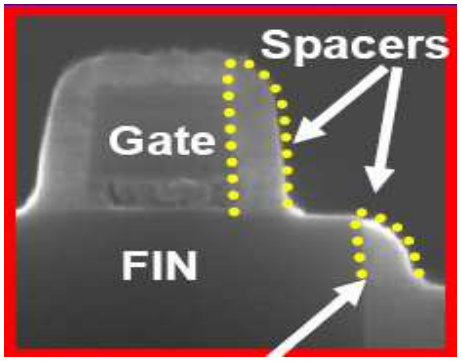
+ Lower Channel Doping	**Lower RDF. Better SRAM Vmin?**

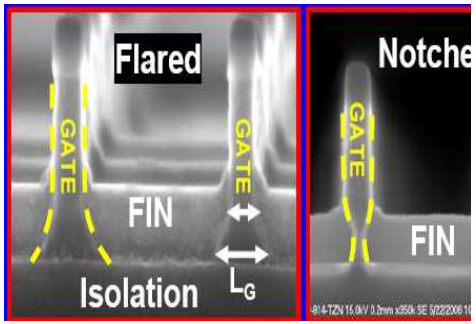
Multi-Gate Transistor is a serious contender for post-45nm CMOS nodes due to its many fundamental advantages

Process Challenges in Fabricating Tri-Gate / FinFET Transistors

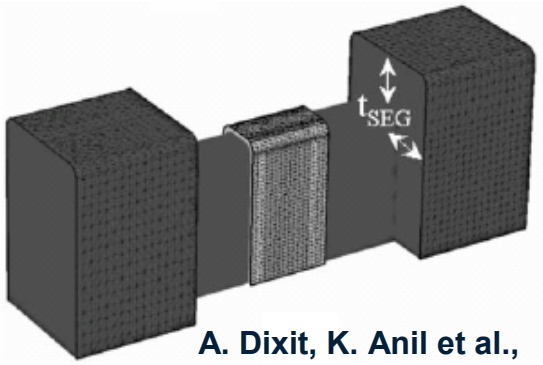
- **Non-Planarity**
- **Implementing high level of channel strain:**
  - Planar Ref= Highly strained and optimized device
- **Higher Rext:**
  - Selective epi S/D
  - Minimize spacer
- **Process control:**
  - Fin width control
  - Poly sidewall profiles







J. Kavalieros et. al. (Intel)
VLSI Symp 2006



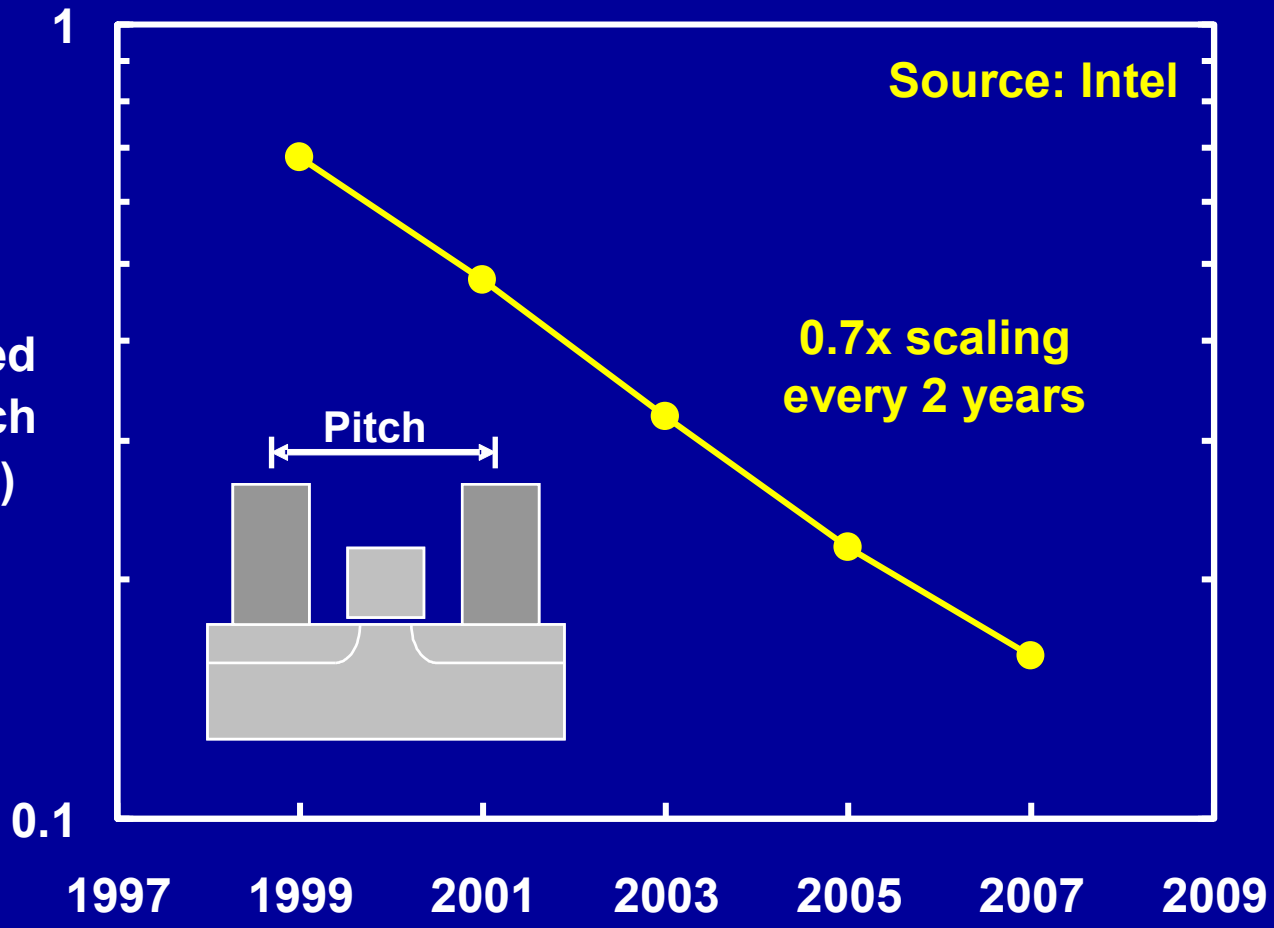
A. Dixit, K. Anil et al., Solid State Electronics, 2006

These concerns need to be successfully addressed for TriGate/FinFET Transistors to become mainstream.

Outline

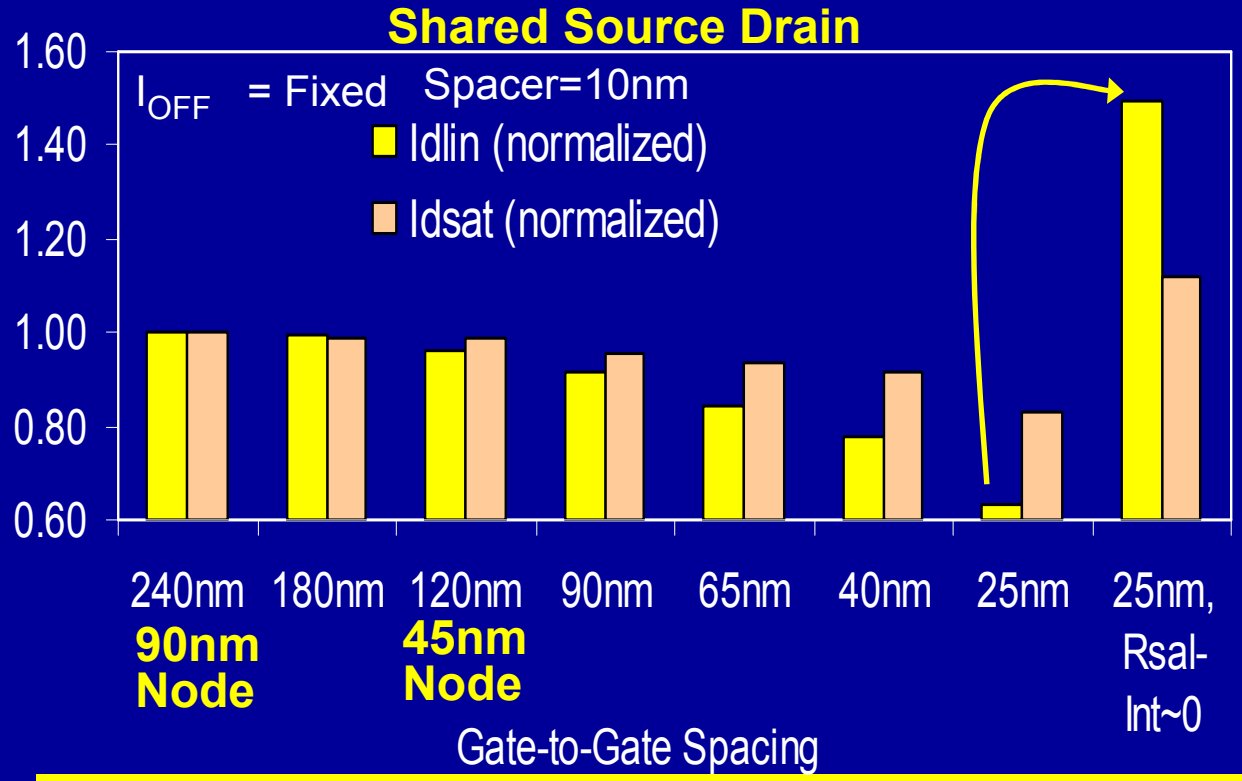
- **End of Traditional Scaling Era**
  - Traditional scaling limiters and implications
- **Intel's Response**
  - Uniaxial Strain (90nm and 65nm Nodes)
  - HiK + Metal Gate + Strain (45nm Node)
- **Challenges and Solutions Beyond 45nm Node**
  - **Higher Strain:** Ultimate limit of silicon mobility enhancement?
  - **Power Limitation:** Implications on future transistor structures
  - **Parasitics Dominated Era:** How to address increasing negative impact of parasitics?
  - **New Channel Materials:** III-V QW channels at Vcc~0.5-0.7V

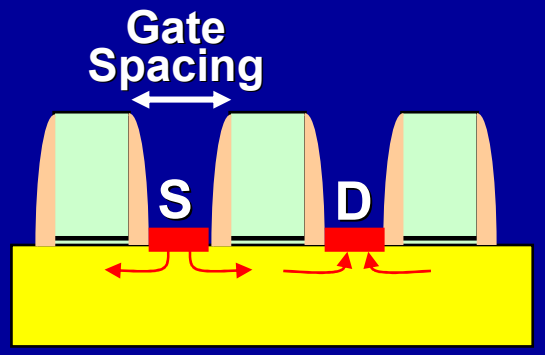
Density Scaling on Track (Gate Pitch)



Gate pitch scaling continues to follow Moore's Law showing 2x transistor increase per area every 2 years

Drive Current Degradation with Gate Pitch Scaling



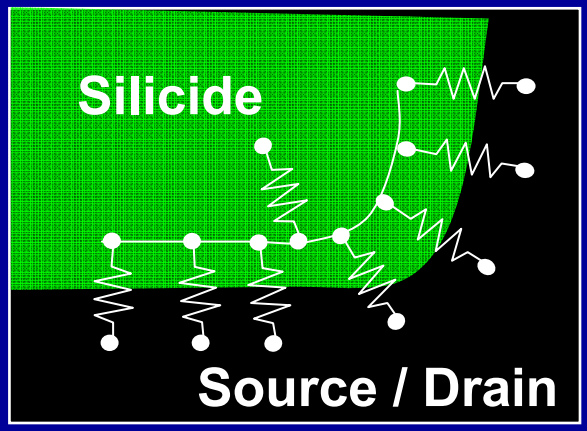


Shared Source Drain

- Beyond 45nm node, gate pitch scaling dramatically drive current dramatically due to increased resistance (shrinking S/D contact area)
- Dramatic performance gains expected if salicide interface resistance can be reduced.
- **Past:** Yield vs. density tradeoff
  Future: Transistor performance vs. density trade-off **(NEW PARADIGM)**

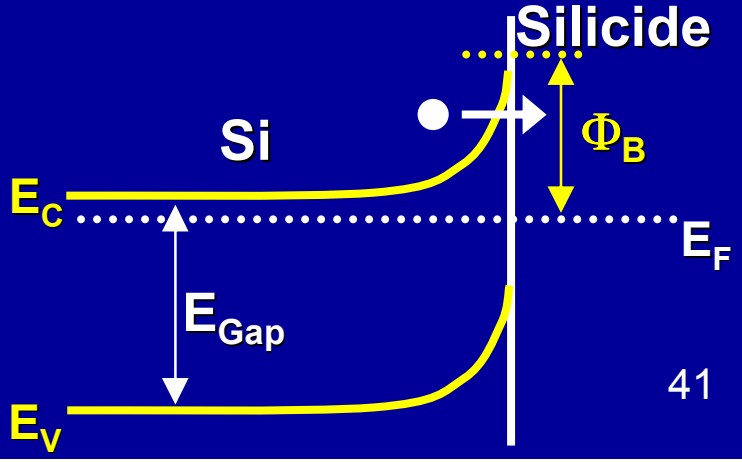
Innovative Solutions for Salicide Resistance Reduction

1. Increase S/D dopant electrical activation above solid solubility:
   Non-Equilibrium regime
2. S/D bandgap engineering to reduce barrier height: **Example: Strained SiGe S/D**
3. Explore new salicides with reduced barrier height: **Dual Salicide**



$$\rho_c \propto \exp\left(\frac{4\pi\Phi_B}{qh}\sqrt{\frac{m^*\varepsilon}{N_{surf}}}\right)$$

2 + 3 Key Challenge:
Interface states dominate band alignment (Fermi level pinning). Need to develop effective interface passivation techniques



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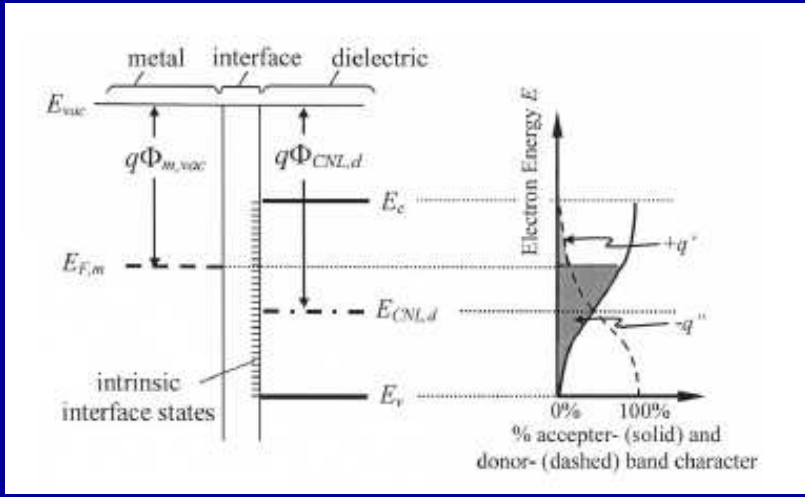
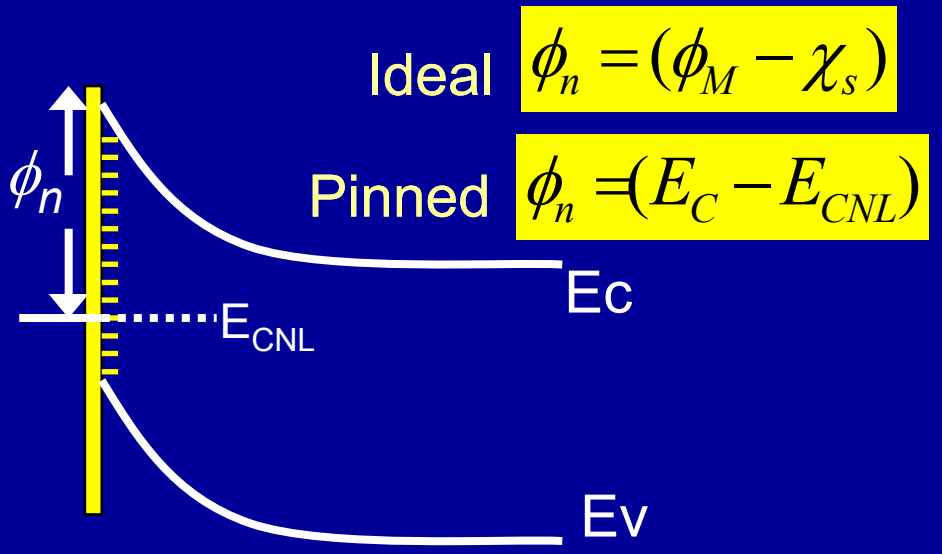
Fermi Level Pinning



Yeo, King and Hu, JAP, 15 Dec 2002



$$\phi_n = S(\phi_M - \chi_s) + (1-S)(E_C - E_{CNL})$$

- Fermi Level Pinning: Barrier height insensitive to metal work function
- Suppress Fermi level pinning by passivating dangling bonds
  Enables dual-metal work function materials with ϕ_M near Ec and Ev
- OR Effective barrier pinned close to desired level (Ev or Ec)

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High Mobility n-Channel Materials

Properties of some NMOS candidates

Material/Property	Si	Ge	GaAs	InAs	InSb
m_{eff}^*	0.19	0.08	0.067	***0.023***	***0.014***
μ_n (cm^2/Vs)	1600	3900	9200	***40,000***	***77,000***
E_G (eV)	1.12	0.66	1.42	***0.36***	***0.17***
ε_r	11.8	16	12.4	14.8	***17.7***

Source: A. Pethe (Stanford)

Ultimate Channel: Ballistic Transport

$$I_{DSAT} = WC_G \upsilon_S(0)(V_{GS} - V_T)$$

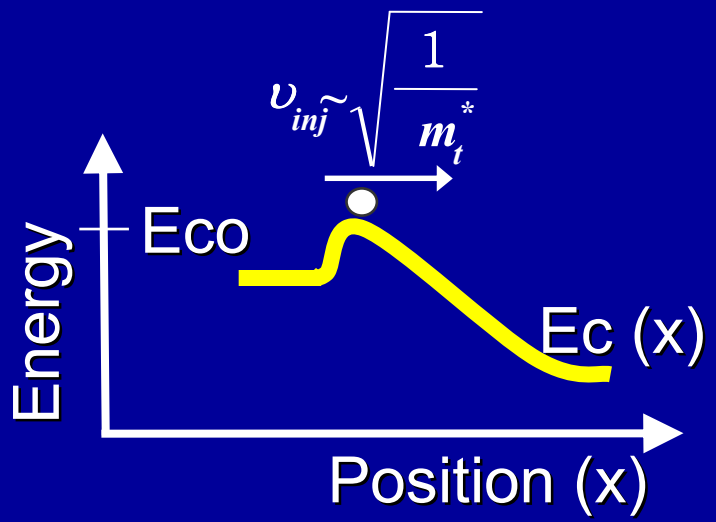
$$\frac{1}{\upsilon_S(0)} = \frac{1}{\upsilon_{inj}} + \frac{1}{\mu_{eff} E(0^+)}$$

Ballistic

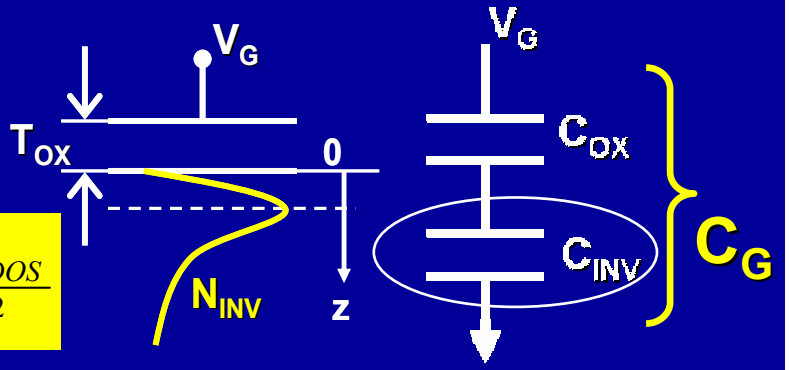
$\uparrow \mu_{eff}$

$$I_{DSAT} = WC_G(V_{GS} - V_T)\upsilon_{inj}$$

$$\upsilon_{inj} = \sqrt{\frac{2kT}{\pi m_t^*}}$$



$$C_{INV} \sim \frac{q^2 m_{DOS}^*}{\pi\hbar^2}$$

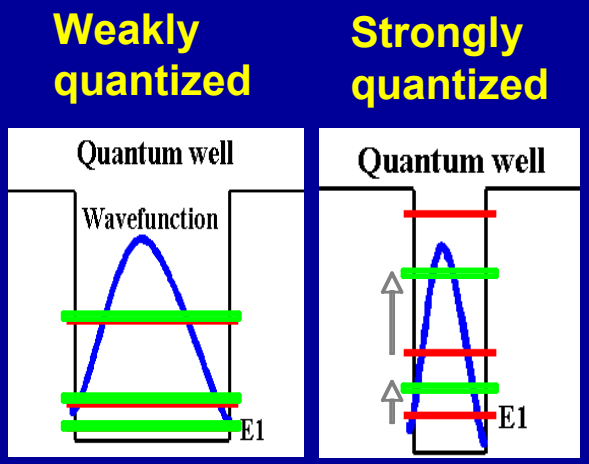


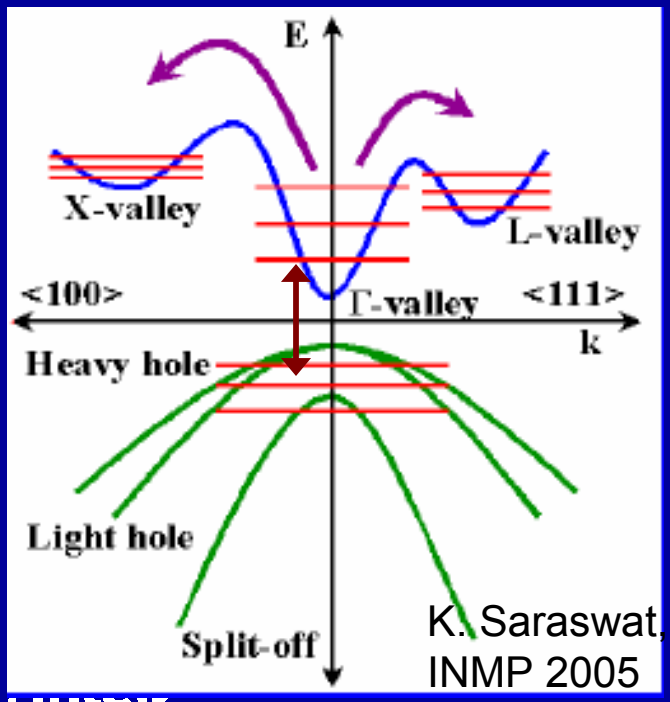
Quantum Capacitance important at thin T_{OX}

High Performance in Ballistic Regime:

1. Low m_t^* along channel direction → High υ_{inj} → Maximize I_{DSAT}
2. High m_{DOS}^* → High C_{GATE} → High Q_{INV} → Maximize I_{DSAT}

High Mobility III-V Channel= High Performance?





- III-V materials (GaAs, InSb, InAs) being investigated due to small Γ-valley m*
  → ↑υ_{inj} → ↑I_{DSAT}
- However, lower m* leads low DOS
  → ↓Q_{INV} → ↓I_{DSAT}
- Γ-valley lifts up due to confinement (1/m*)
  Charge transfers into X & L valleys with high m*
  → ↓υ_{inj} → ↓I_{DSAT}
- Small E_G (InAs, InSb):
  → High BTBT leakage
  → Tailor bandgap by QW confinement
- Higher ε:
  → Higher sub-T slope (poor SCE)

Projecting III-V NMOS performance based on simplistic models could lead to erroneous performance assessment. Need detailed physics modeling + fabricate devices

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Requirements for Building a Competitive III-V Channel Transistor Technology (V_{CC}~ 0.5-0.7V)

- Integrate III-V layers on large Silicon wafers
- Develop HiK dielectric compatible with III-V channels
- Determining PMOS material to go with NMOS
- Insertion 15nm node or beyond. Meet L_G< 20nm.
  III-V devices may need to be Tri-Gate / FinFET structure.
  It is expected to be scalable beyond first node.

III-V channel materials will have to simultaneously meet <u>multiple</u> requirements to be serious contenders as replacement for Strained-Si channel transistors

Transistor Feature Set Mapping to CMOS Nodes: Potential Roadmap

TODAY 65nm Node	45nm Node	32nm Node	22/15nm Nodes
• Process induced strain+ (2nd gen) • Gate Oxide with poly-Si Gate • NiSi	• **Hik + MG (Intel)** • Process induced strain ++ • NiSi	• HiK + MG **(Intel: 2nd Gen.)** • Process induced strain +++ • NiSi • **Alternative wafer orientation?** • **Dopant super-activation?**	• HiK + MG (3rd gen) • Process induced strain ++++ • Alternative wafer orientation? • Dopant super-activation? • **Multi-Gate FET's with strained Si?** • **Next generation silicide /contacts?**

Challenging but feasible roadmap for scaling logic CMOS technology down to 15nm CMOS Node with Si Channel.

Transistor Feature Set Mapping to CMOS Nodes: Potential Roadmap

15nm Node

- Multi-Gate FET's with HiK/MG and strained-Silicon channel
- Next generation silicide /contacts

ACADEMIA TOP FOCUS

Beyond 15nm Node

VERY SPECULATIVE

- Vcc < 0.7V (Power Limitations)
- Scaled Multi-Gate Transistors with ultra-low resistance nano-contacts
- Alternative Channel Multi-Gate FET (III-V, strained Ge QW) with ultra-low resistance nano-contacts
- Ultra-low Power: (Vcc<0.5V)
  Super steep sub-T slope (<<60 mV/dec)
  Would require tunneling limited transport
  - Reasonable Ion?
  - Tight control?
- Carbon Nanotubes?

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Summary / Key Message

- Transistor structure and material innovations pioneered at Intel such as uniaxial strained silicon and high-k/metal gate have enabled Intel to scale planar CMOS beyond 90nm node.
- Achieving high performance at low Vcc is critical in a power limited world and will play important role in transistor architecture and front-end feature set selection.
- Multi-Gate transistors have potential to improve performance vs. power tradeoff and enable lower Vcc on products
- Improving transistor parasitics is as important as improving intrinsic transistor performance. Needs higher focus!!
- Roadmap for scaling CMOS technology during next 10 years is quite challenging but feasible

THANK YOU!