# Low Frequency Noise in Advanced MOS Transistors

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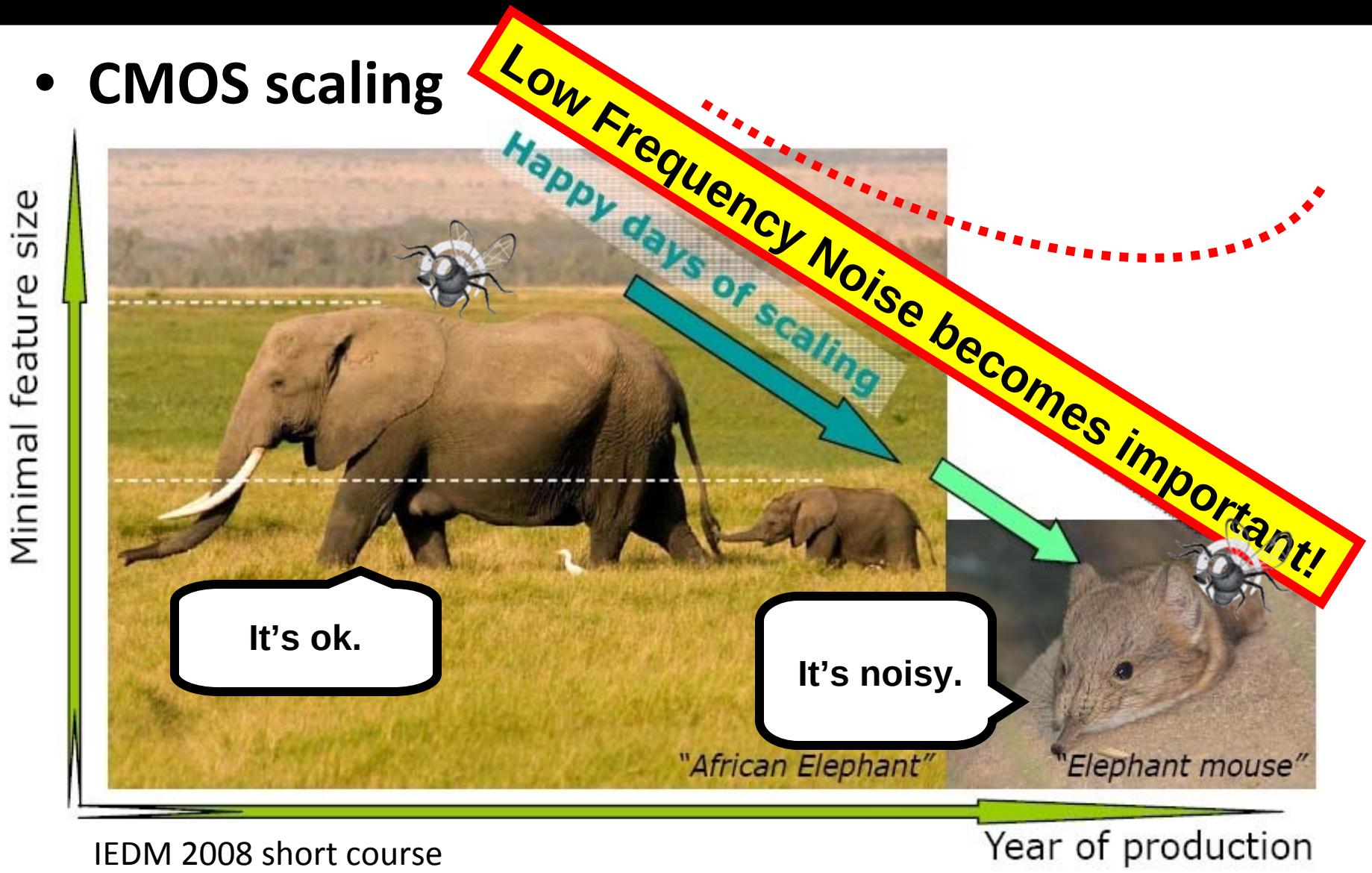
# Motivation

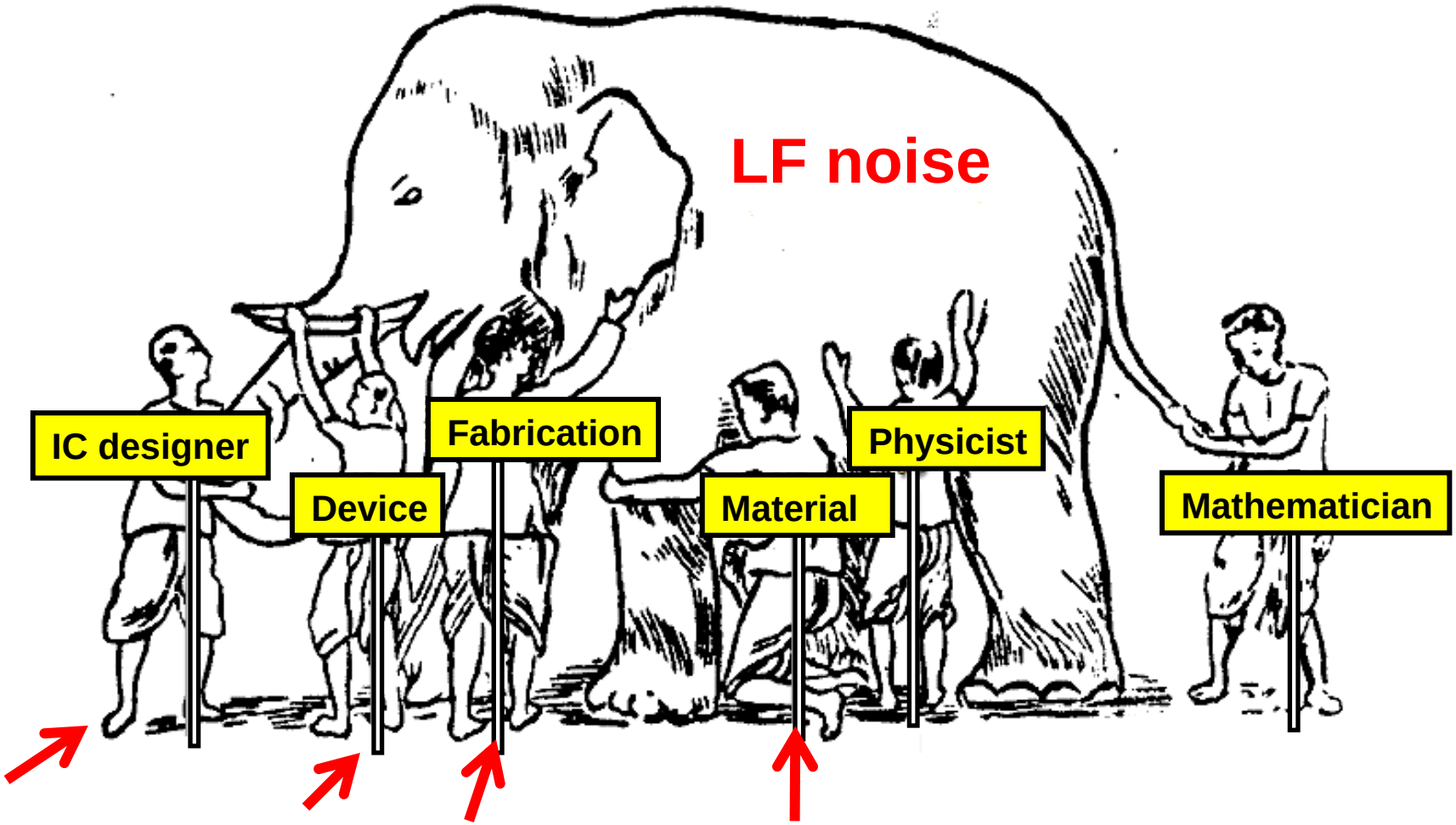
- **CMOS scaling**




IEDM 2008 short course

# Motivation

- **Low Frequency (LF) noise**



# Outline

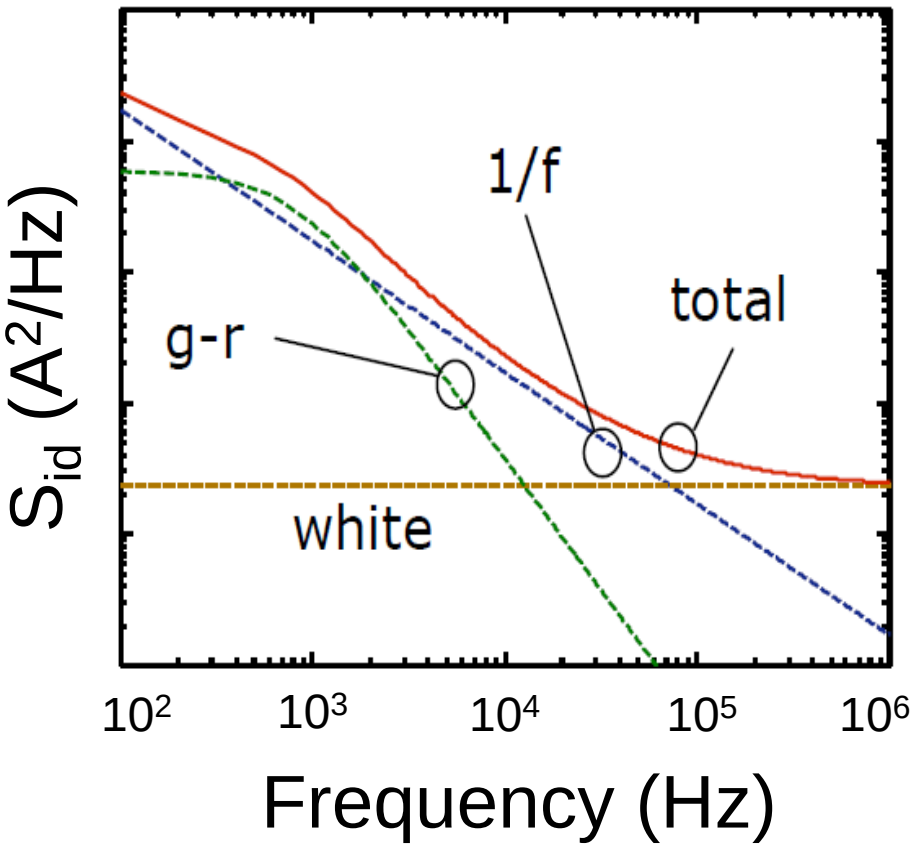
- Introduction
- Methodology
- SiGe channel
- Size effect
- Conclusions

# Outline

- **Introduction**
  - Why LF noise is important?
  - The origin of LF noise
  - CMOS scaling
- **Methodology**
- **SiGe channel**
- **Size effect**
- **Conclusions**

# Why LF noise is important?

- **Noise in a MOSFET**

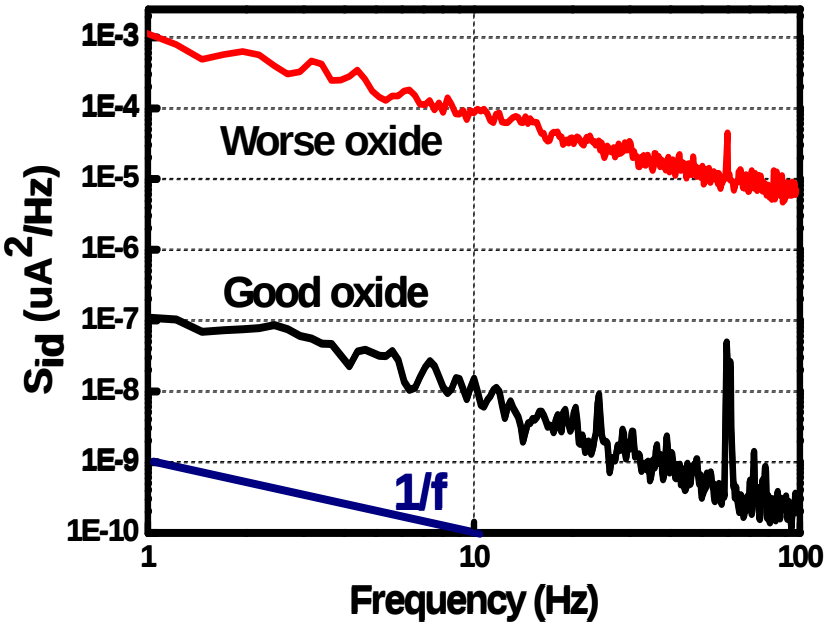


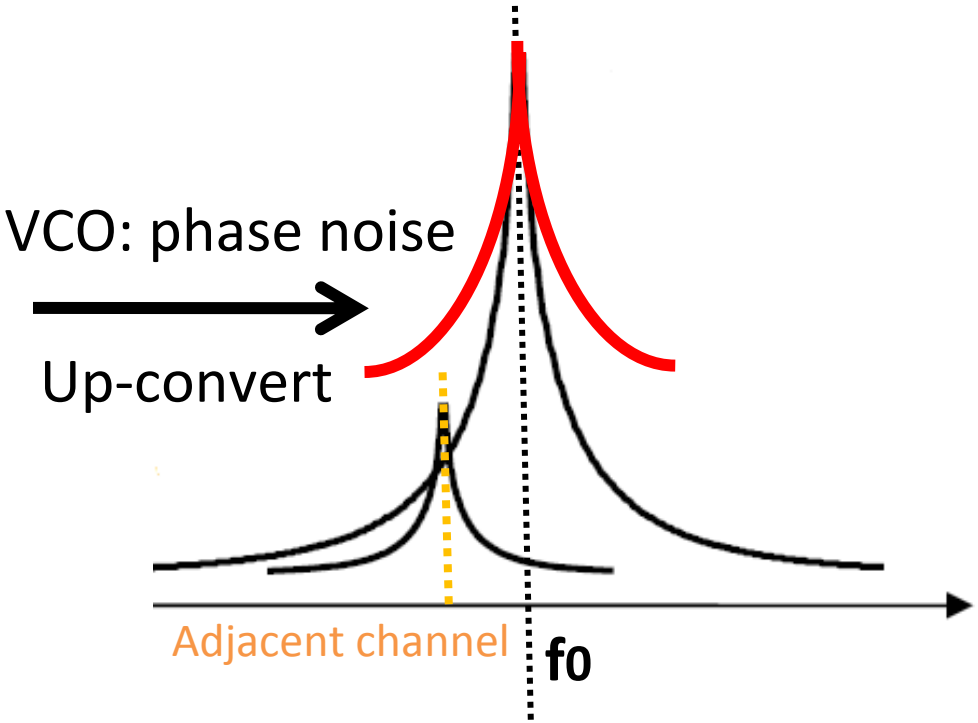

- **White noise:** thermal noise and shot noise.
- **1/f noise:** certain trap distribution or fluctuation in mobility.
- **G-R noise:** trap/de-trap mechanism; one special case is **RTN**.

Low frequency (LF) noise

# Why LF noise is important?

- **Analog domain**

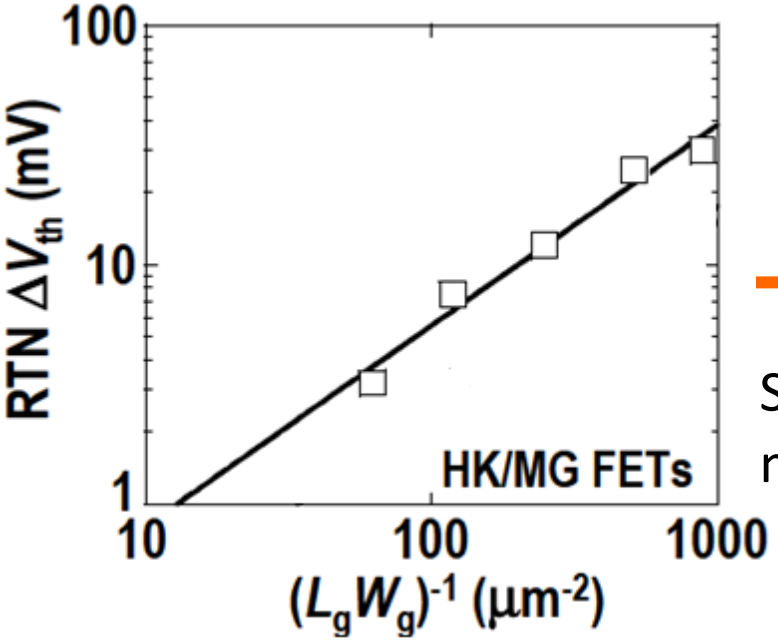


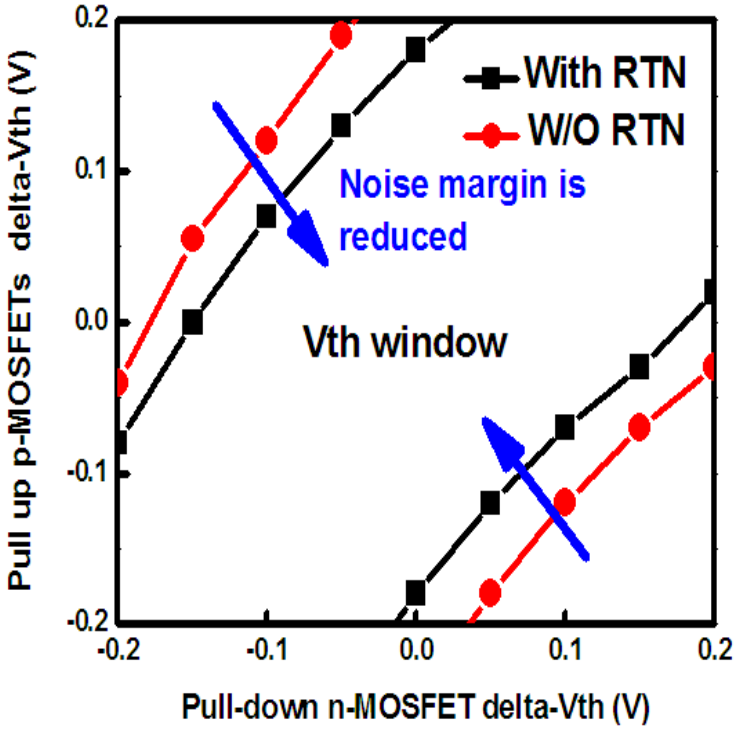

  - LF noise is up-converted and causes phase noise.
  - Phase noise limits channel capacity.

# Why LF noise is important?

- **Digital domain**




SRAM: noise margin




N. Tega, VLSI symp. 2009, p. 50-51.

- LF noise increases with scaling.
- Noise margin becomes small.

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  - Why LF noise is important?
  - The origin of LF noise
  - CMOS scaling
- **Methodology**
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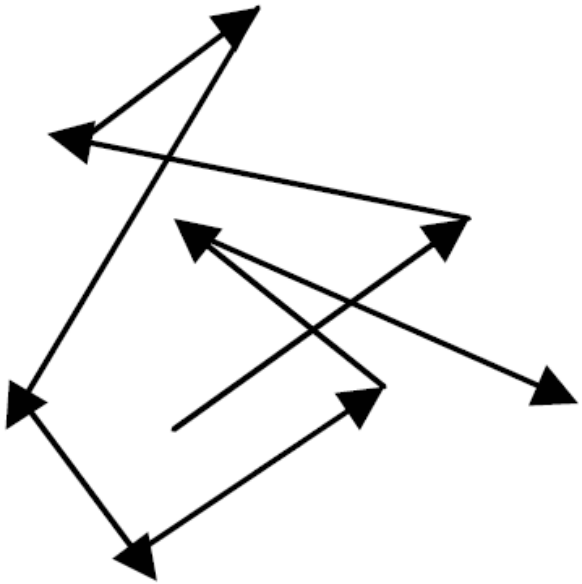
- **Size effect**
- **Conclusions**

# The origin of LF noise

- **Two schools**



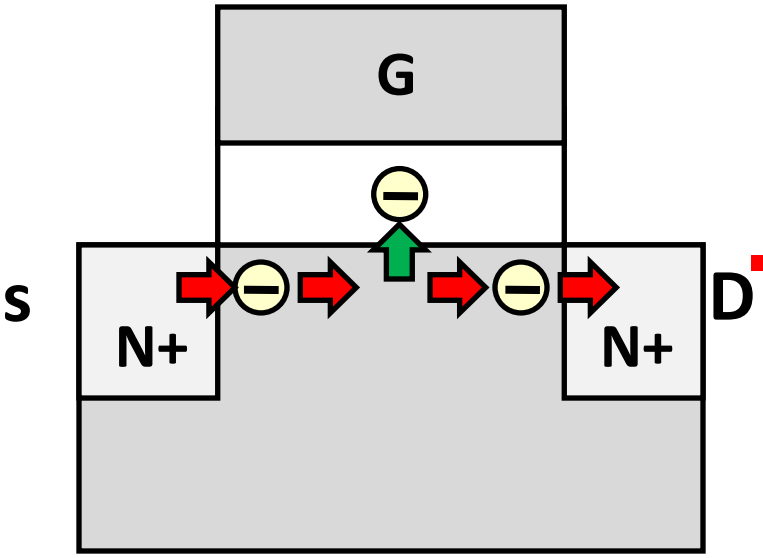
$$\sigma = \mu_{eff} N$$

  - Conductivity fluctuation.
  - Two schools: number fluctuations ($\Delta N$) and mobility fluctuations ($\Delta \mu$).

# The origin of LF noise

- **ΔN model: one trap**

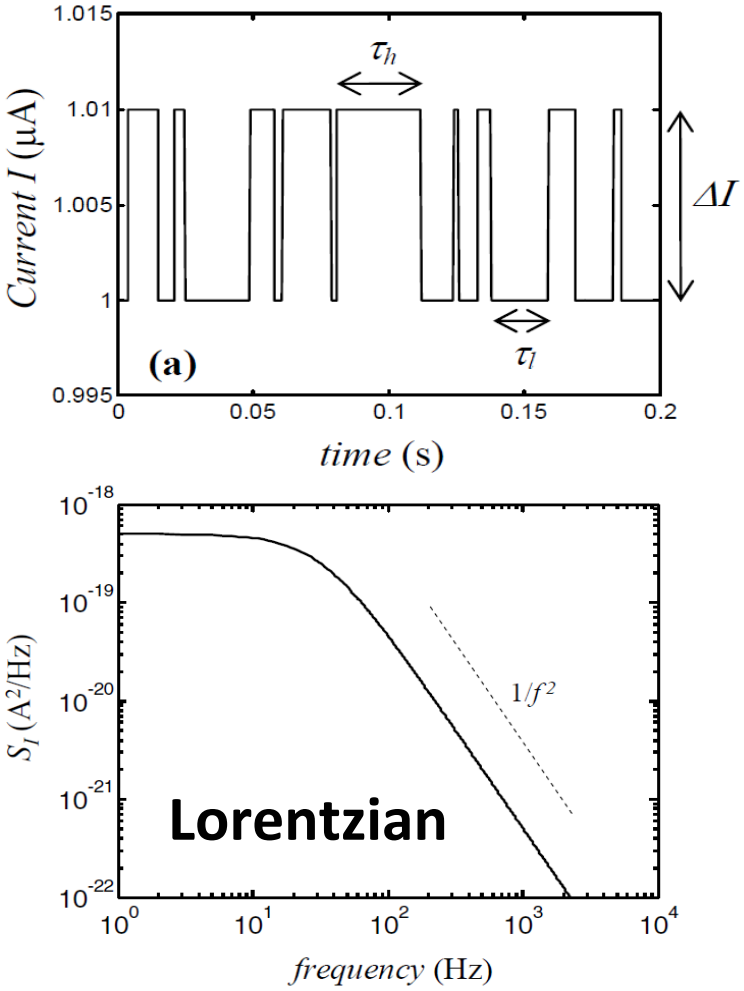
**one trap/de-trap**




A. McWhorter, *Semi. Surf. Phys.*, 1957.

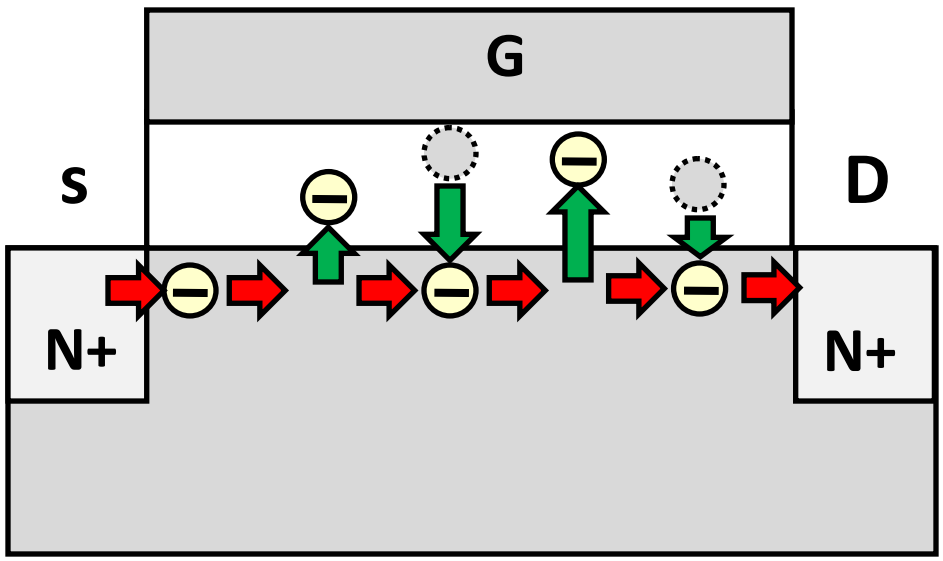
**Surface effect**

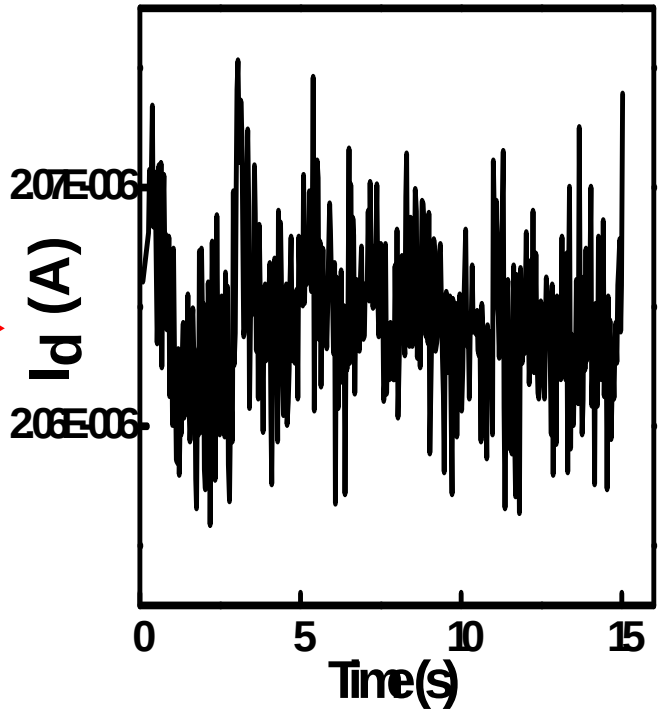
**Random telegraph noise**



# The origin of LF noise

- **ΔN model: a lot of traps**



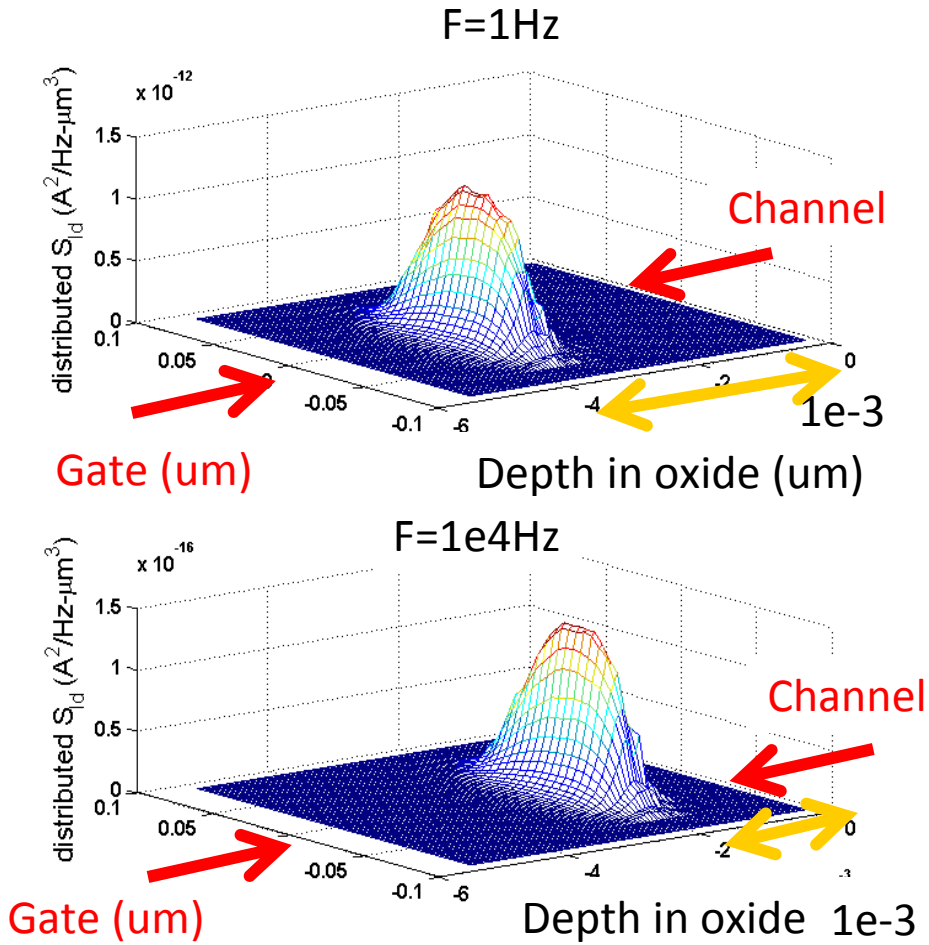




A. McWhorter, *Semi. Surf. Phys.*, 1957.

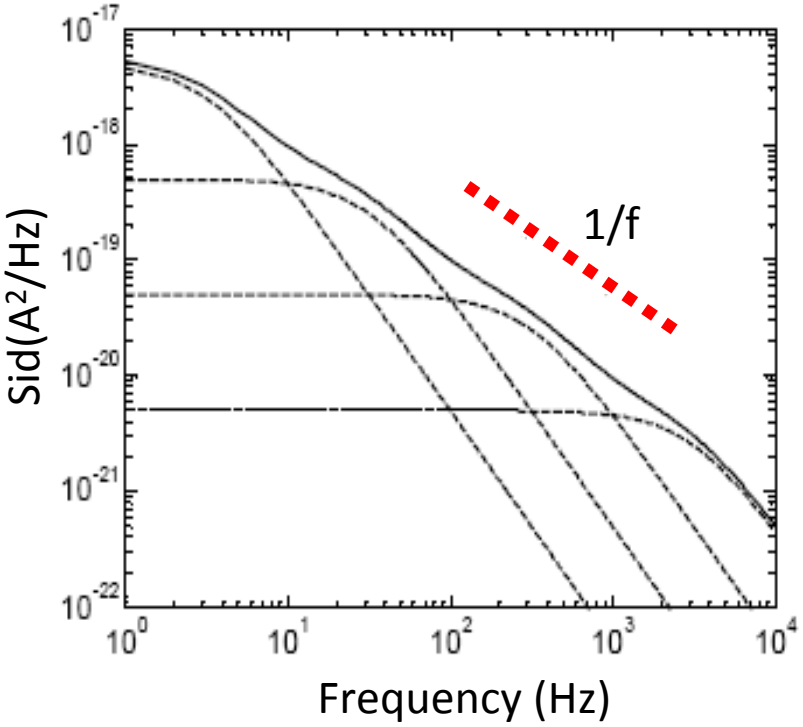
**Correlated Δμ is also induced.**

# The origin of LF noise

- **ΔN model: a lot of traps**



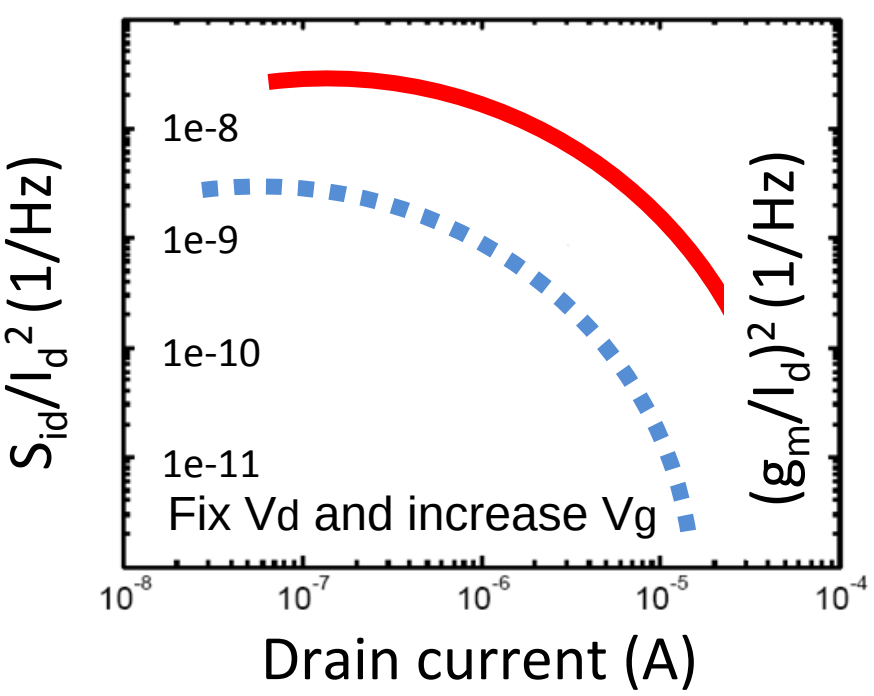

SISPAD 2006, Y. Liu

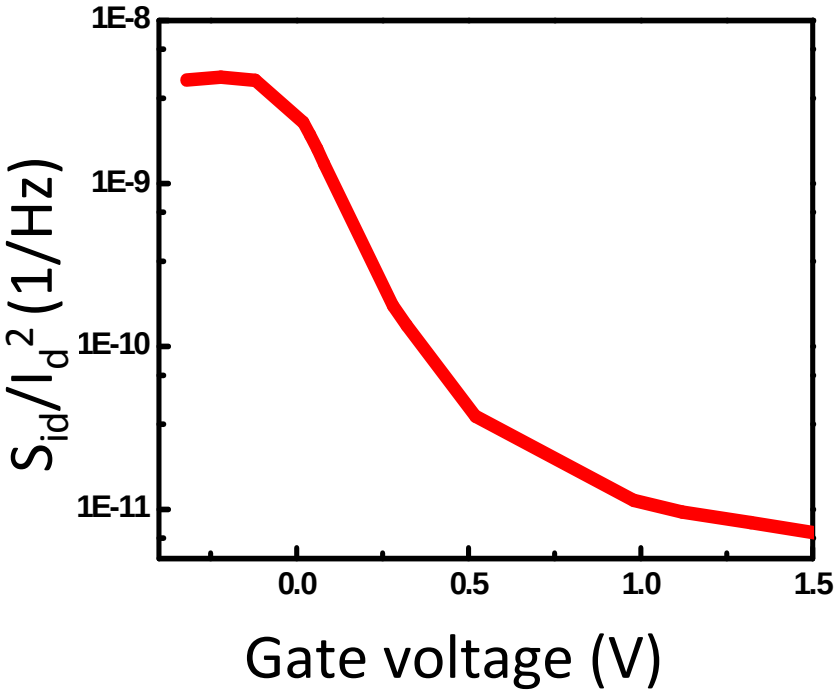



– Sum of Lorentzians: 1/f noise

# The origin of LF noise

- **ΔN model: $I_d$ and $V_g$ dependence**

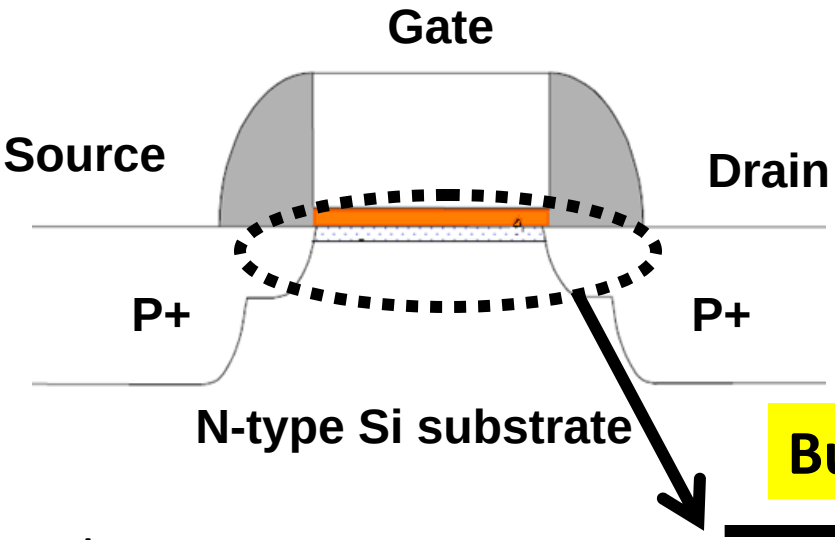


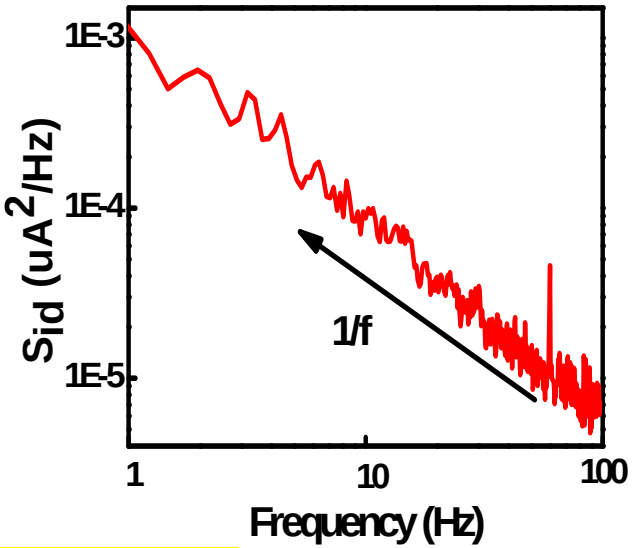




- $I_d$: $S_{id}/I_d^2 \alpha (g_m/I_d)^2$.
- $V_g$: flat in weak inversion.

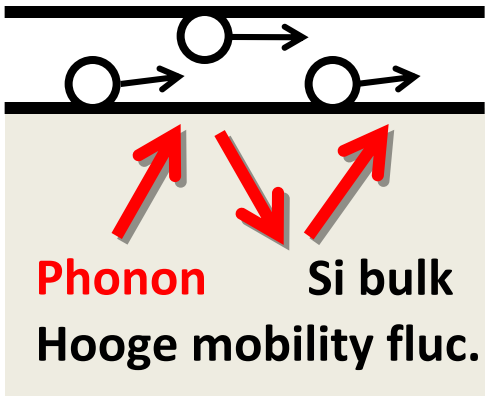
# The origin of LF noise

- **Δμ model**
  - Bulk phonon scattering




**Bulk effect**



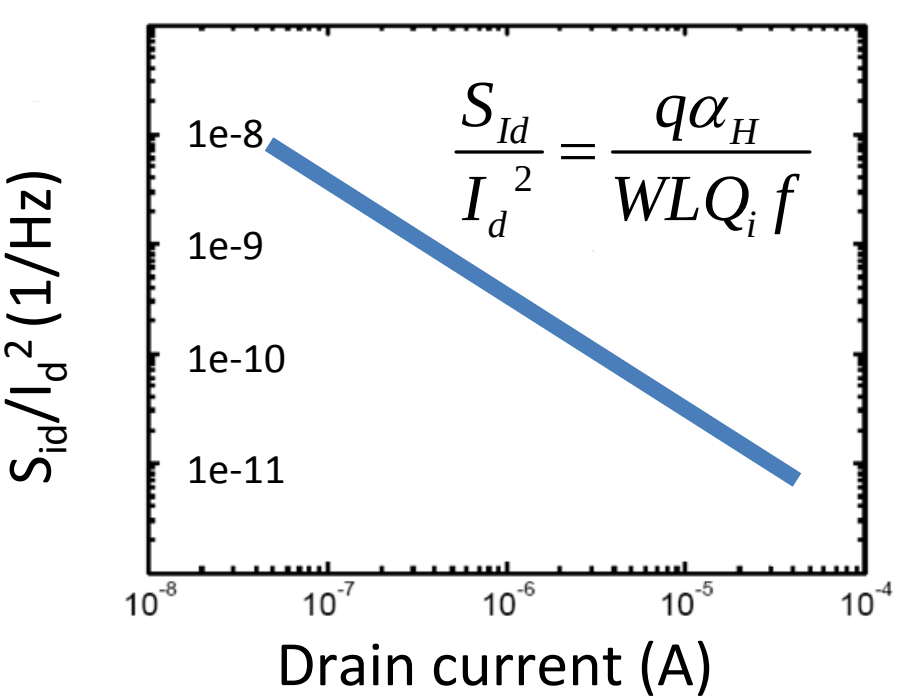

  - Empirical equation

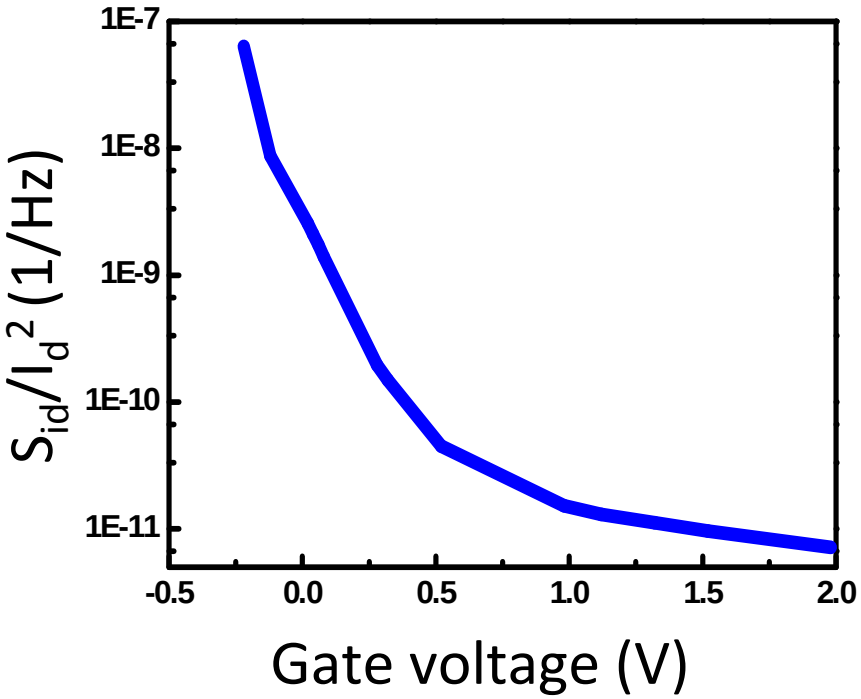
$$\frac{S_{Id}}{I_d^{\,2}} = \frac{q\alpha_H}{WLQ_i f}$$

T-ED 1994, F. N. Hooge

# The origin of LF noise

- **Δμ model: $I_d$ and $V_g$ dependence**

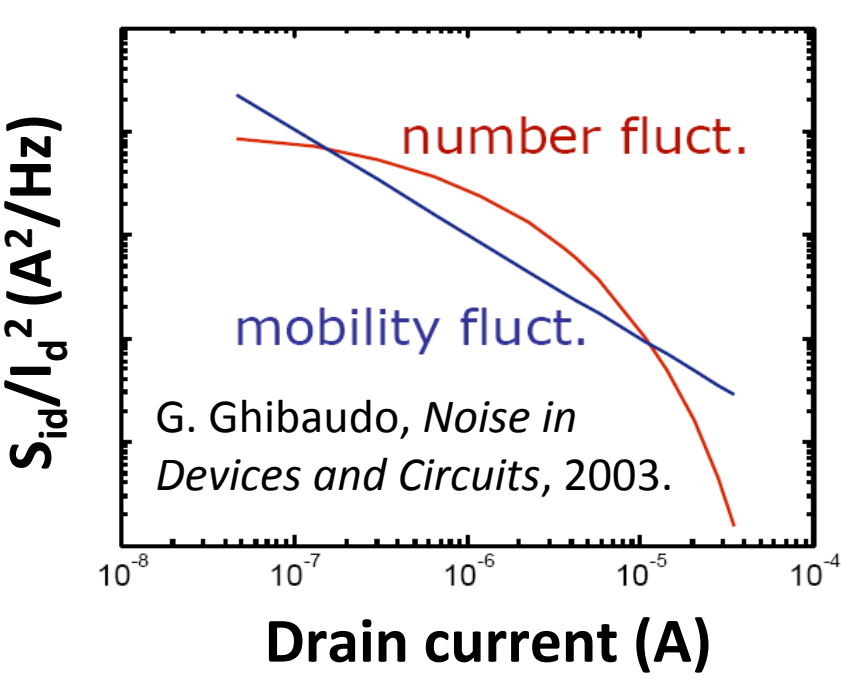


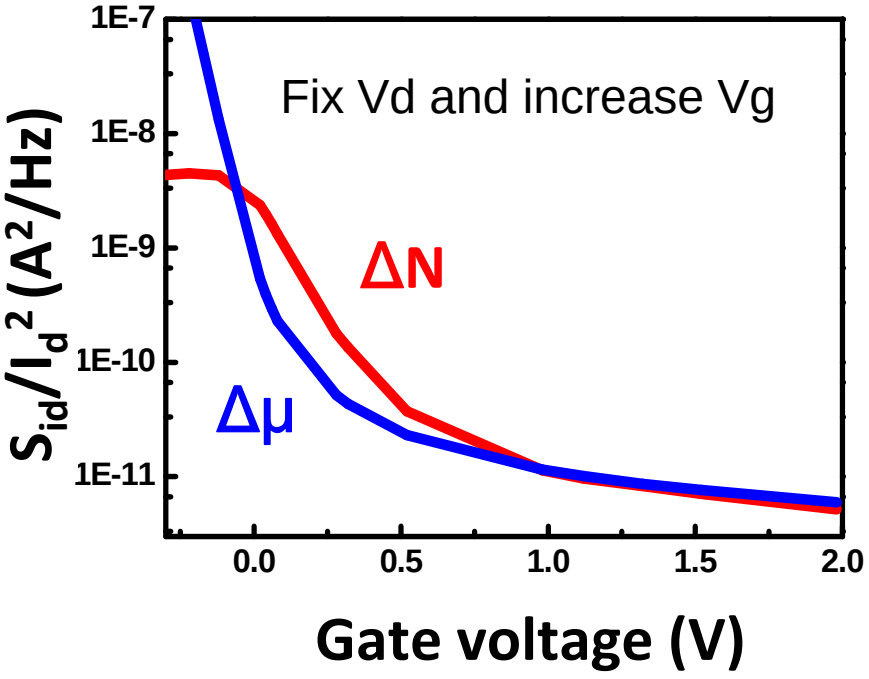




- $I_d$: $S_{id}/I_d^2$ α $1/I_d$.
- $V_g$: $S_{id}/I_d^2$ increases when $V_g$ decreases.

# The origin of LF noise

- **ΔN or Δμ?**



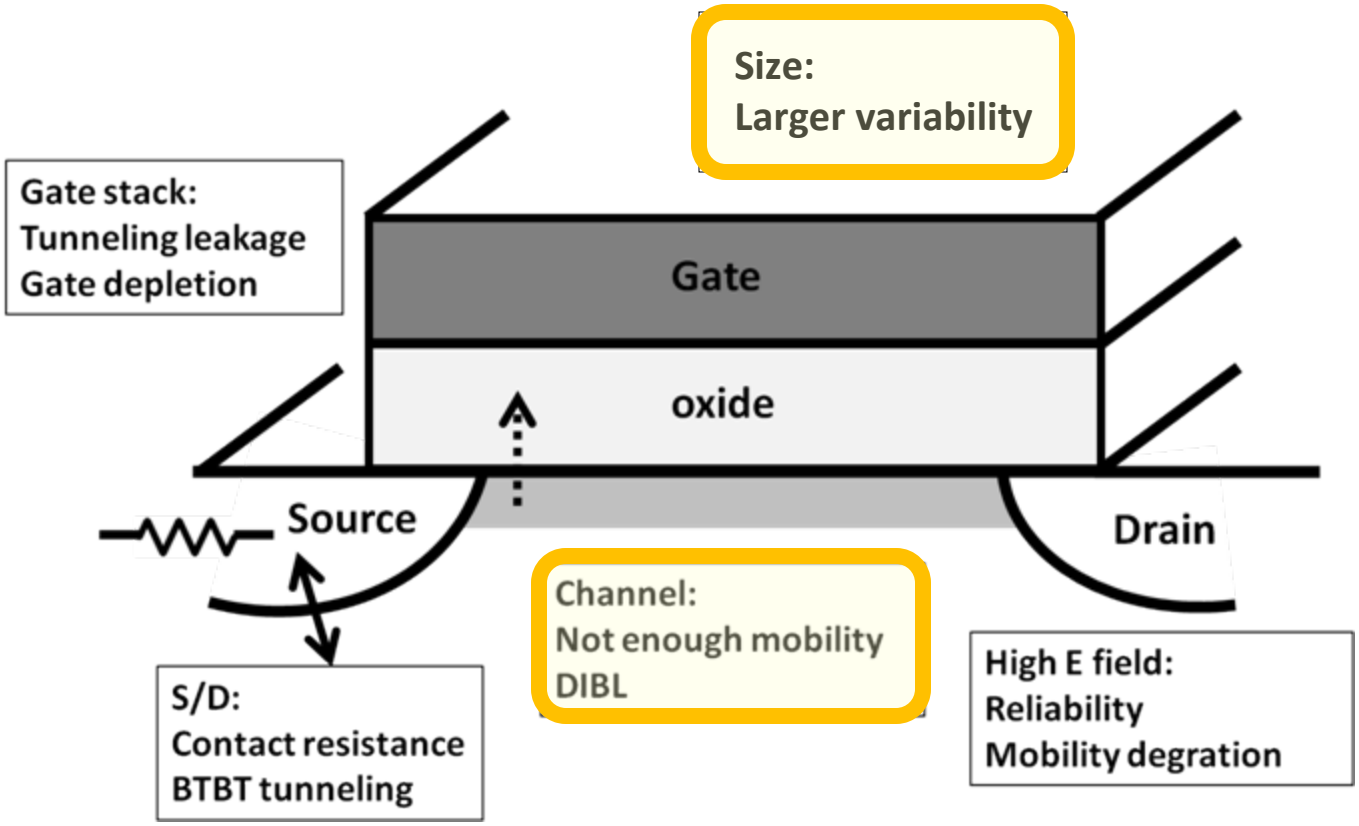




– Different trend in $I_d$ and $V_g$ dependence.

# Outline

- **Introduction**
  - Why LF noise is important?
  - The origin of LF noise
  - CMOS Scaling
- **Methodology**
- **SiGe channel**
- **Size effect**
- **Conclusions**

# CMOS scaling

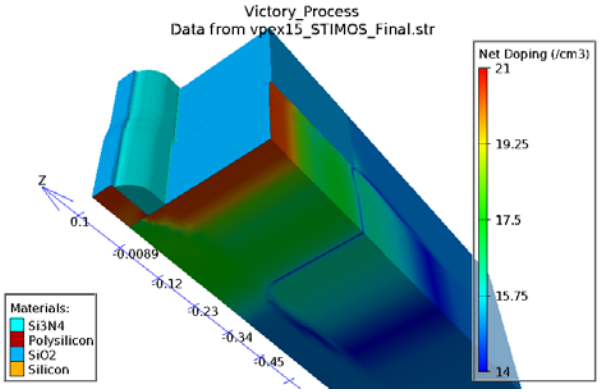



– CMOS scaling: provide new opportunity to optimize LF noise.

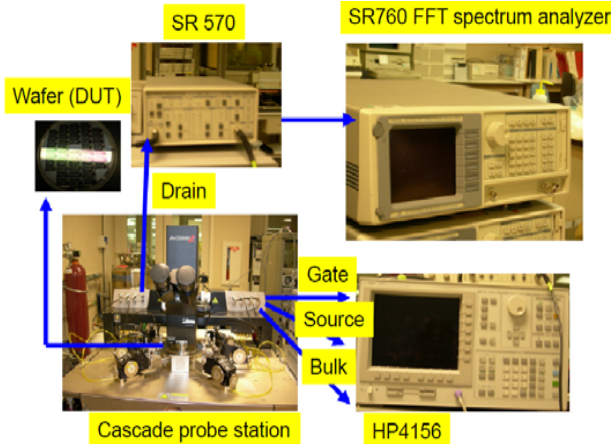
# Outline

- Introduction
- **Methodology**
  - Overview
  - TCAD simulations
  - Noise characterization
- SiGe channel
- Size effect
- Conclusions

# Overview




**TCAD simulations**




**Noise characterization**

**Explain low frequency noise mechanism**

# Outline

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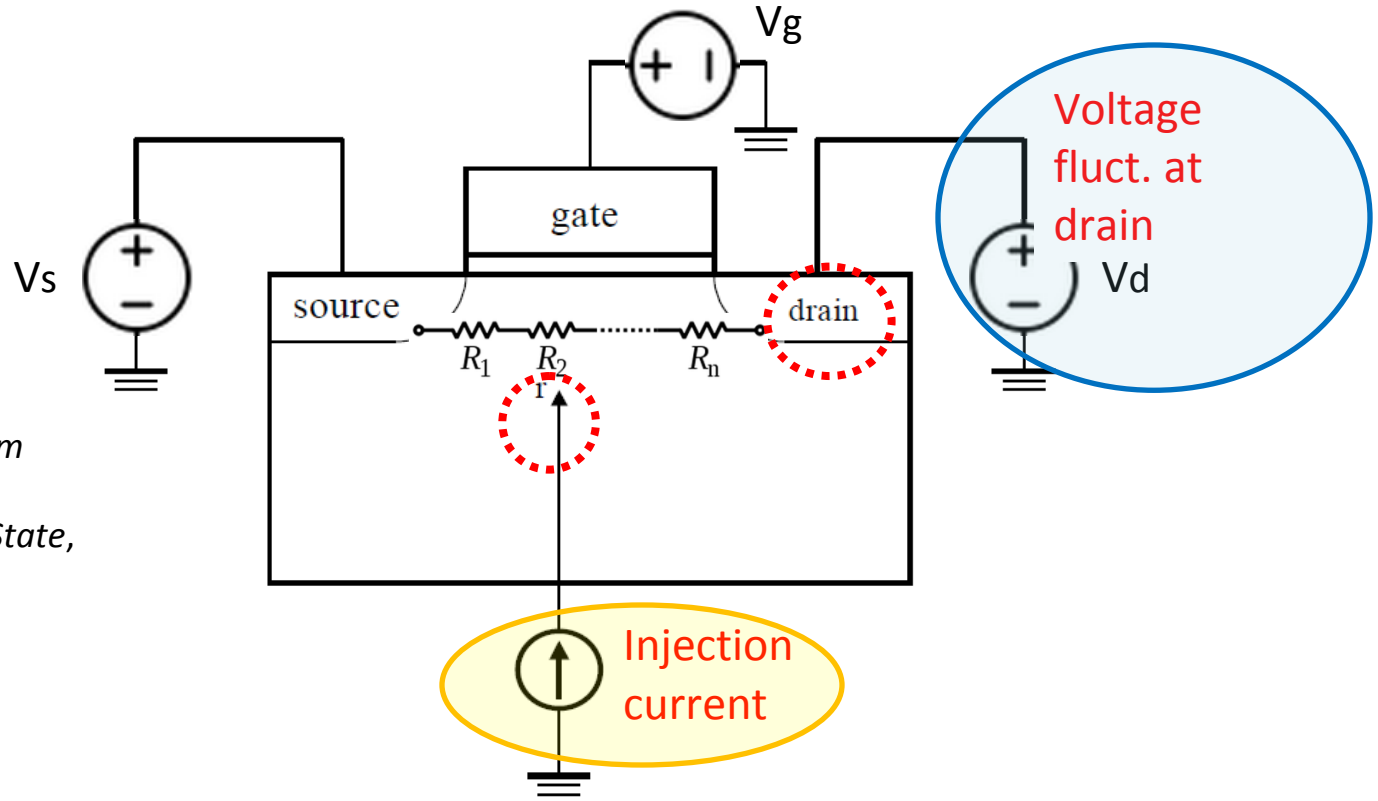
# TCAD simulation

$$S_{id\_total} = S_{id\_\Delta N} + S_{id\_\Delta \mu}$$

- Total noise is the sum of ΔN and Δμ.
- No correlation.

# TCAD simulation

- **Impedance field method (IMF)**

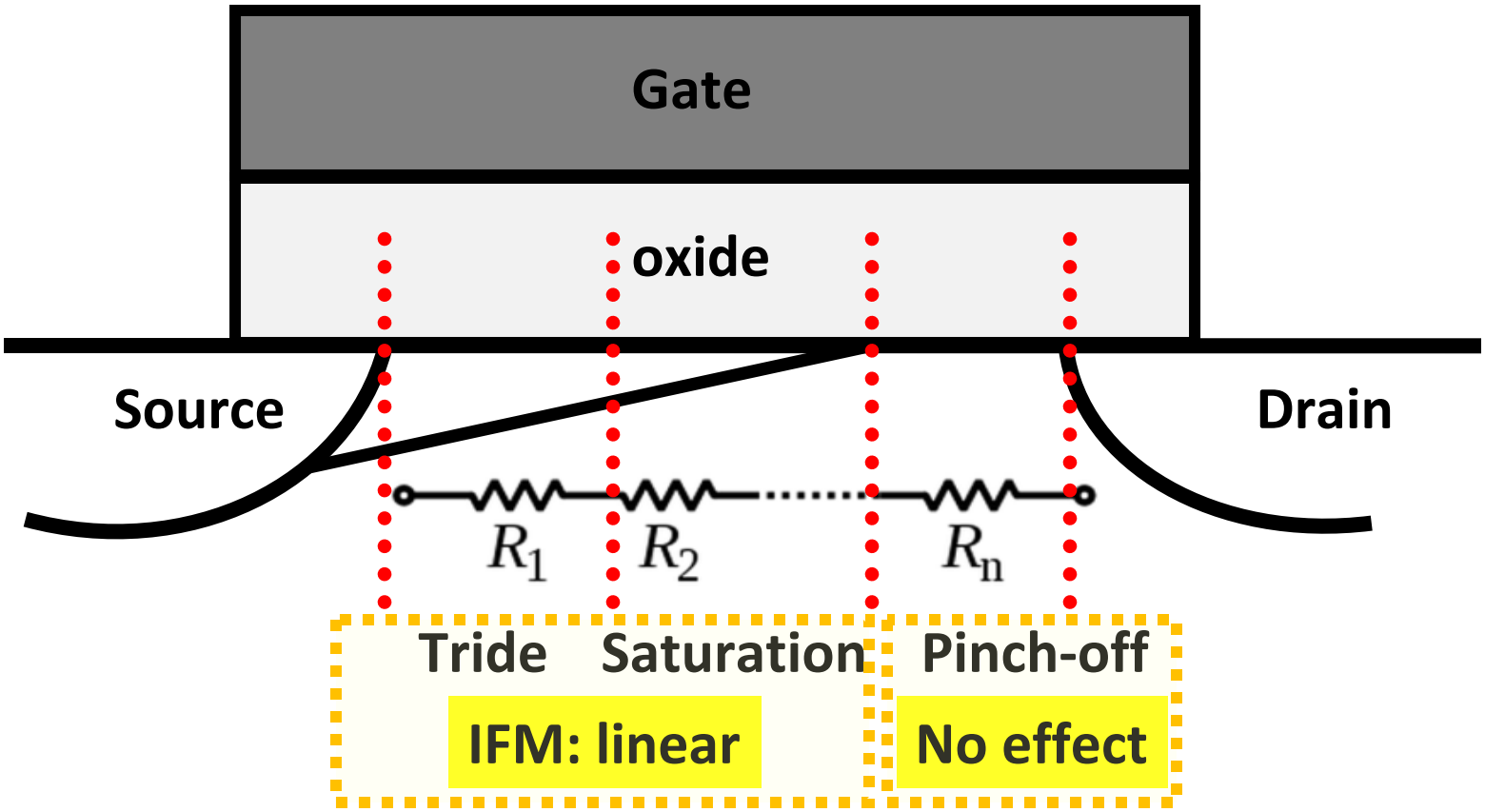



W. Shockley, *Quantum Theory of Atoms, Molecules and Solid State*, 1966, pp. 537–563.

$$Z_{kr} = \frac{\text{Voltage fluctuation at kth electrode}}{\text{Injected current at r in the device}}$$

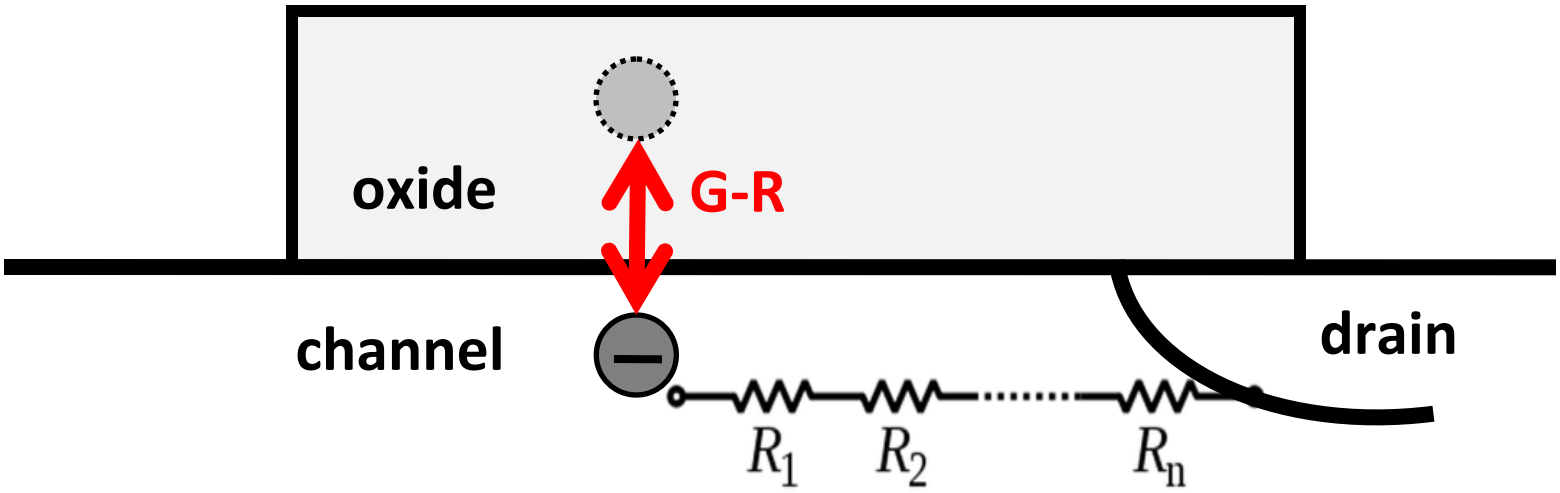
# TCAD simulation

- **Impedance field method (IFM)**



# TCAD simulation

- **ΔN model**




  - Noise source is inside oxide.
  - A rate equation to correlate oxide traps and channel carriers and then apply IMF to calculate $S_{id}$.

# TCAD simulation

- **Δμ model**

~1e-5 for Si material

$$\frac{S_{Id}}{I_d^{\,2}} = \frac{q\alpha_H}{WLQ_i f}$$

Extract from TCAD

– Extract parameters from TCAD simulations such as $Q_i$.

IEEE T-ED 2008, C.-Y. Chen

# Outline

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  - Noise characterization
- SiGe channel
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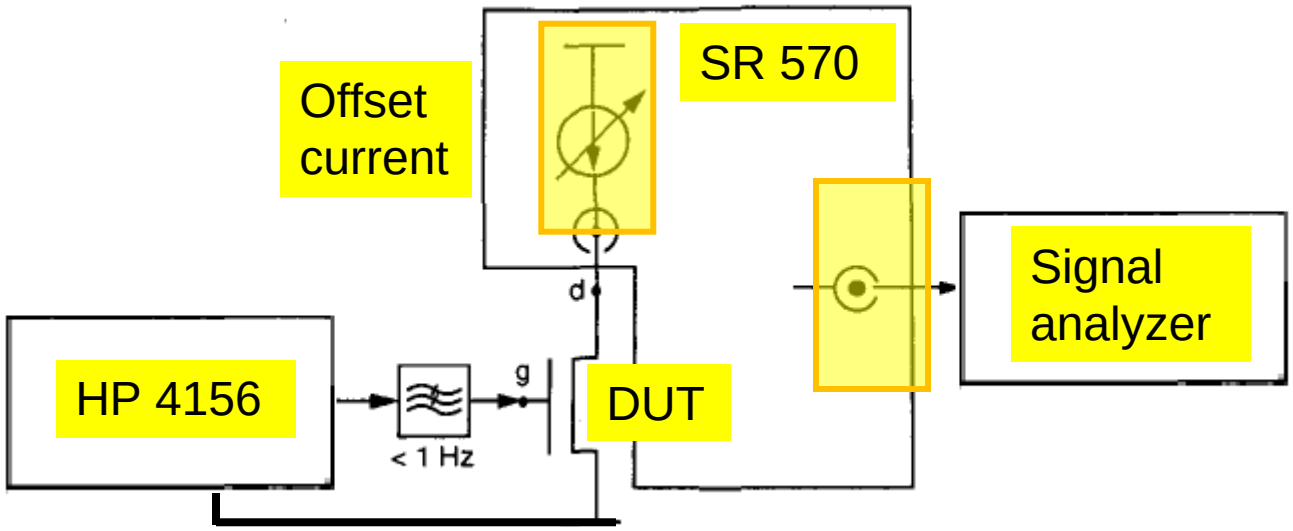
# Noise characterization

- **Basic schematic**

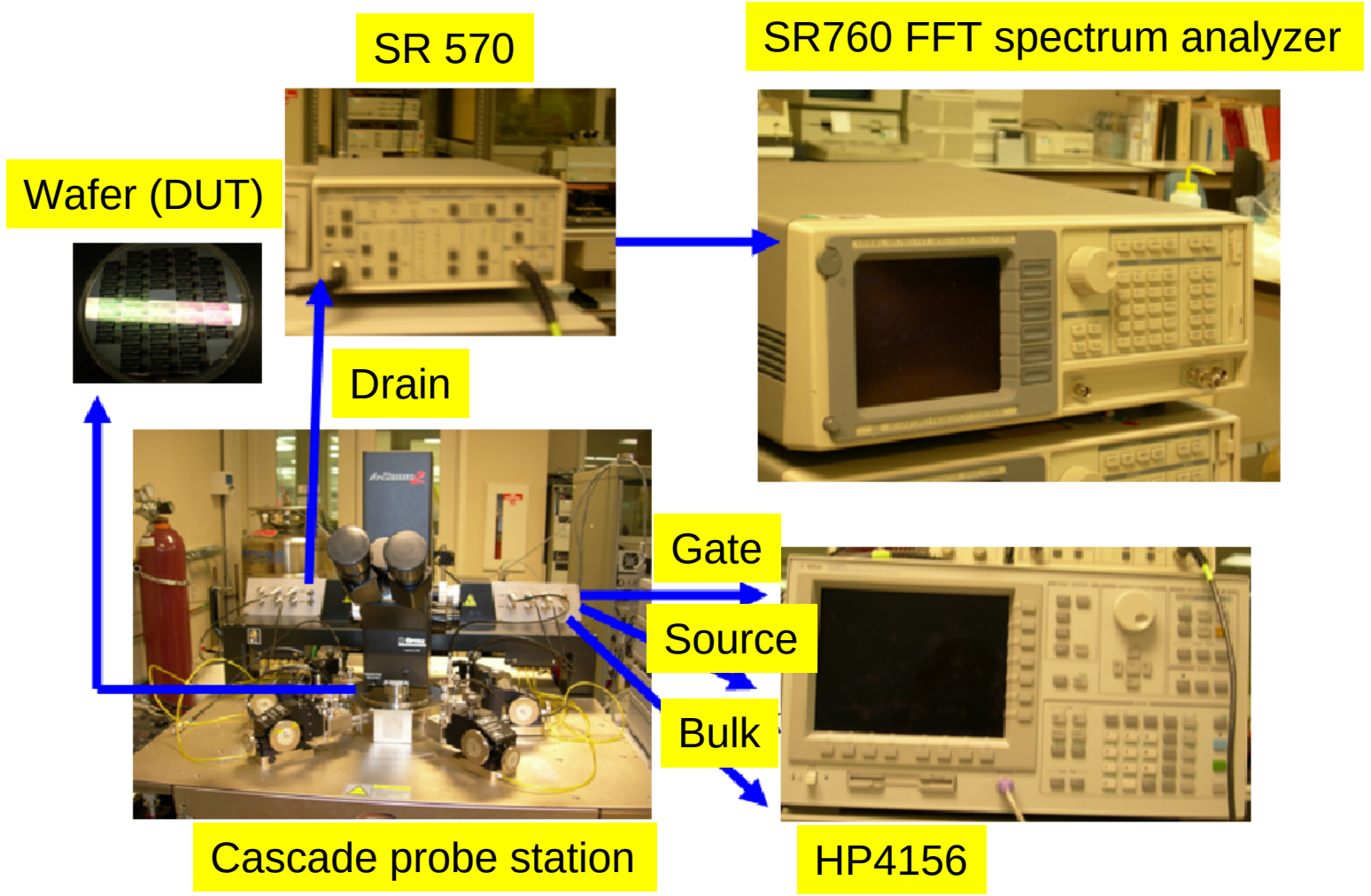



A. Blaum, Agilent document, 2000.

  - Offset current removes the DC component at the input.
  - SR570 is used to drive high impedance loads and input impedance of signal analyzer should be high.

# Noise characterization

- **Measurement bench**

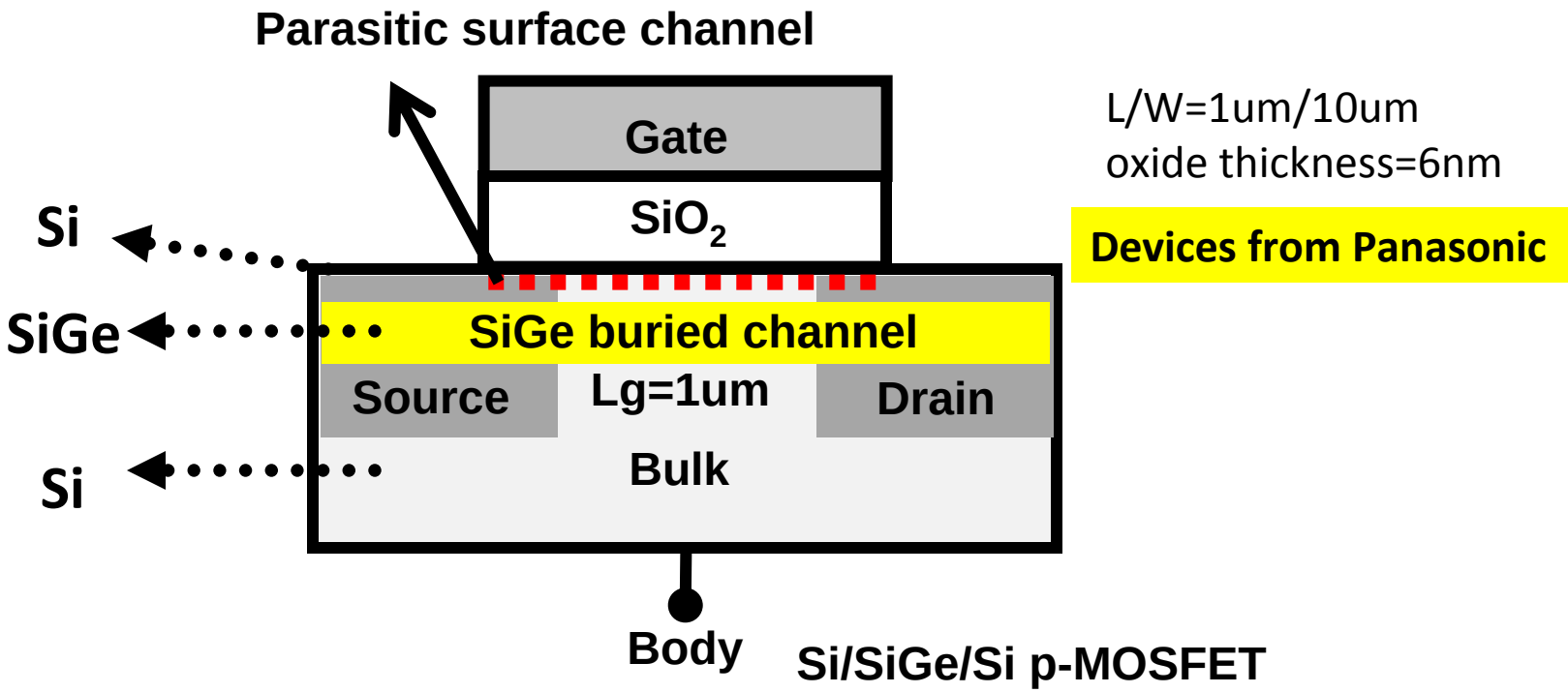


# Outline

- Introduction
- Methodology
- **SiGe channel**
  - Device schematic
  - Gate bias
  - Body bias
- Size effect
- Conclusions

# Device schematic

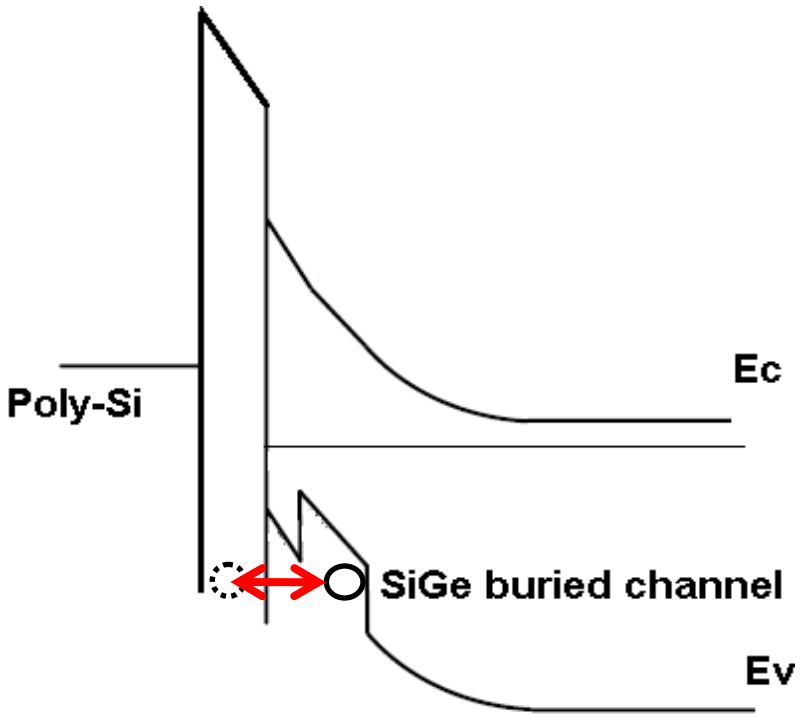
- **Si/SiGe/Si p-HFET**

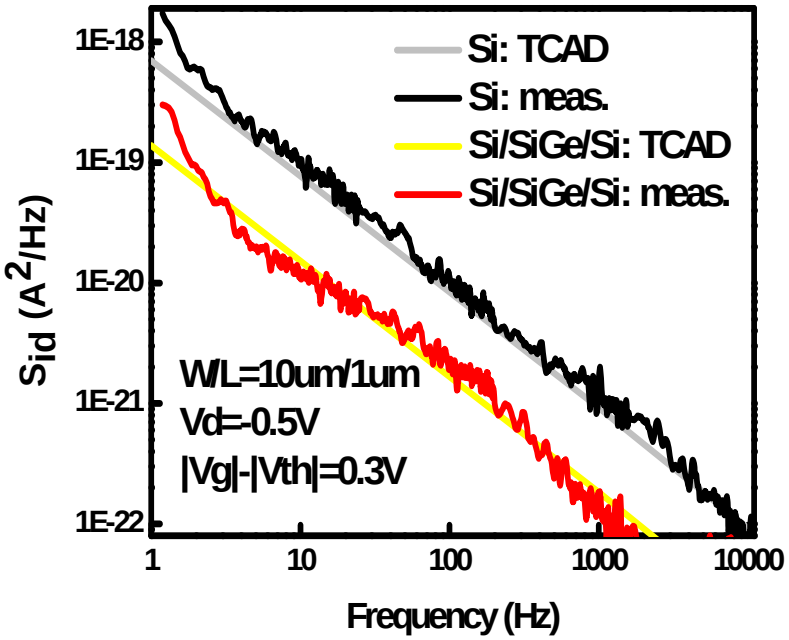



– Two channels: SiGe buried channel and parasitic surface channel.

# Device schematic

- **Advantage**




– Improve LF noise: (1) longer tunneling distance and (2) smaller Coulomb interaction.

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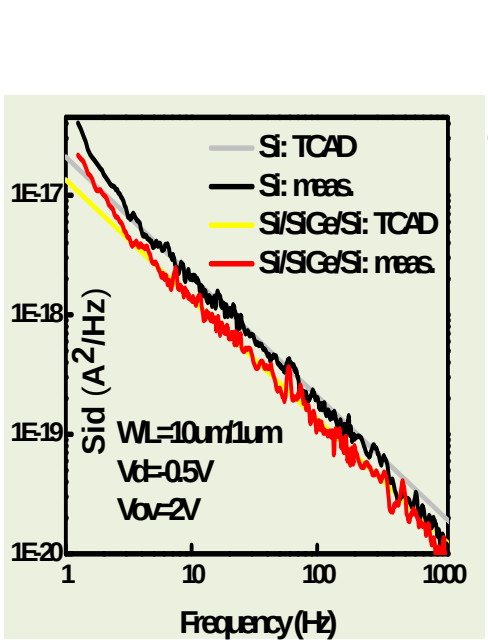
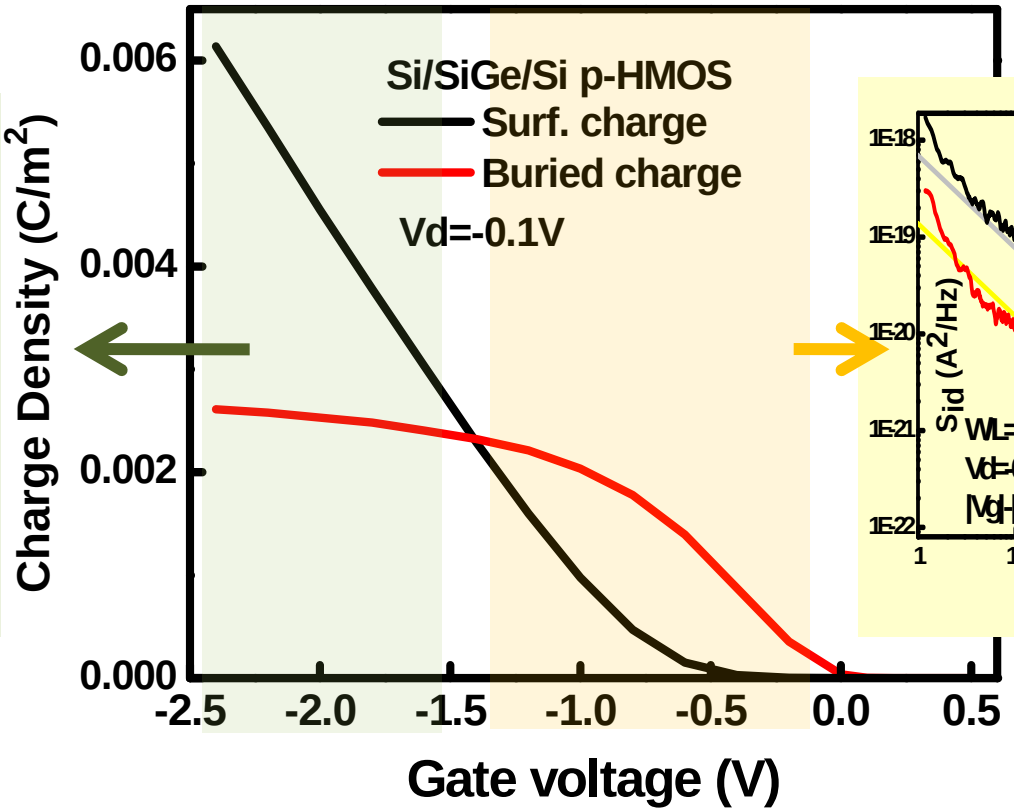
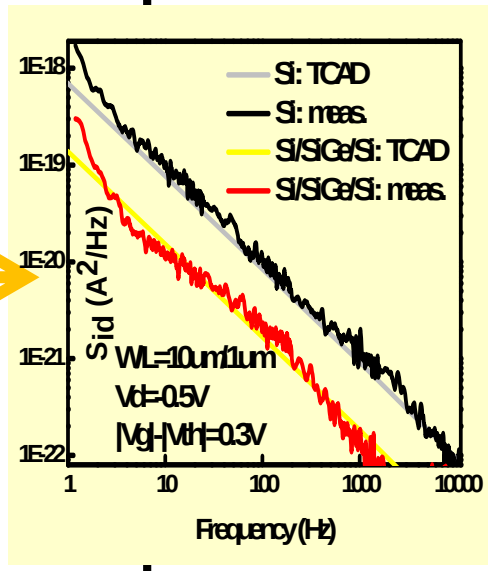
# Gate bias

- **Dual-channel behavior**



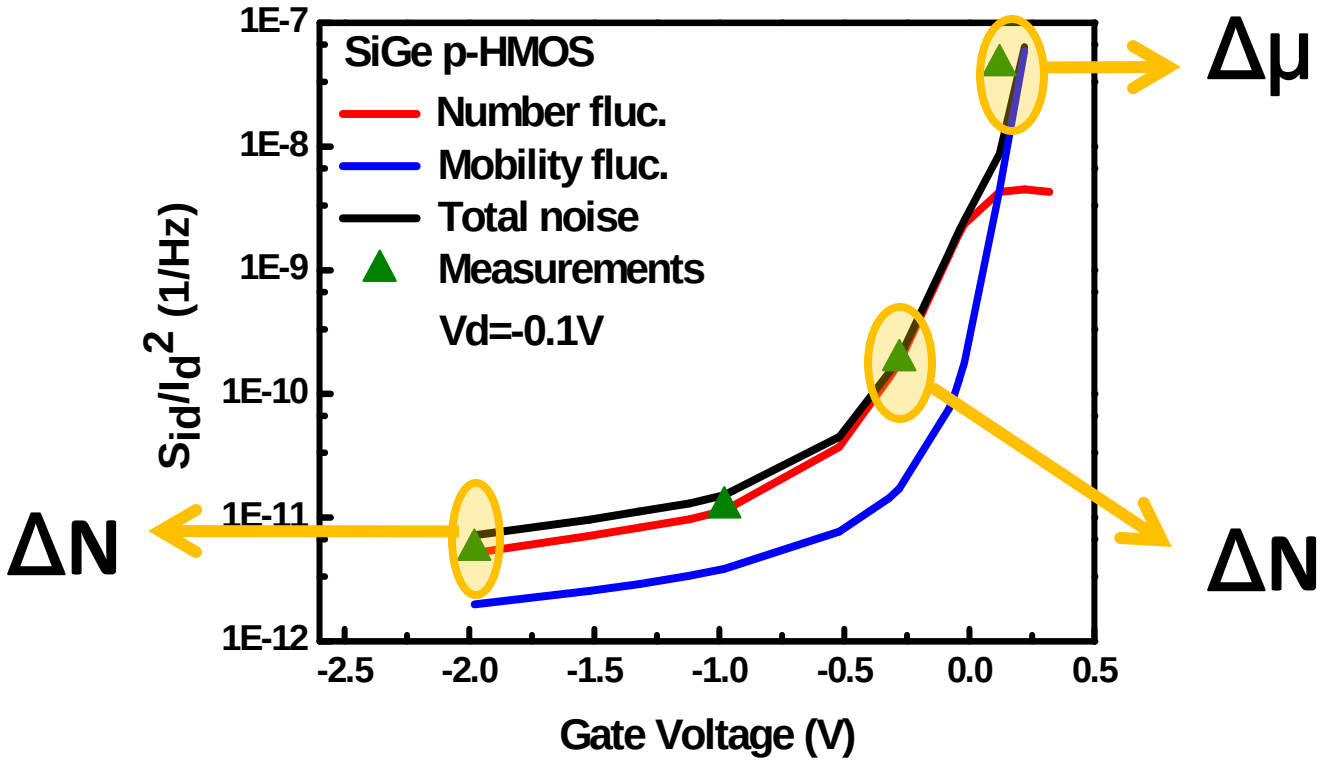




  - When buried channel dominant LF noise is reduced.

# Gate bias

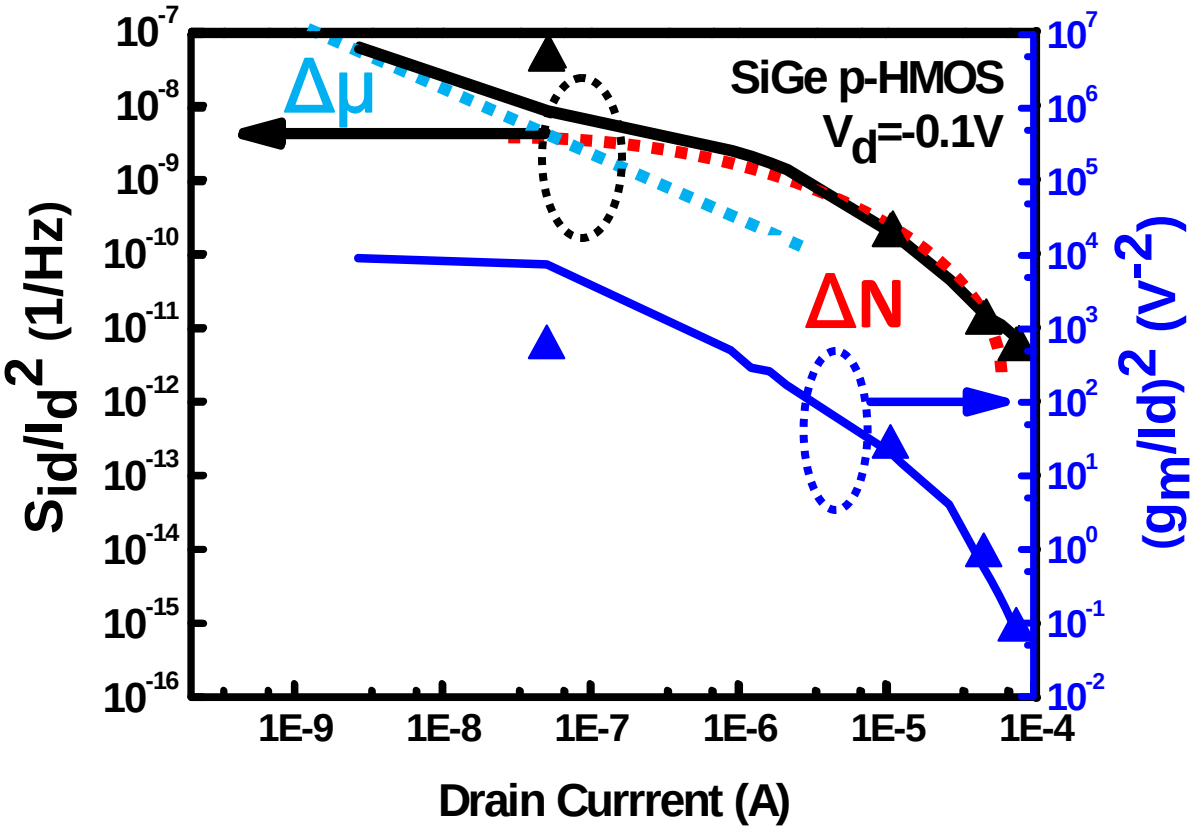
- $V_g$ dependence




  - Weak inversion: Δμ
  - Medium/strong inversion: ΔN

# Gate bias

- $I_d$ dependence




  - Weak inversion: Δμ
  - Medium/strong inversion: ΔN

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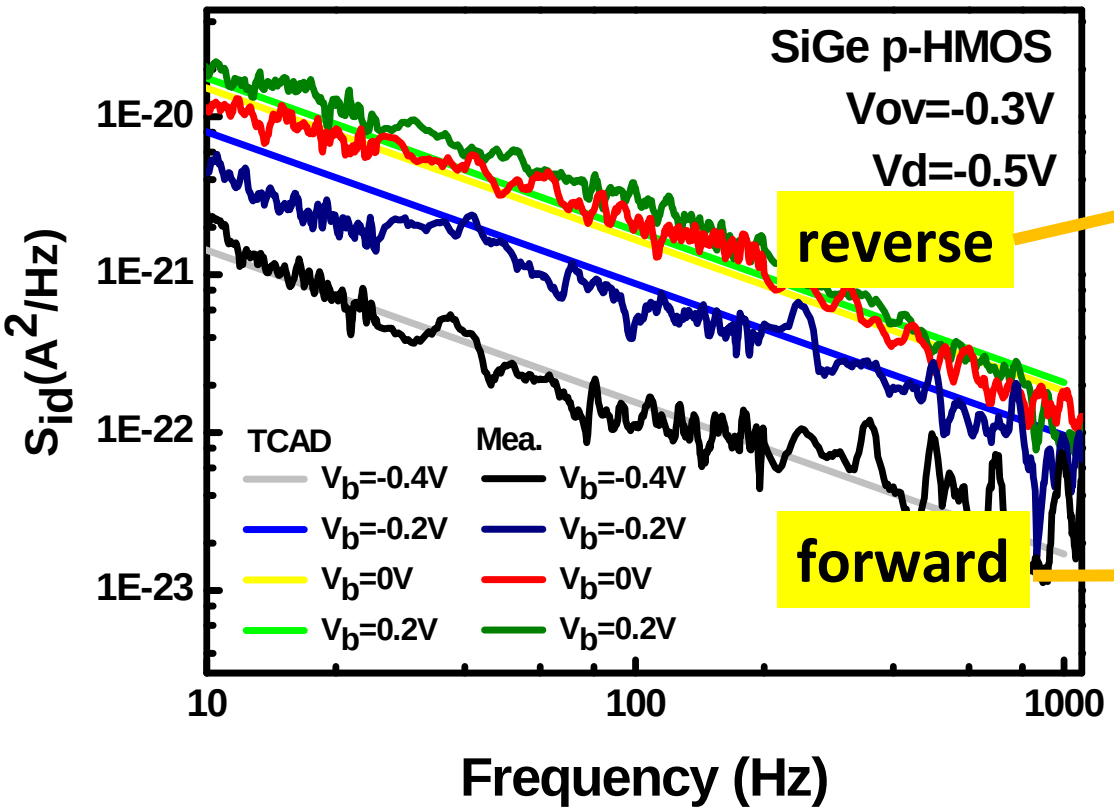
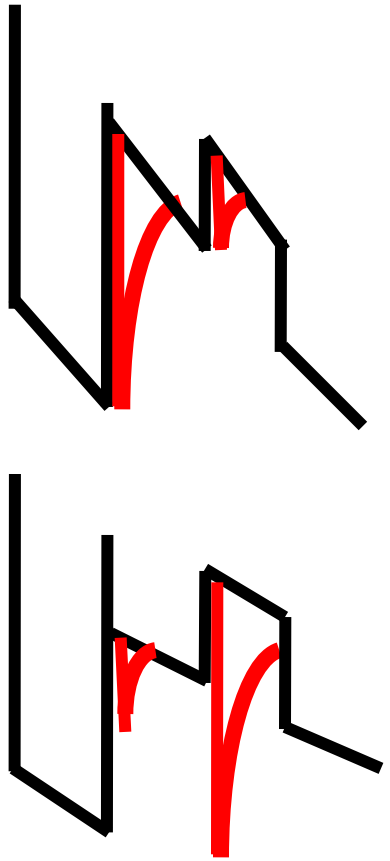
# Body bias

- **SiGe p-HFET**



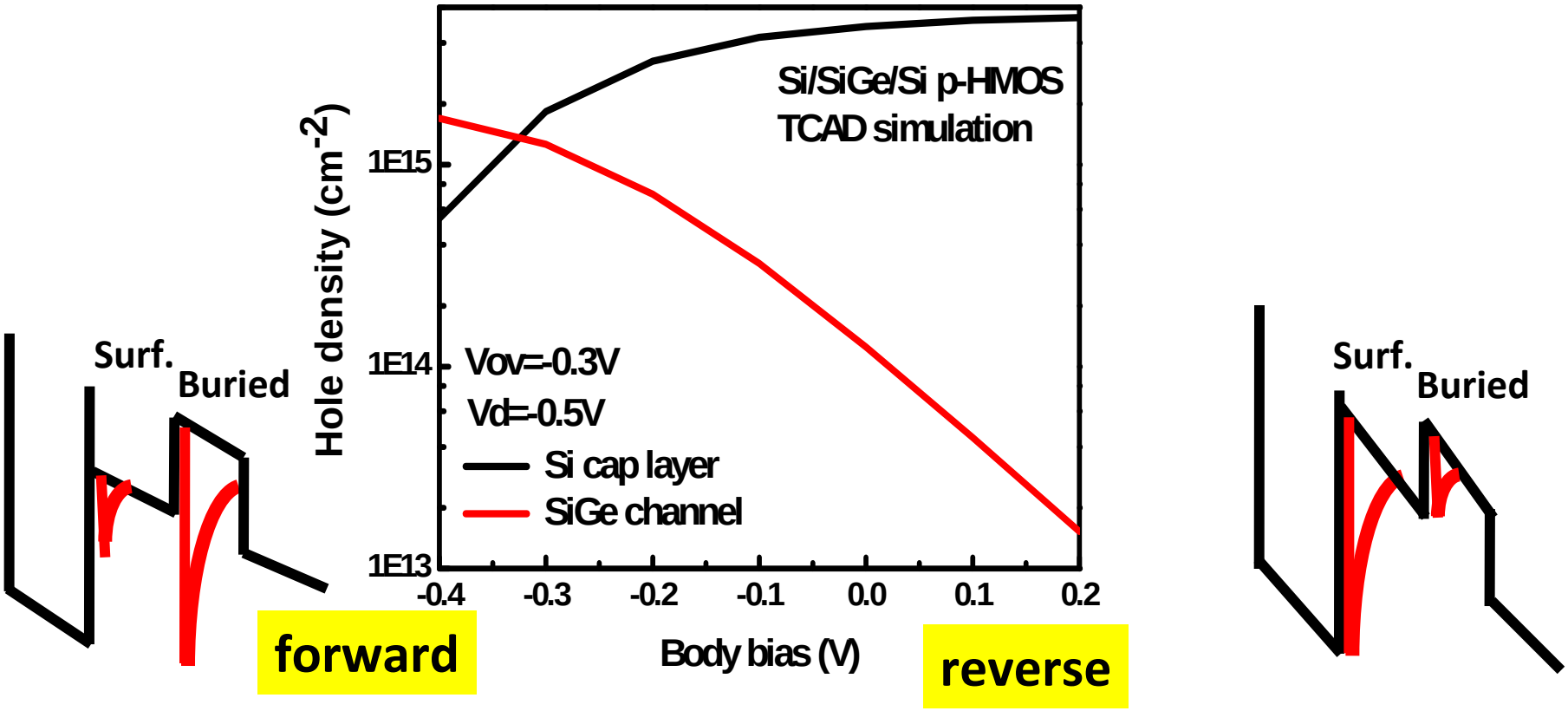




SISPAD 2007, C.-Y. Chen

- LF noise in SiGe p-HFET has strong body bias dependence.

# Body bias

- **SiGe p-HFET**

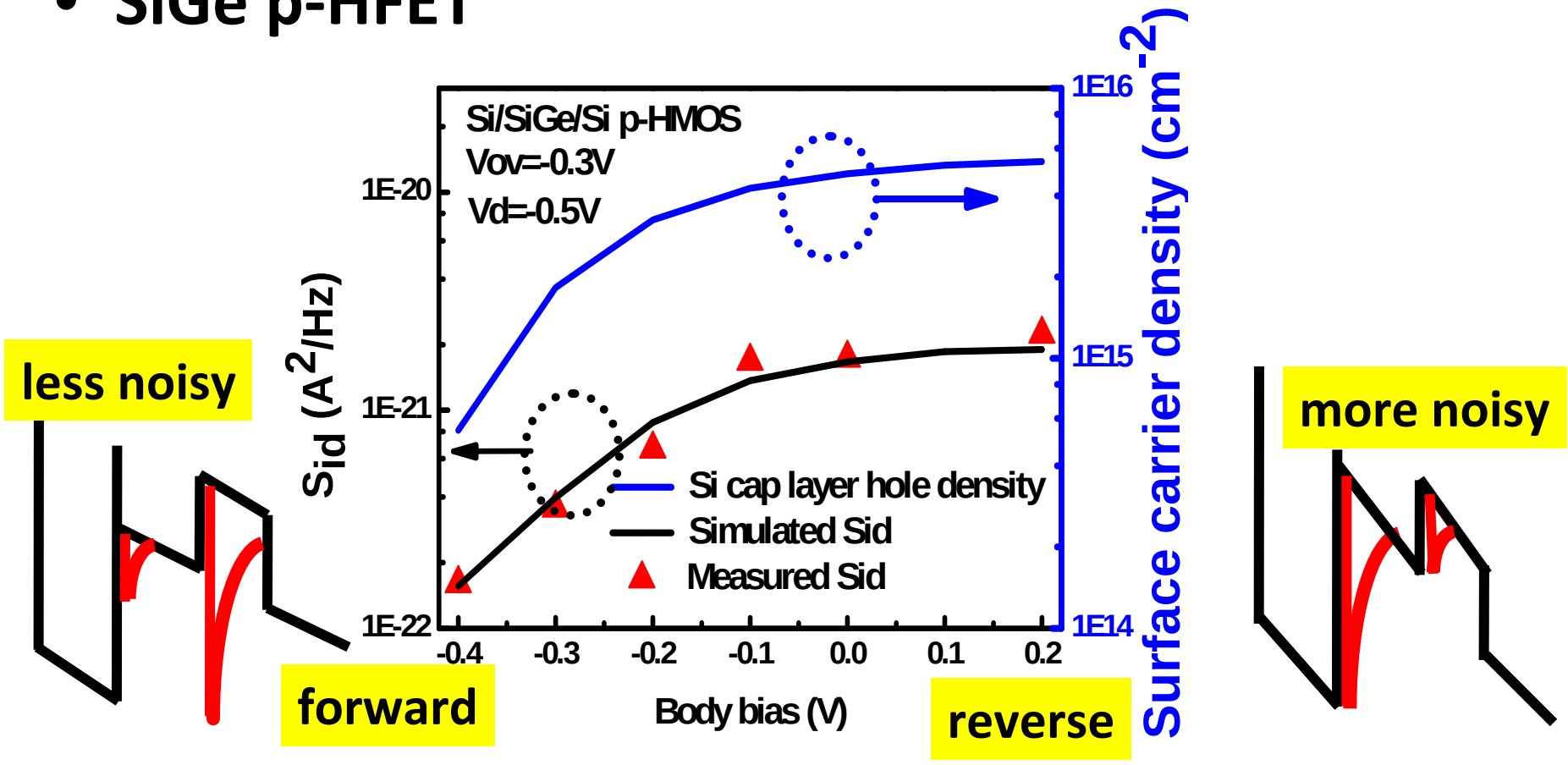



  - Body bias changes carrier distribution in dual channels

T-ED 2008, C.-Y. Chen

# Body bias

- SiGe p-HFET

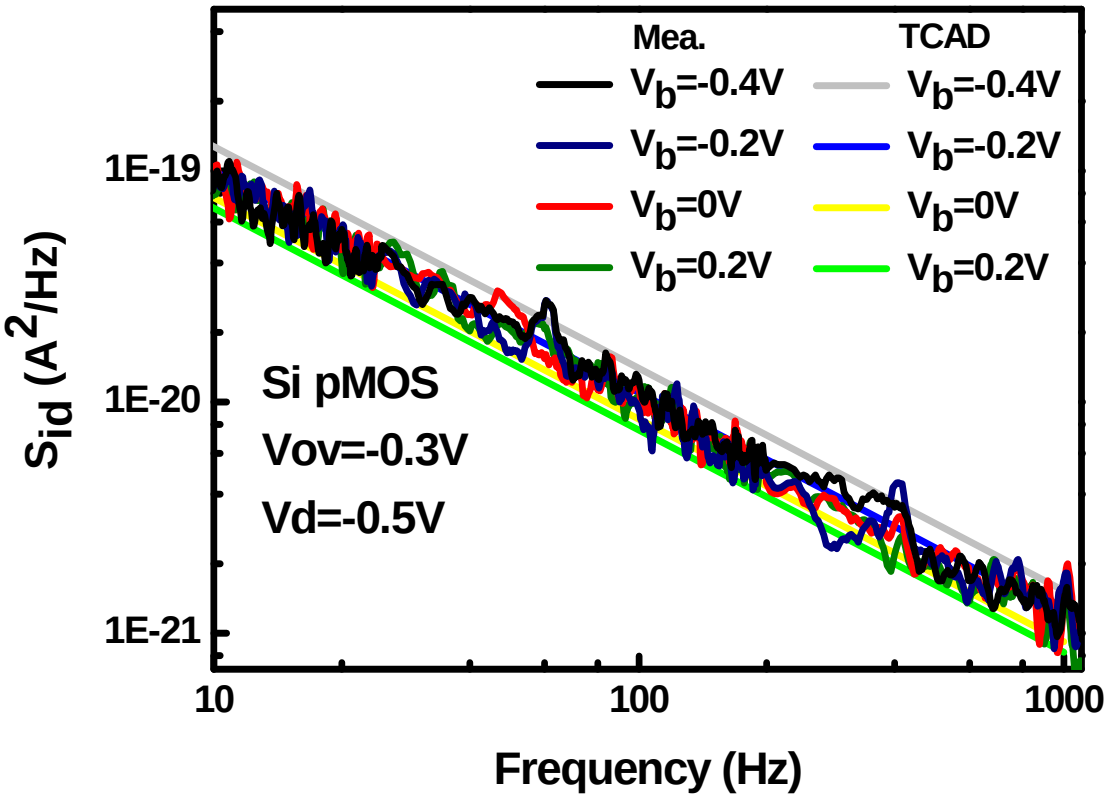


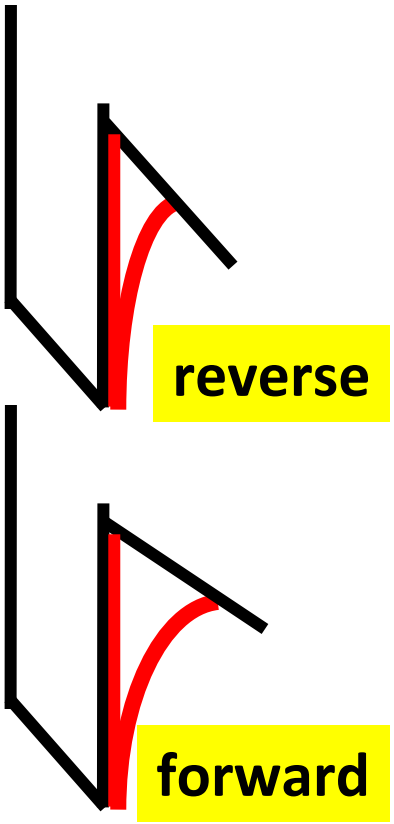

  - FL noise is mainly from surface channel.

T-ED 2008, C.-Y. Chen

# Body bias

- **Si p-FET**




SISPAD 2007, C.-Y. Chen

  - Si p-MOS does not show body bias dependence.

# Outline

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- Methodology
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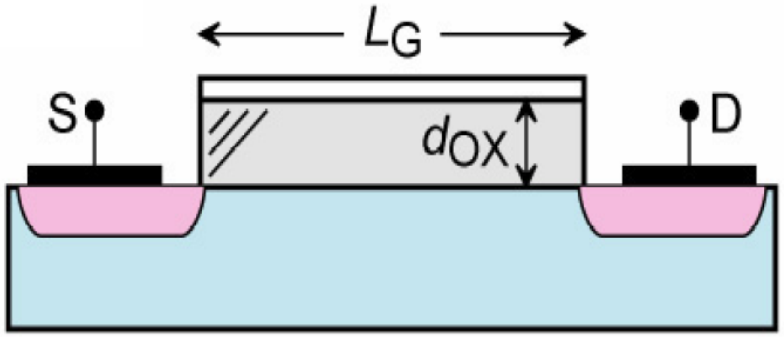
- **Size effect**
  - Device schematic
  - Mechanism
  - Gate bias
- Conclusions

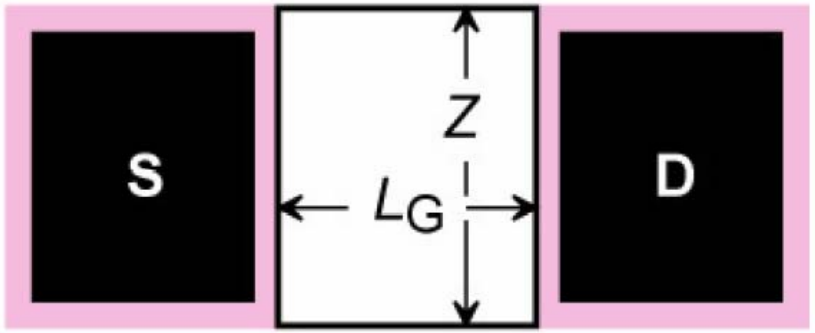
# Device schematic

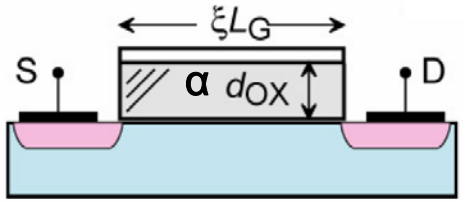
- **Scaled MOSFETs (small gate area)**

Cross view



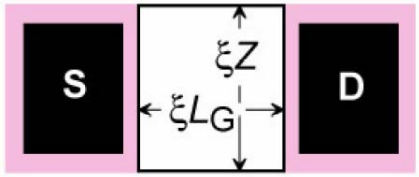

Top view




L/W=40nm/70nm
oxide thickness~2.5nm

**Devices from G-foundries**



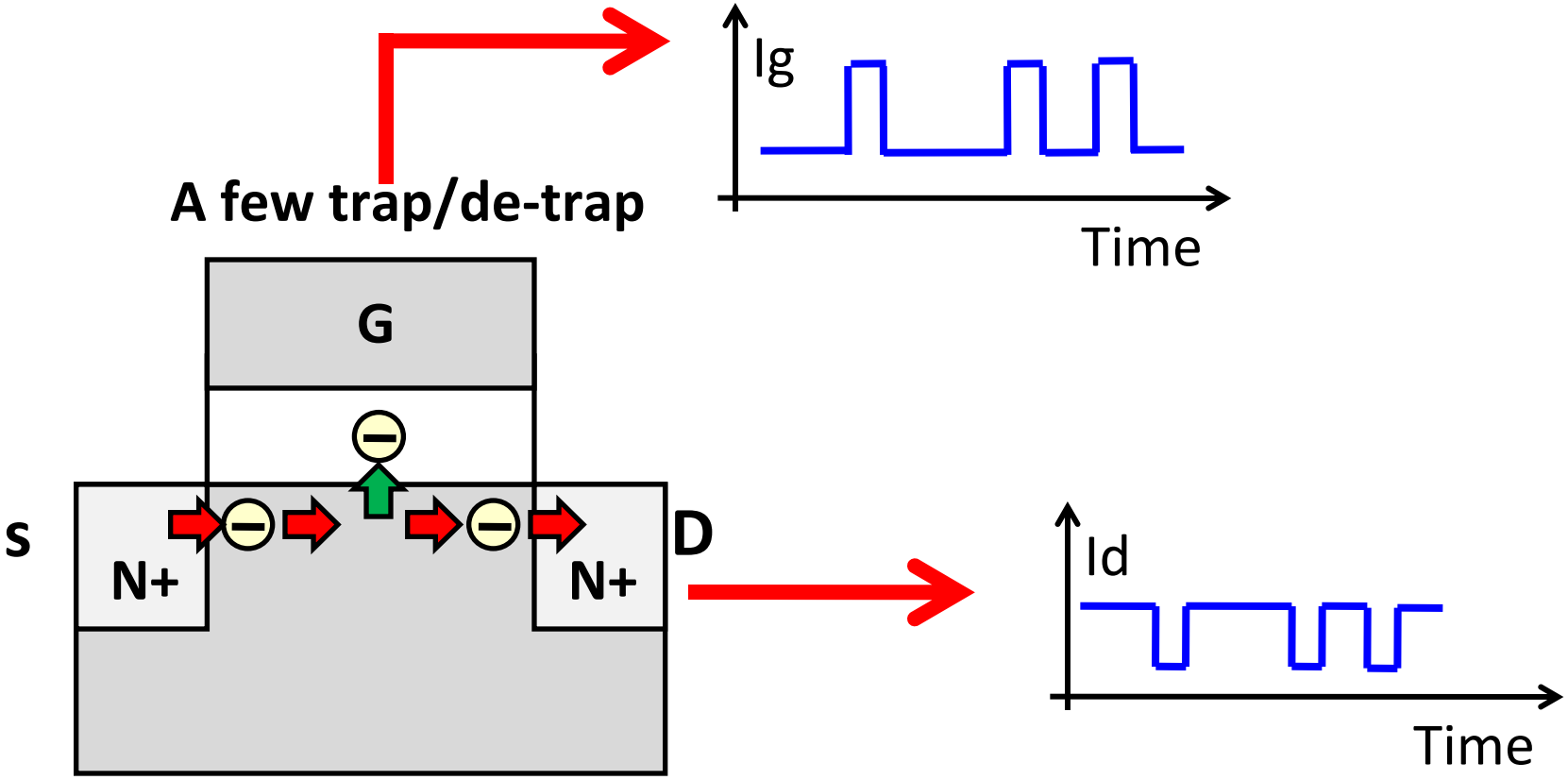

- Only a few traps are involved.
- ΔN predicts RTN; Δμ shows 1/f noise.

# Outline

- Introduction
- Methodology
- SiGe channel
- **Size effect**
  - Device schematic
  - Mechanism
  - Gate bias
- Conclusions

# Mechanism

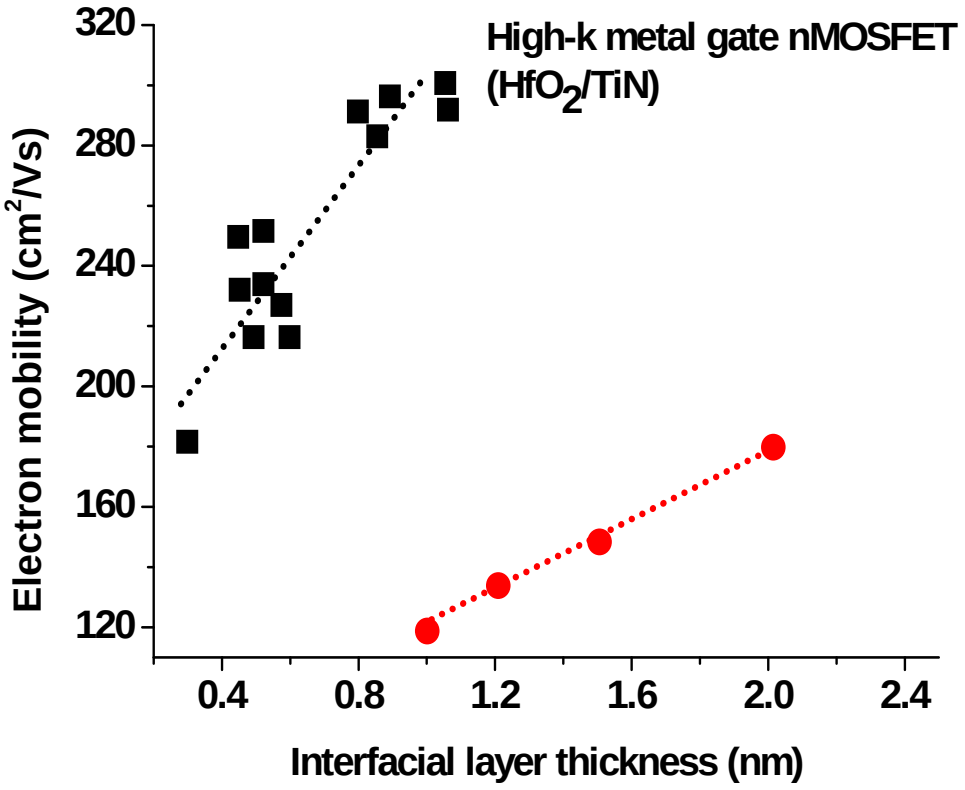
- **Ig- / Id-RTN**

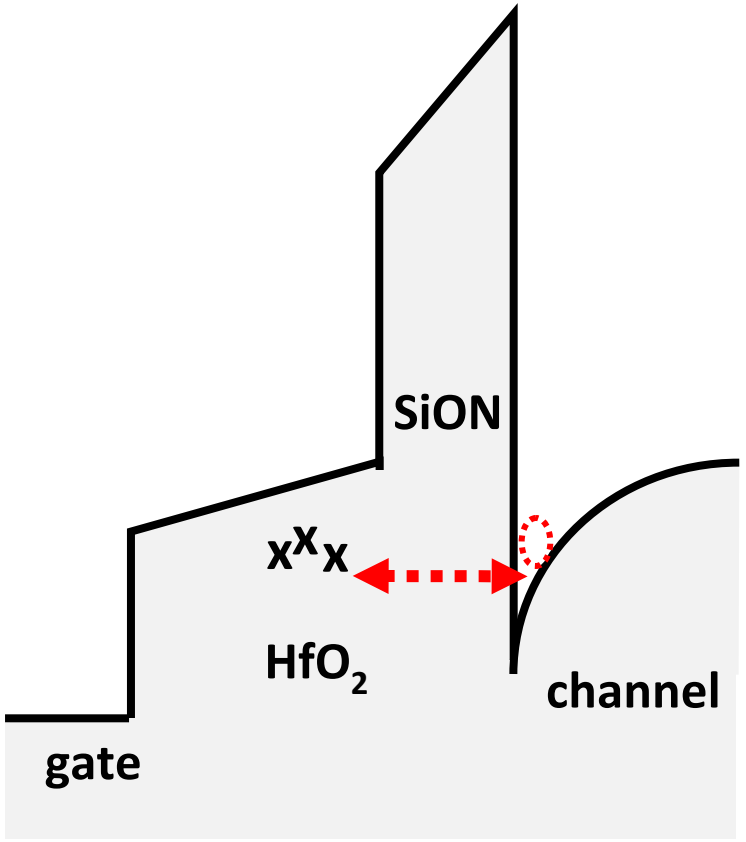



  - Two types: Ig-RTN and Id-RTN.

# Mechanism

- **Where are traps?**

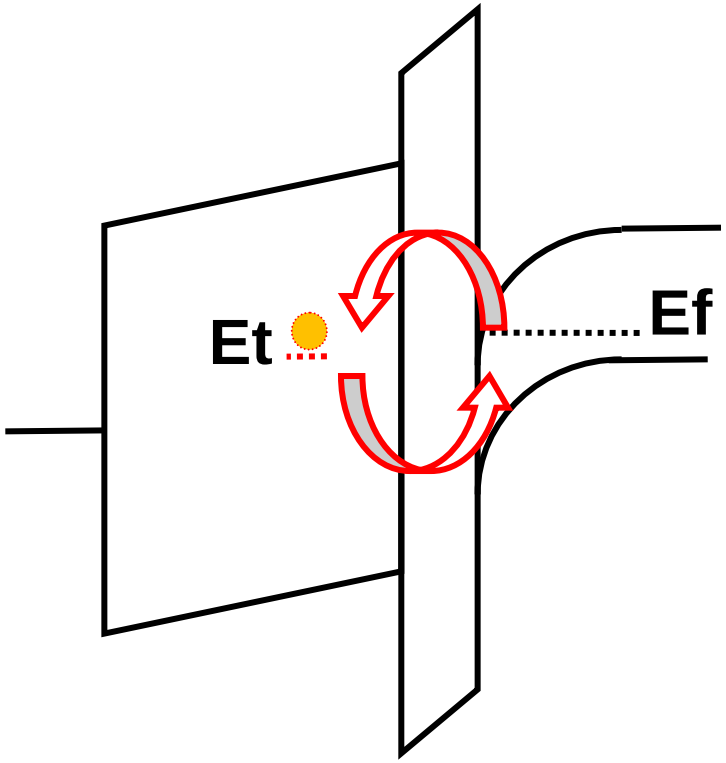


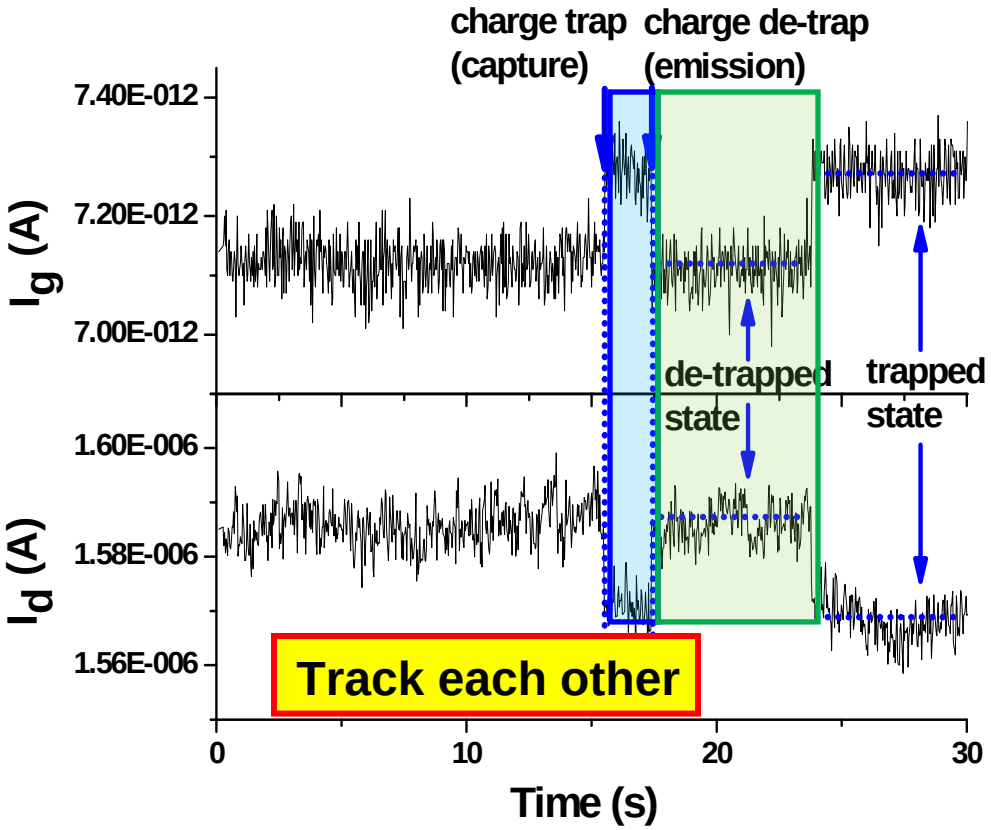




– Traps should be inside high-κ oxide.

# Mechanism

- **Trap/de-trap**

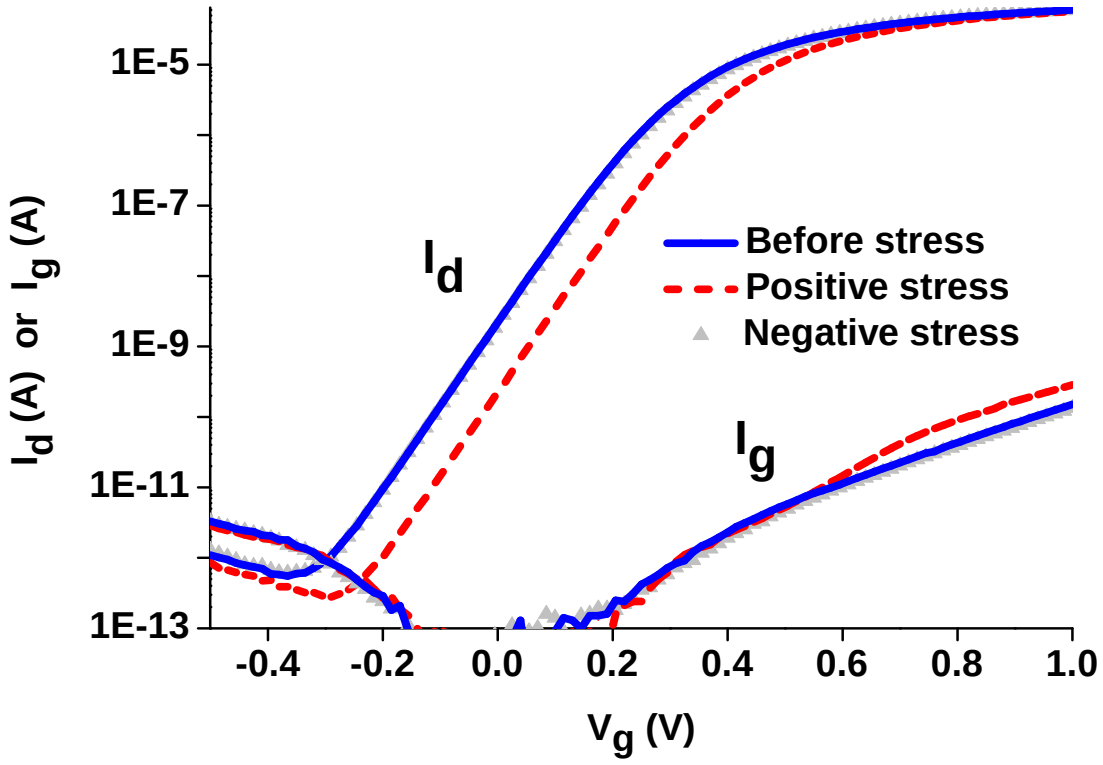



- Capture: $V_{th}$ and TAT increase → $I_d$↓ and $I_g$↑
- Emission: $V_{th}$ and TAT decrease → $I_d$↑ and $I_g$↓

# Mechanism

- **PBTI and RTN**



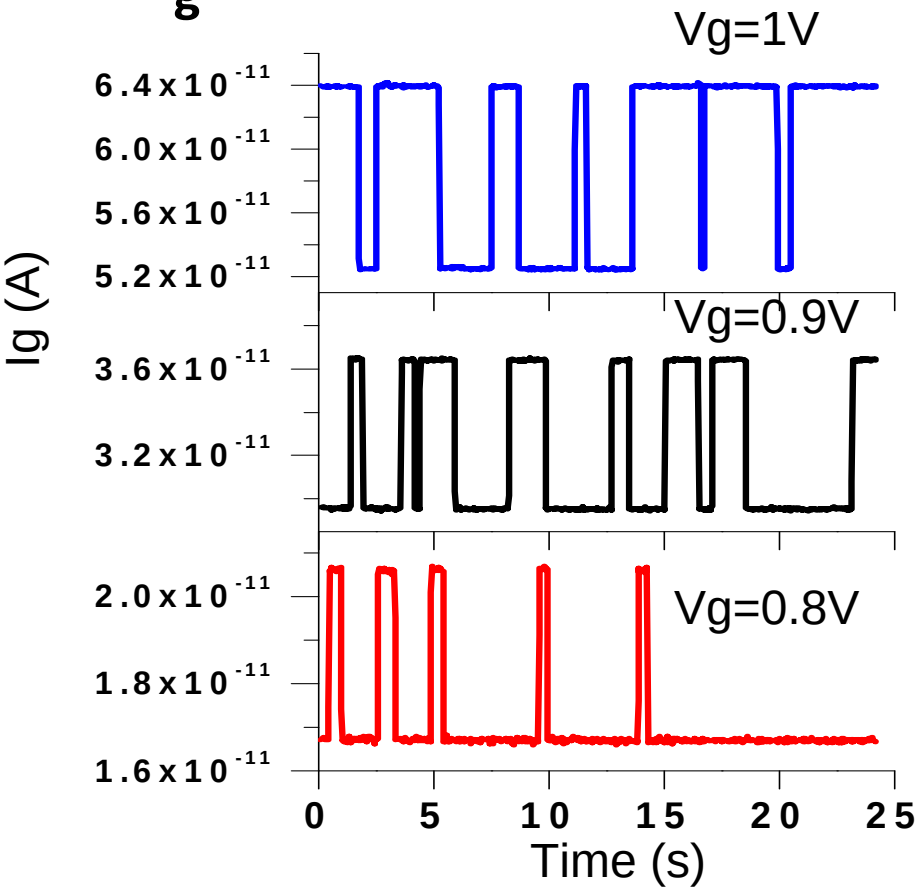

– Consistent with RTN results.

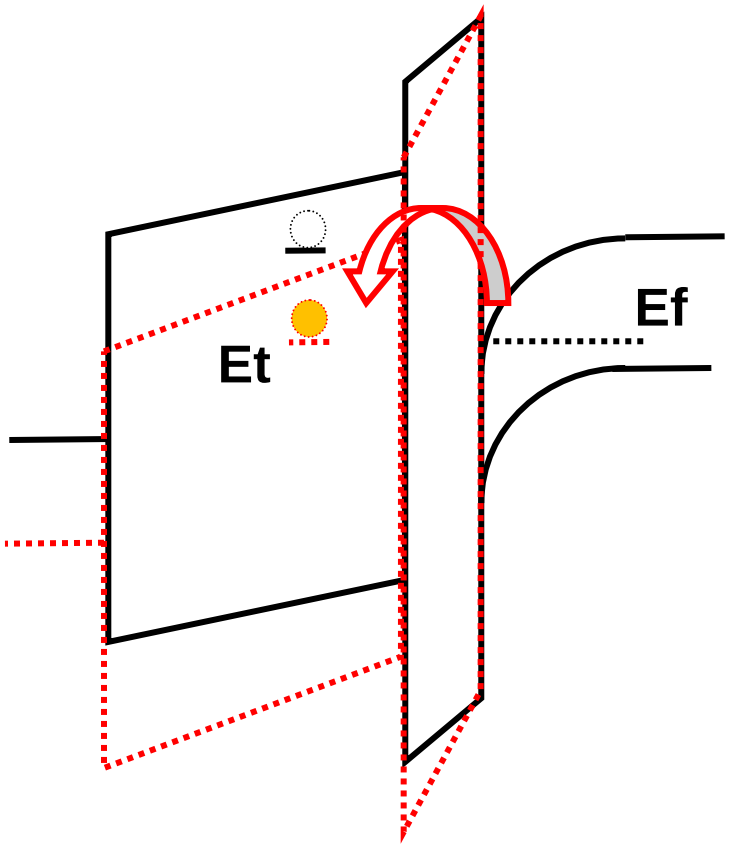
# Outline

- Introduction
- Methodology
- SiGe channel
- **Size effect**
  - Device schematic
  - Mechanism
  - Gate bias
- Conclusions

# Gate bias

- $I_g$-RTN

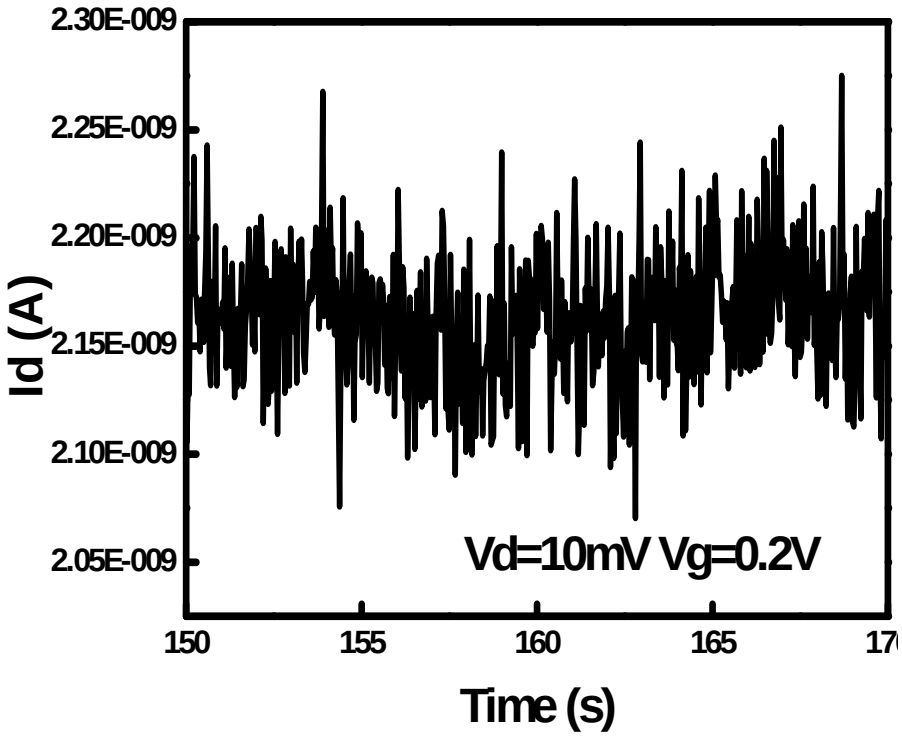


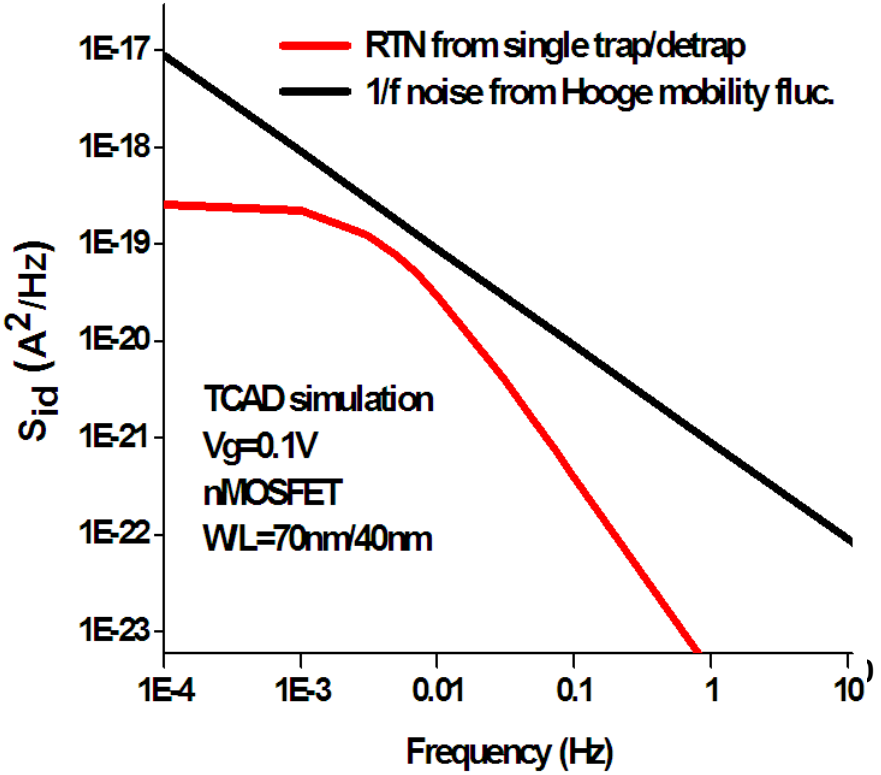




  - $V_g$ increases: Time in high-$I_g$ state increases.

# Gate bias

- $I_d$-RTN: Low Vg

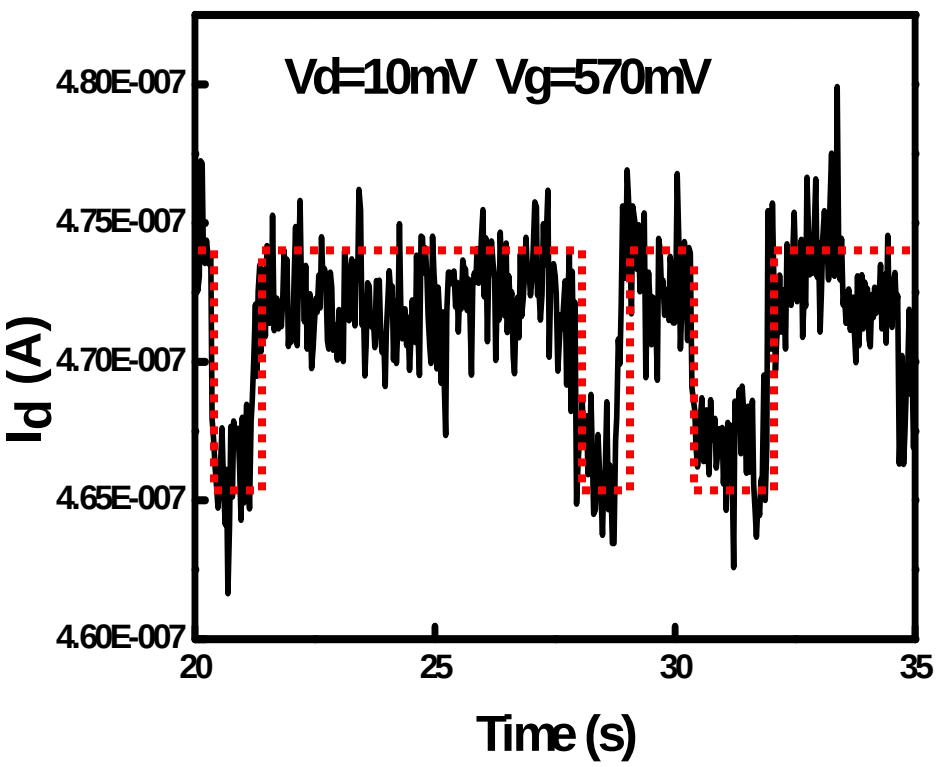


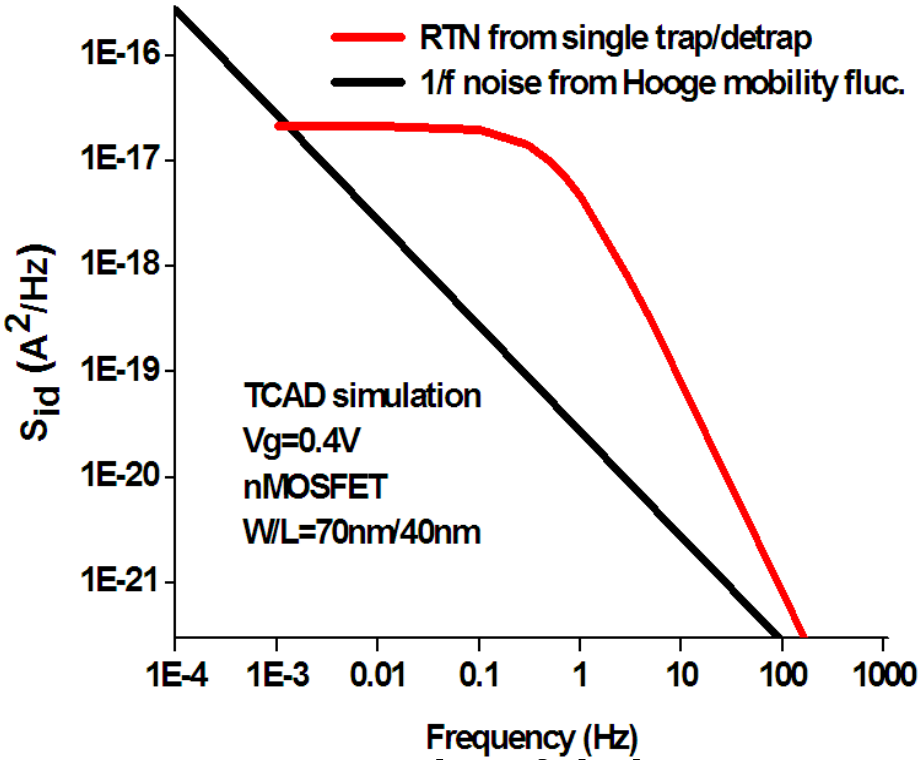




  - Measurement still shows 1/f noise; Δμ model is dominant.

# Gate bias

- $I_d$-RTN: High gm bias condition

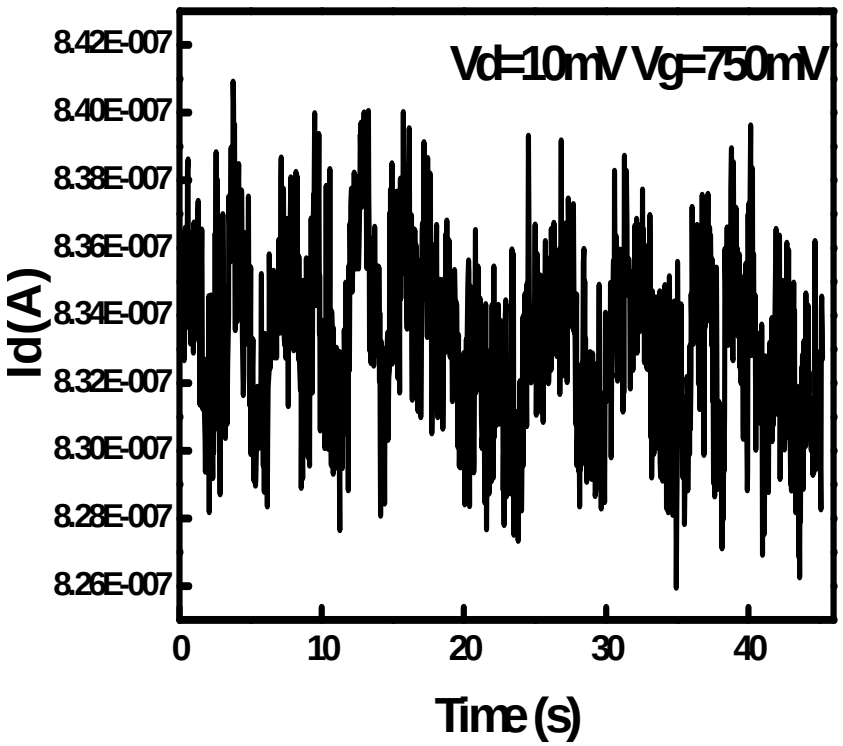


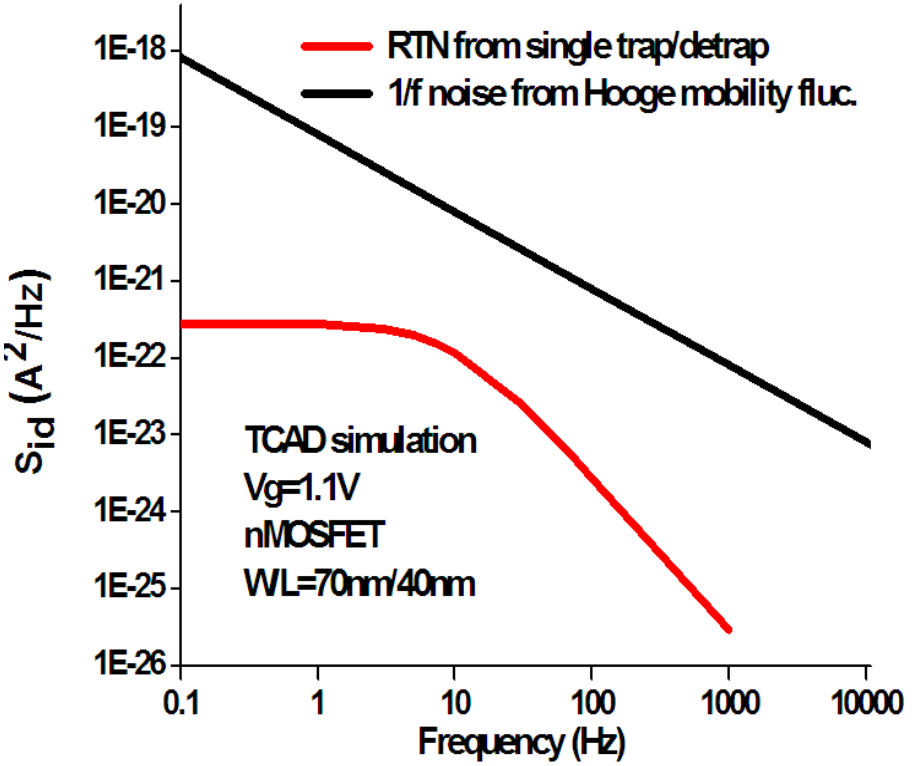




  - RTN and Lorentzian shape are observed in high gm region.

# Gate bias

- $I_d$-RTN: High Vg

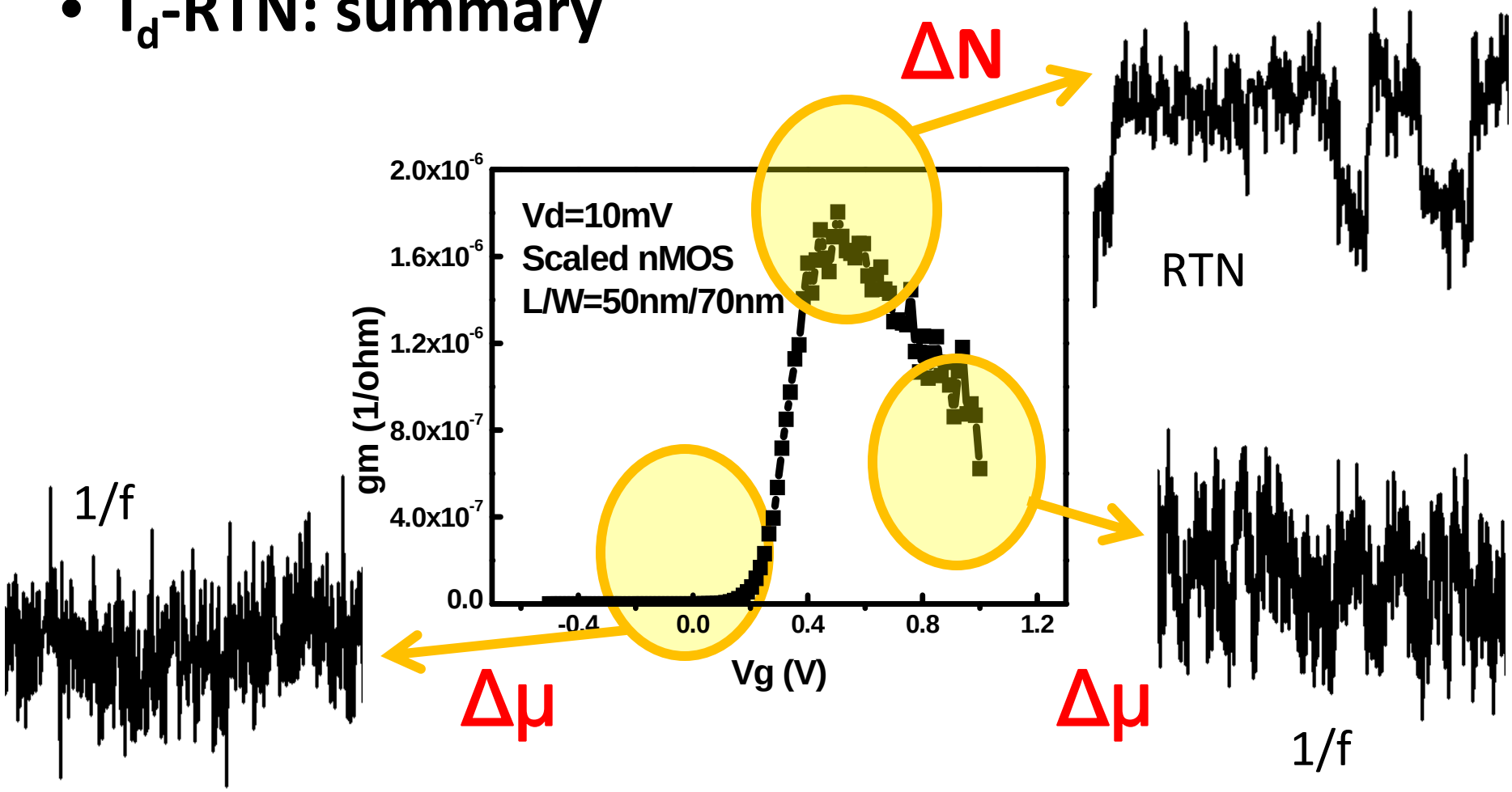



  - 1/f noise is shown in a very scaled MOSFET: Δμ is dominant.

# Gate bias

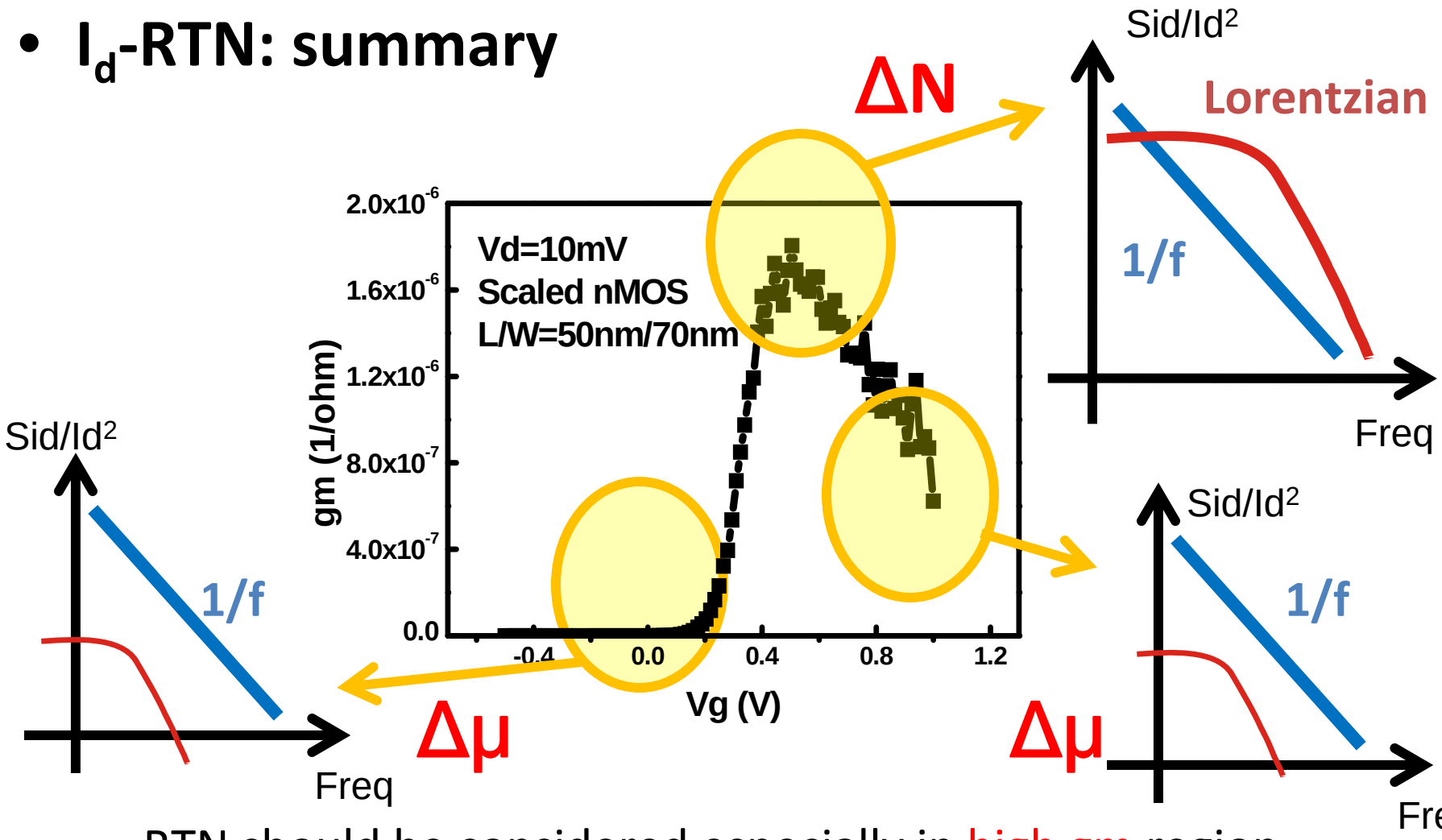
- $I_d$-RTN: summary




– RTN should be considered especially in high gm region.

# Gate bias

- $I_d$-RTN: summary




– RTN should be considered especially in high gm region.

# Outline

- Introduction
- The origin of LF noise
- Methodology
- SiGe channel
- Size effect
- **Conclusions**
  - Summary
  - Contributions
  - Future work

# Summary

| Bias | SiGe H-MOS (Lg~1um) | Scaled MOS (Lg~40nm) |
|---|---|---|
| Weak inversion | Δμ model is dominant. | Δμ model is dominant. |
| High gm region (~ $V_{dd}/2$) | ΔN model is important; LF noise is mostly surface effect. | ΔN model becomes important; RTN should be considered. |
| High $V_g$ condition | ΔN is dominant in our device, but in general it can be technology dependence. | Δμ model is dominant |

# Summary

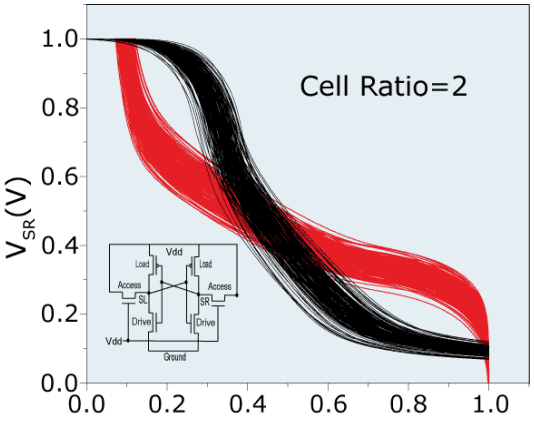
- **The origin of LF noise:** (1) ΔN model and (2) Δμ model.
- **Methodology:** TCAD simulations and noise measurements
- **SiGe channel:** Dual-channel is important to explain the low frequency noise performance.
- **Size effect:** $I_g$-RTN is directly related to physical trapping or de-trapping and the $I_d$-RTN reflects sensitivity to charge trapping as determined by $g_m$.
- **CMOS scaling:** provides a new opportunity for LF noise study.

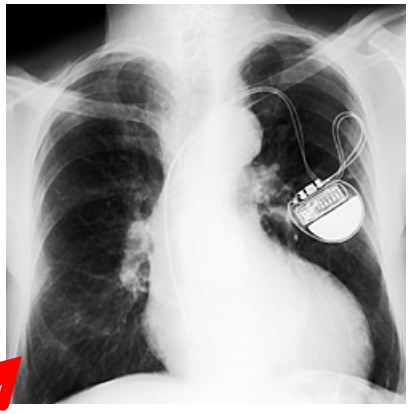
# Contributions

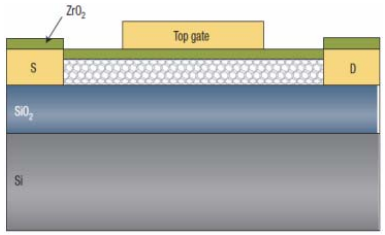
- Detailed LF noise mechanisms in SiGe p-HFET are proposed.
- LF noise mechanisms in scaled MOSFETs are measured and analyzed.

- Other parts: (1) LF noise mechanisms in high-κ MOSFET, (2) A LF noise compact model in SiGe p-HFET, (3) linearity of asymmetric channel doping for LDMOS, (4) linearity in GaN HEMTs, and (5) asymmetric FET scaling.

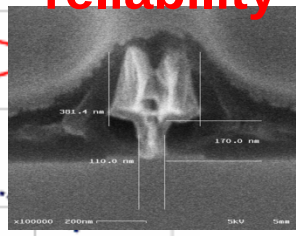
# Future work



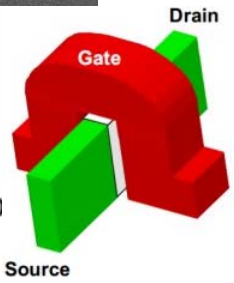






**Rethink "device noise" "distortion" and "reliability"**



# Publications


[1] **C.-Y. Chen**, Q. Ran, H.-J. Cho, A. Kerber, Y. Liu, M.-R. Lin, and R. W. Dutton, *IRPS, 2011.*

[2] **C.-Y. Chen**, C.-C. Wang, Y. Ye, Y. Liu, Y. Cao, and R. W. Dutton, *SASIMI, 2010.*

[3] **C.-Y. Chen**, O. Tornblad, R. W. Dutton, *IEEE Trans. on Microwave Theory and Techniques*, Dec. 2009.

[4] **C.-Y. Chen** and R. W. Dutton, *IEEE Design & Test of Computers*, 2009.

[5] **C.-Y. Chen**, Y. Liu, J. Kim, R. W. Dutton, *SISPAD* 2009, Sept. 2009.

[6] **C.-Y. Chen**, O. Tornblad, R. W. Dutton, *IEEE MTT-S International Microwave Symposium Dig. (IMS),* pp. 601-604, 2009.

[7] **C.-Y. Chen**, Y. Liu, R. W. Dutton, J. Sato-Iwanaga, A. Inoue, H. Sorada, *SASIMI* 2009, Sapporo, Japan, pp. 405-409, March 2009.

[8] **C.-Y. Chen**, Y. Liu, R. W. Dutton, J. Sato-Iwanaga, A. Inoue, H. Sorada, *IEEE Trans. Electron Devices*, July, 2008.

[9] J. Kim, **C.-Y. Chen** and R. W. Dutton, Journal of Computational Electronics, Jan. 2008.

[10] **C.-Y. Chen**, Y. Liu, R. W. Dutton, J. Sato-Iwanaga, A. Inoue, H. Sorada, *SASIMI*, Sapporo, Japan, pp. 238-241, Oct. 2007.

[11] **C.-Y. Chen**, Y. Liu, R. W. Dutton, J. Sato-Iwanaga, A. Inoue, H. Sorada, *Workshop on Compact Modeling (WCM) 2007*, San Jose, USA, March 2007.

[12] J. Kim, **C.-Y. Chen**, R. W. Dutton, *SISPAD*, Nov. 2007.

[13] J. Kim, **C.-Y. Chen**, R. W. Dutton, *Proc. of 12th International Workshop on Computational Electronics (IWCE)*, Oct. 2007.

# Backup: Linearity analysis of lateral channel doping in RF power MOSFETs

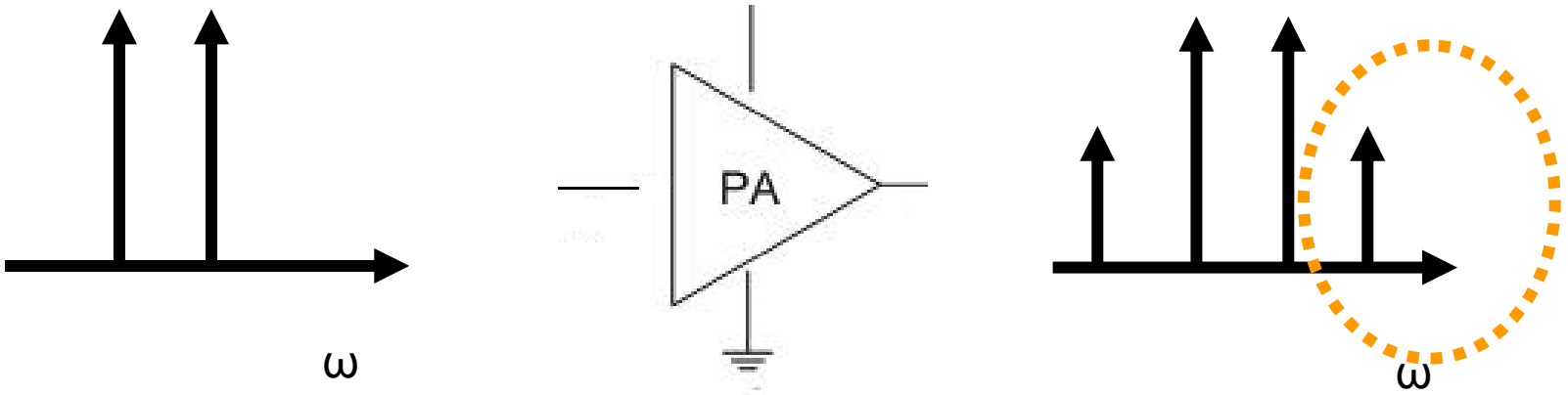
**Chia-Yu Chen**
**Department of Electrical Engineering**
**Stanford University**

# Backup: Outline

- Introduction
- Quasi-1D structure
- Realistic LDMOS structure
- Conclusions

# Backup: Introduction (1 of 2)

**Linearity:**

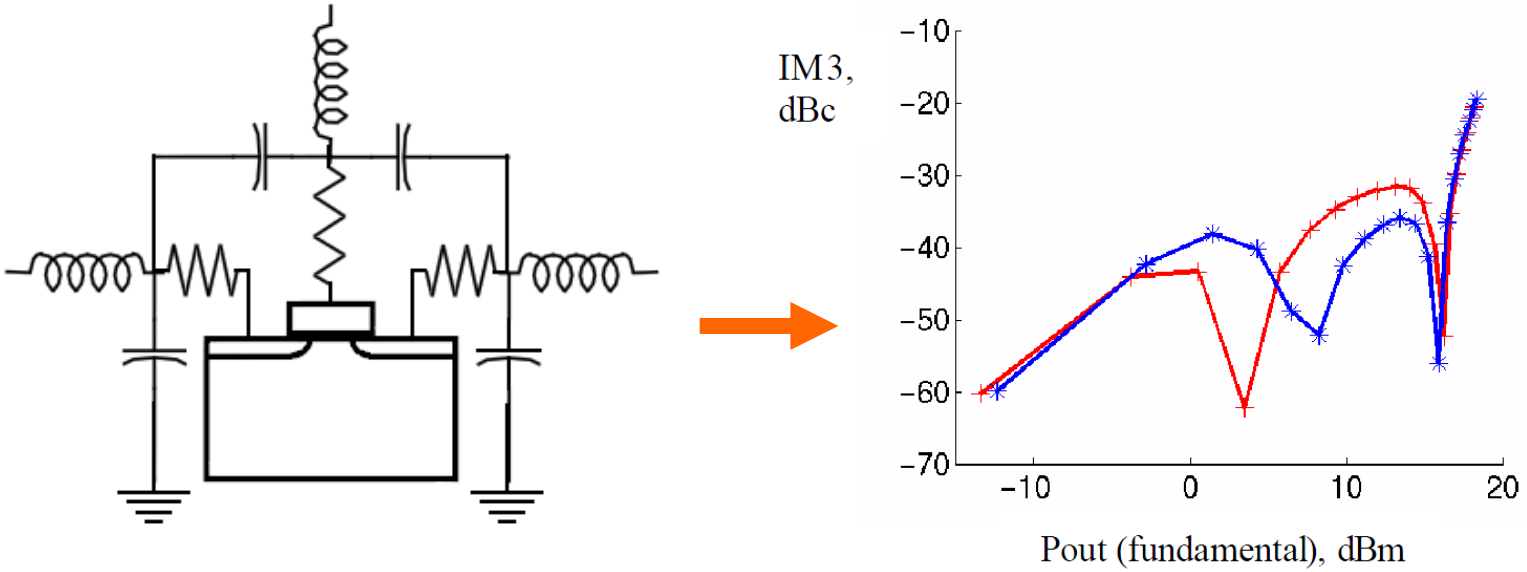



Low distortion is one of the most important concerns for wireless communication systems.

Analysis of the distortion generated by the device itself has been fairly limited.

# Backup: Introduction (2 of 2)

## Harmonic balance device simulations:

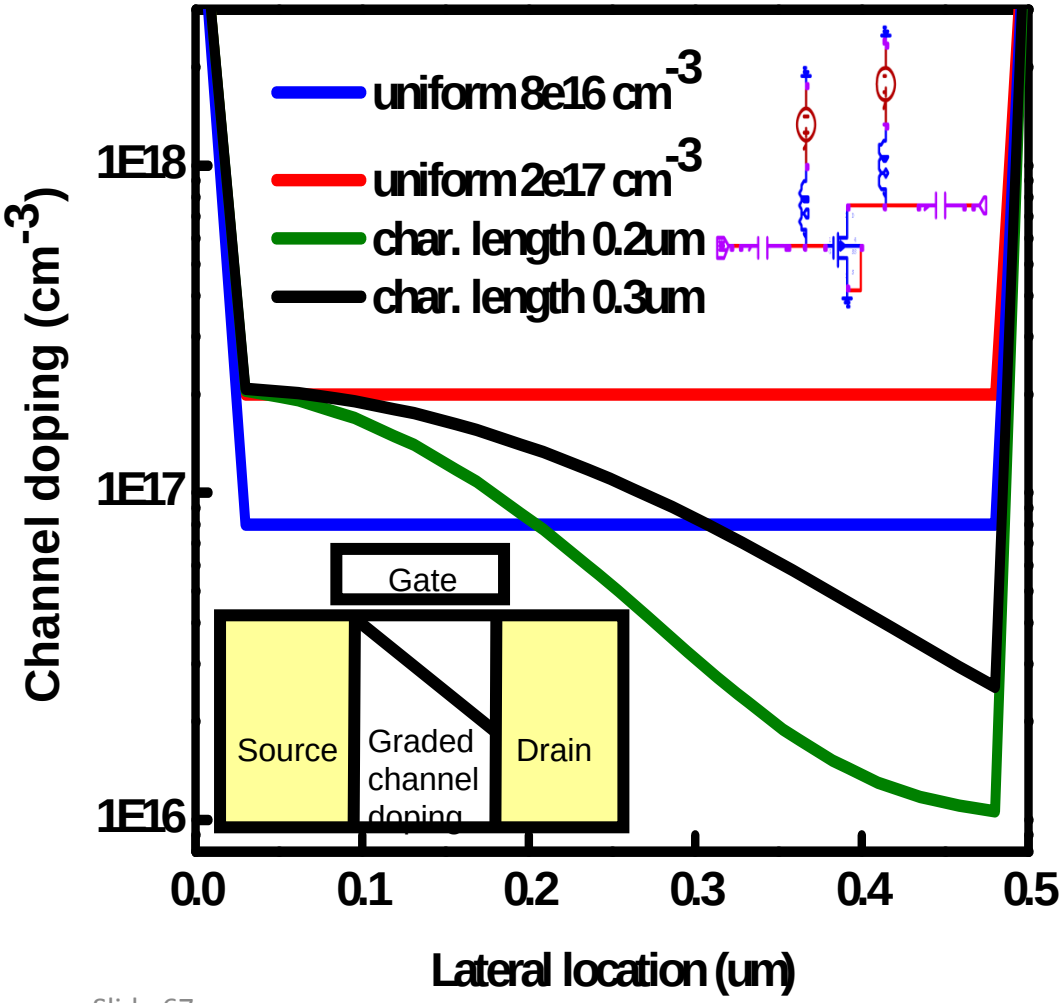



A unique harmonic balance (HB) device simulator with the capability of including external circuitry is used.

In the HB simulations, variations in device parameters are directly reflected in the final large signal RF performance.

# Backup: Quasi-1D structure (1 of 3)

## Device schematic:




0.5um gate length, 30nm oxide thickness.

Avoid 2D-effects.

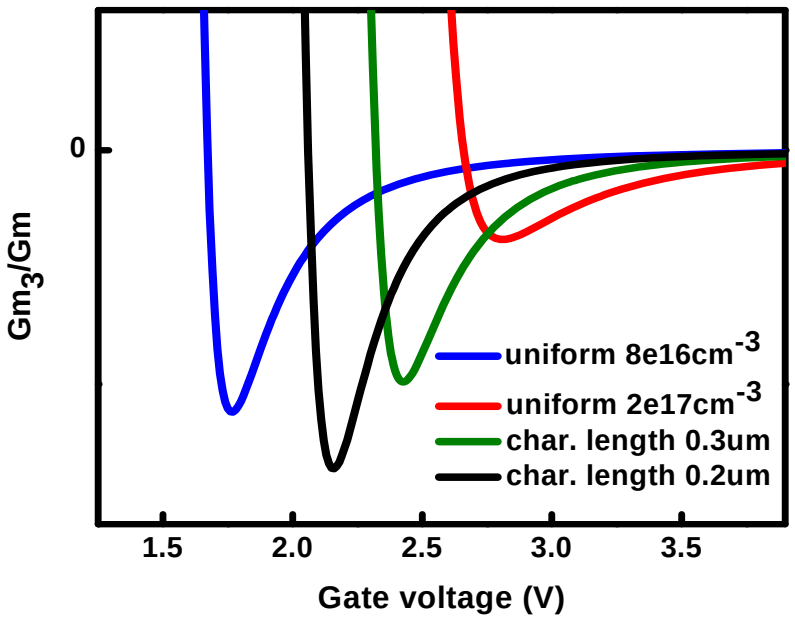
Very high source and drain dopings to avoid compensation effects at source and drain junctions.

4 cases: 2 uniform doping and 2 laterally graded.

Test circuit consisting of bias feeds and blocking capacitors on input and output.

# Backup: Quasi-1D structure (2 of 3)

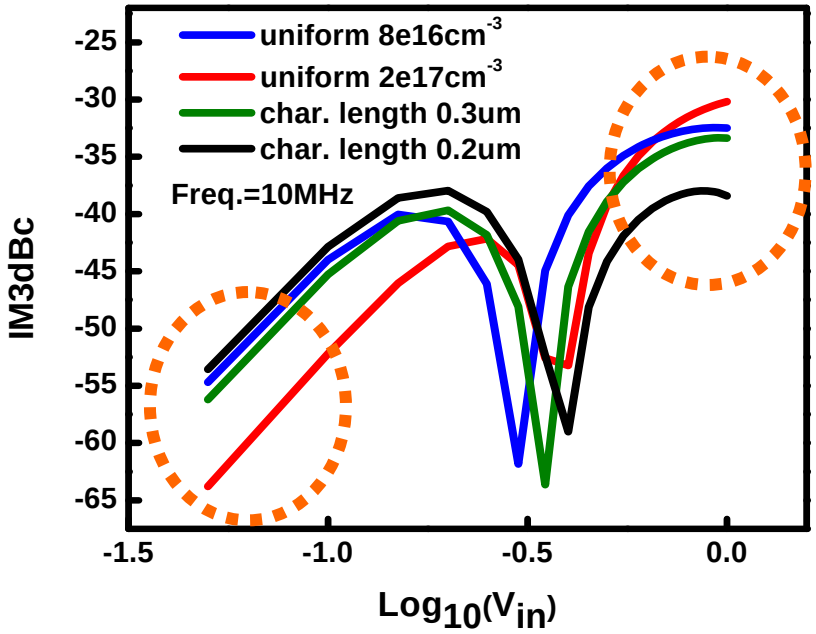
## gm3/gm:




Different gm3/gm magnitudes for different cases.

Devices were biased at gm3/gm minima, close to overall best linearity.

## IM3:

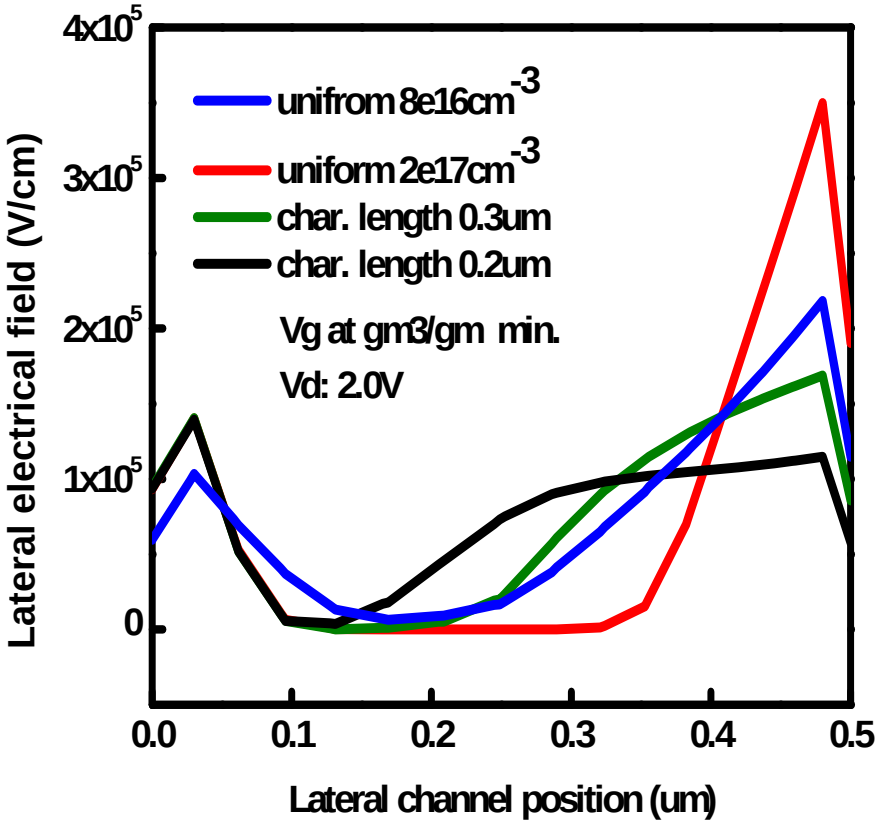



First data point correlates to magnitude of gm3/gm minima.

Shorter char. length / lower uniform doping: higher IM3 at low input power lower IM3 at high input power.

# Backup: Quasi-1D structure (3 of 3)

## Field distribution:



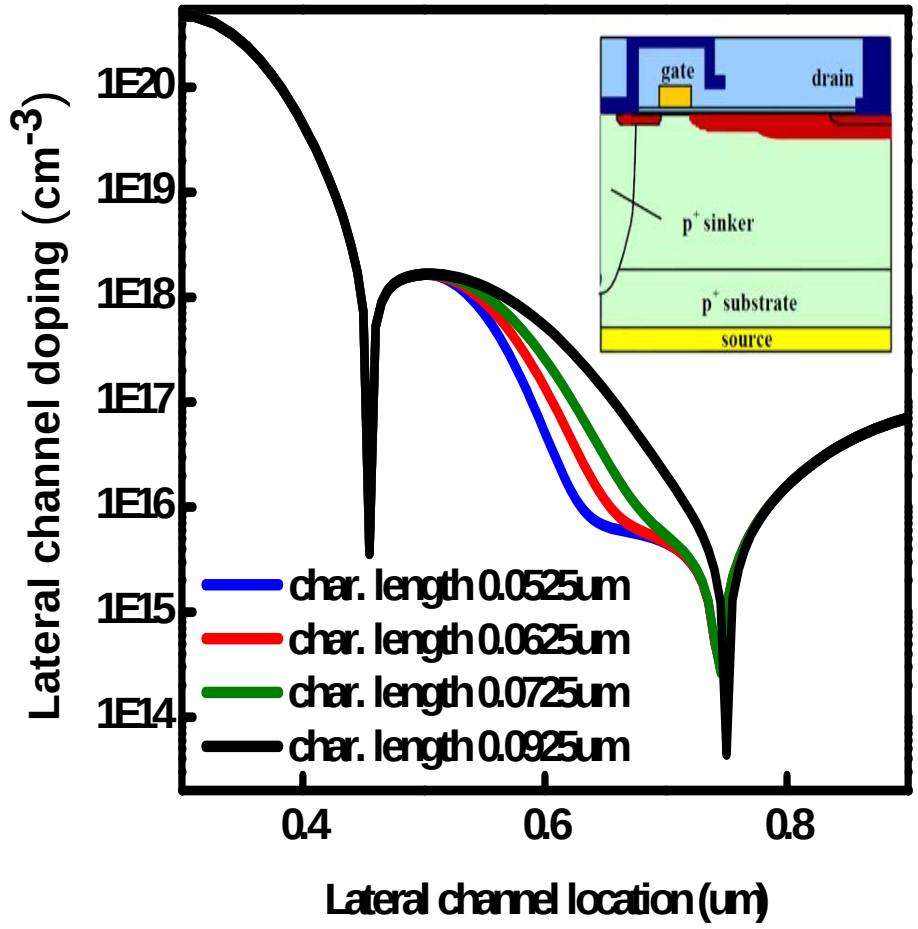

Graded cases → more uniform field.

Smaller uniform doping →more uniform field.

Uniform lateral field → better linearity at higher power.

# Backup: Realistic LDMOS (1 of 4)

**Device schematic (based on Infineon 7th generation design):**



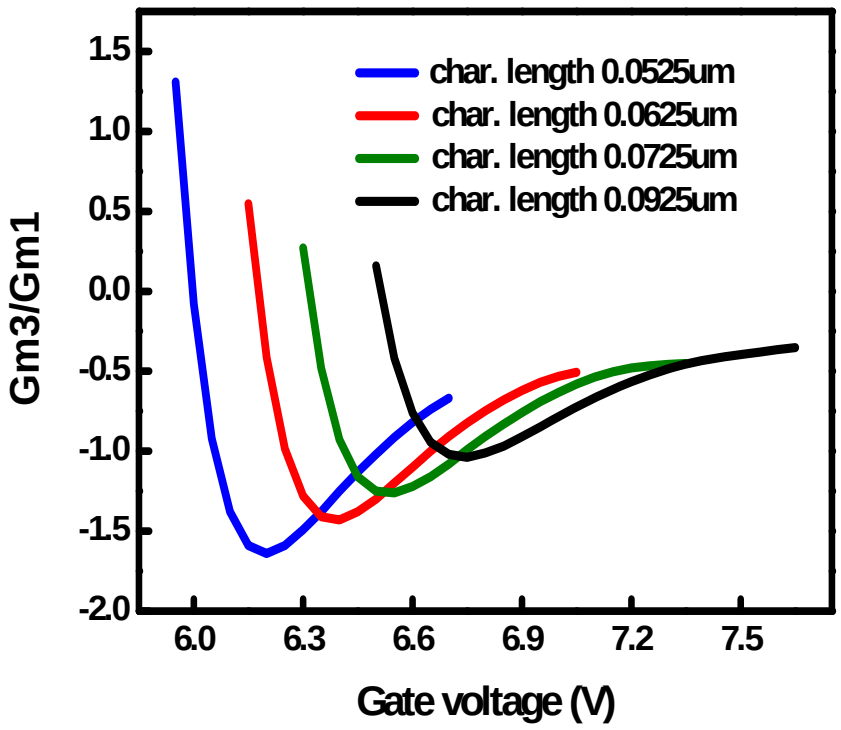

Two different lightly doped drain regions: optimize on-resistance and breakdown voltage.

Source doping and lightly doped drain kept the same for all cases.

Four different lateral grading cases in channel, defined through analytical expressions.

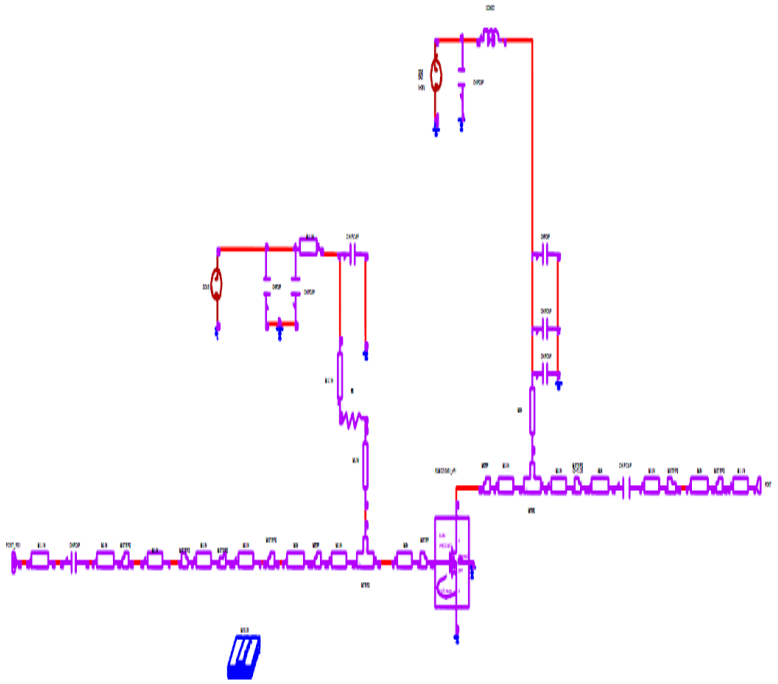
# Backup: Realistic LDMOS (2 of 4)

## gm3/gm:




Bias-point at gm3/gm minima.

## Test circuitry:

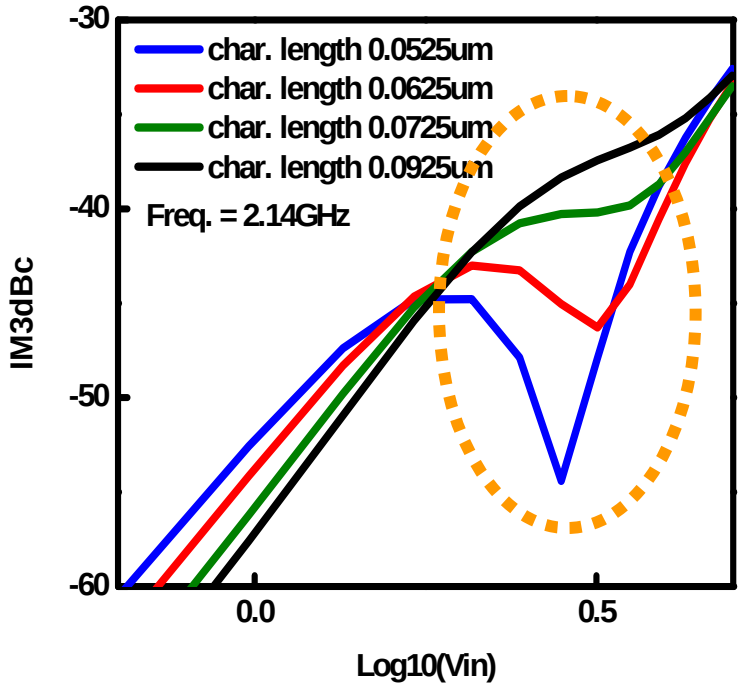


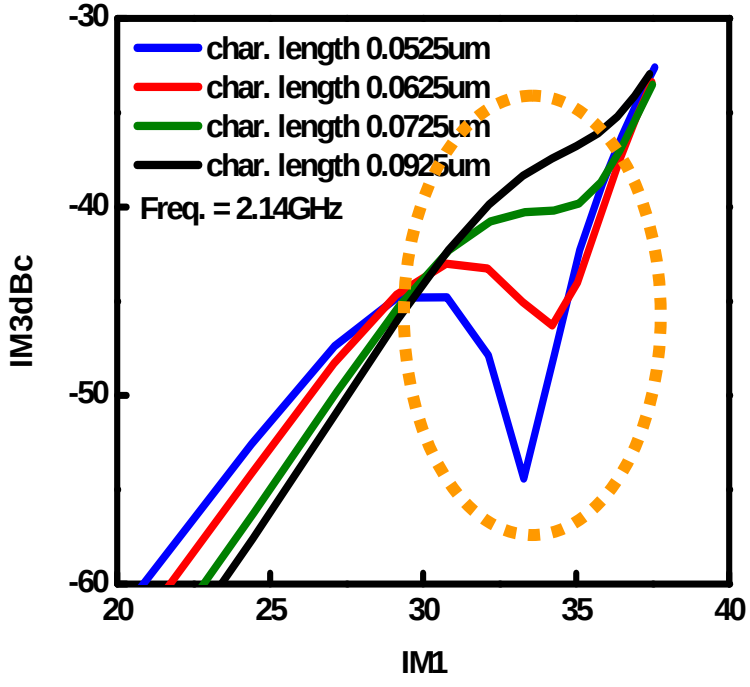
Circuitry with internal and external matching and bias.

Infineon product PTF210451.

# Backup: Realistic LDMOS (3 of 4)

## IM3 at 2.14GHz:



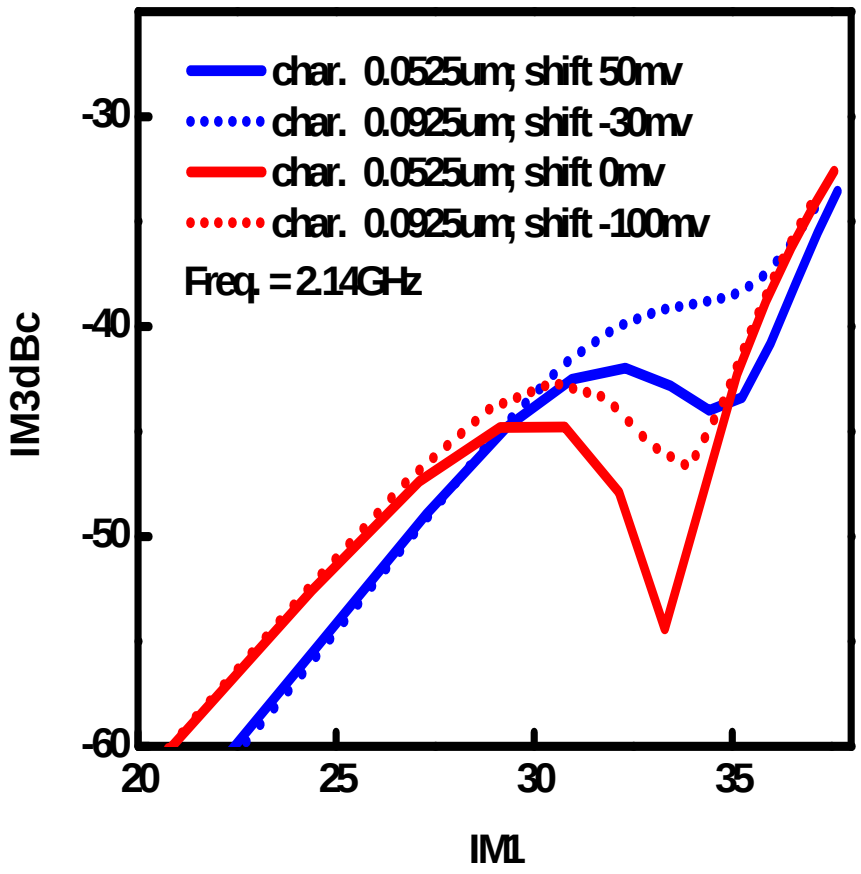




Effect of graded doping is significant → the nonlinearities in capacitances will not swamp the studied effects at high frequency.

More graded channel profile shows better linearity in the intermediate power regime.

# Backup: Realistic LDMOS (4 of 4)

## Vgs shifts from gm3/gm:




Vgs shifts from gm3/gm minima → IM3 change is quite sensitive.

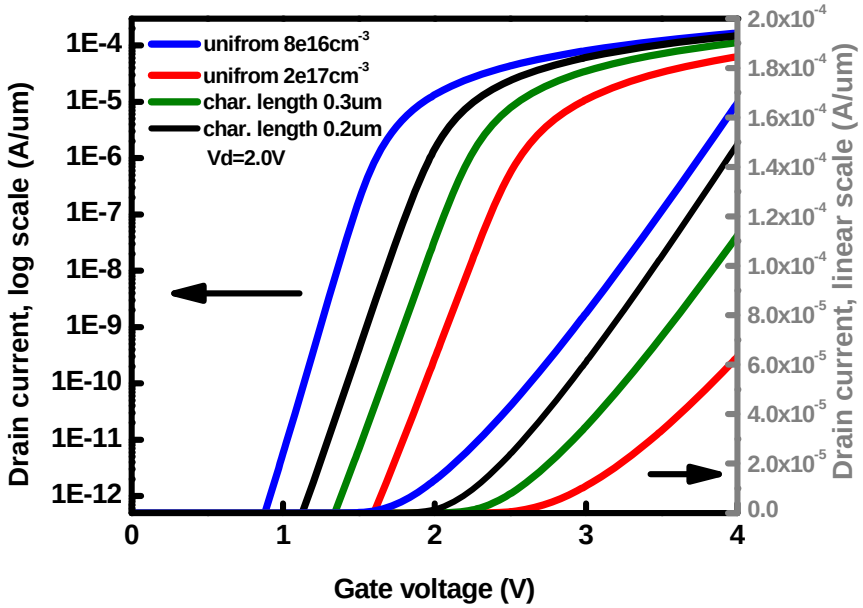
Different device designs give different IM3 that cannot be compensated for by simply changing Vgs bias (Idq setting).

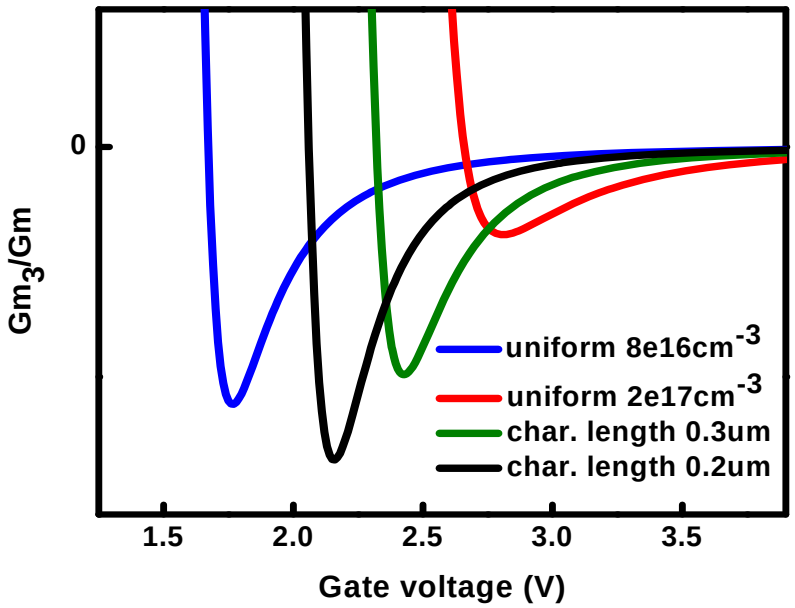
# Backup: Conclusions

- A graded channel has better linearity for intermediate to high powers. By contrast, for increased back-off, the situation is reversed.
- Nonlinearities in intrinsic capacitances will not swamp the effect of graded channel doping at high frequency.
- The effect of graded channel doping cannot be fully compensated for by adjusting the Idq bias point.
- The analysis lays ground-work for RF device optimization for improved linearity.

# Backup: Additional information (1 of 4)

## Quasi-1D structure: IdVgs



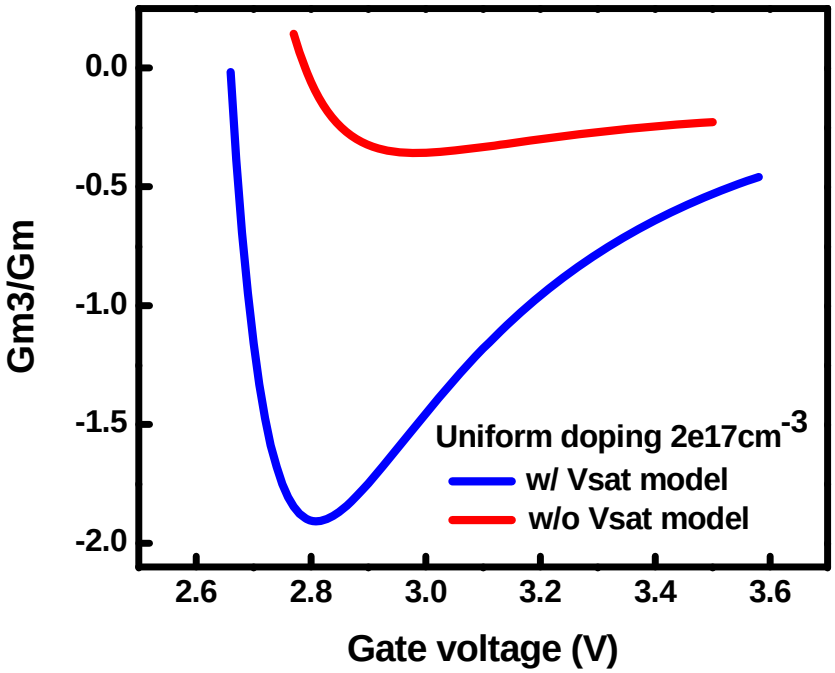

Clearly different gm3/gm magnitudes for different cases.

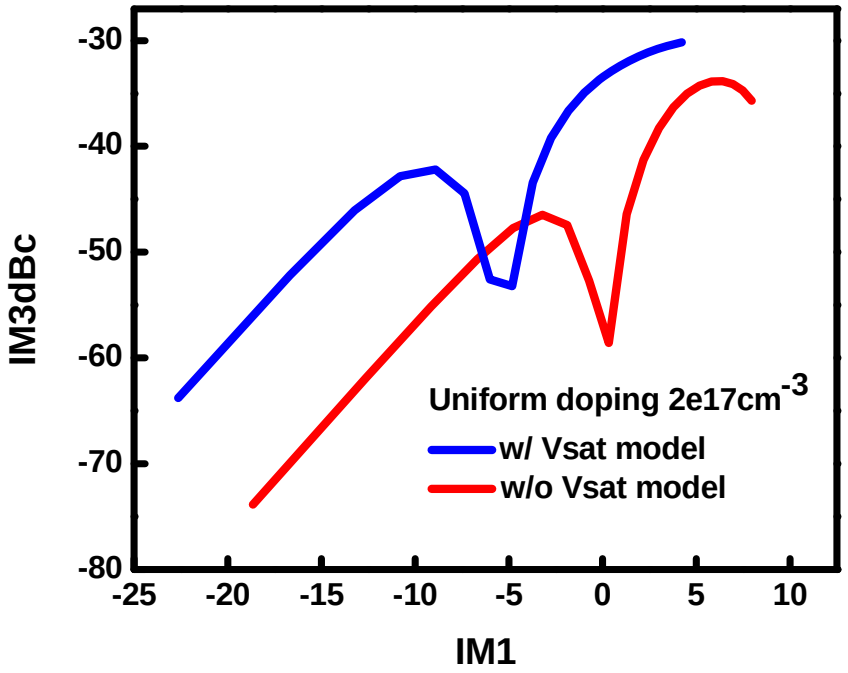
Shorter characteristic length and lower doping give larger gm3/gm magnitudes.

Devices were biased at gm3/gm minima, close to overall best linearity for many applications.

# Backup: Additional information (2 of 4)

## Quasi-1D structure: velocity saturation:



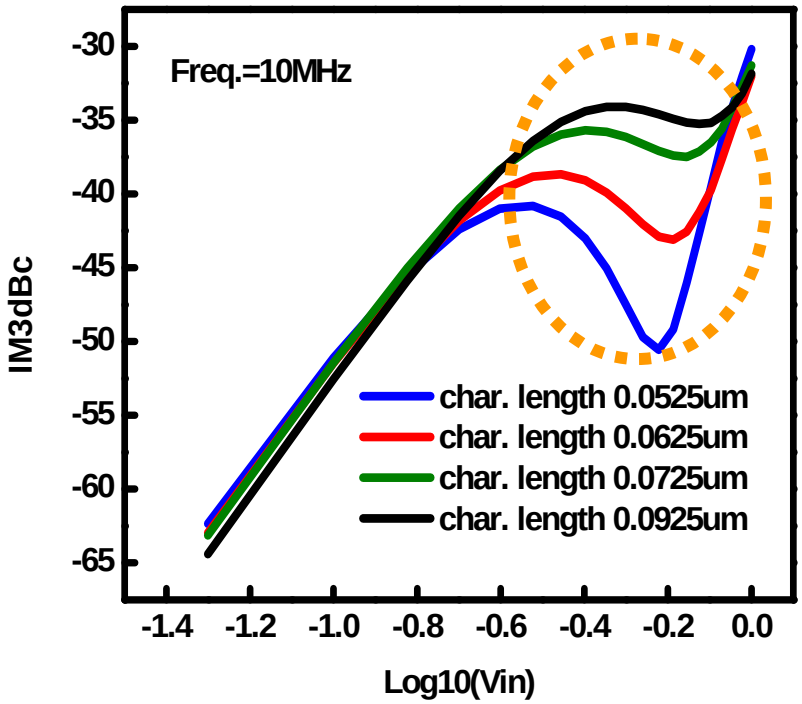



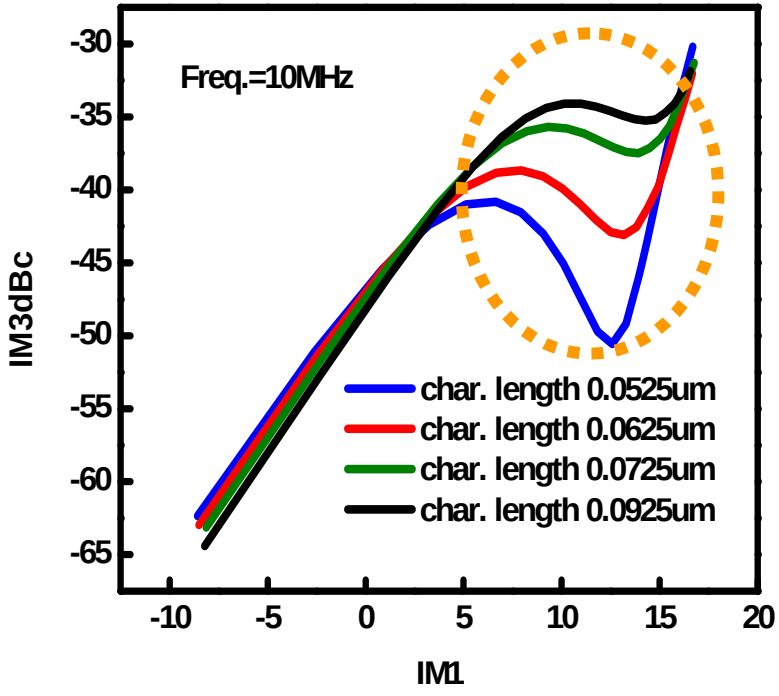

When Vsat model is not included:

1. gm3/gm shifts to a smaller magnitude.
2. IM3 is much lower, both initially and for high powers.

# Backup: Additional information (3 of 4)

## Realistic LDMOS: IM3 at 10MHz



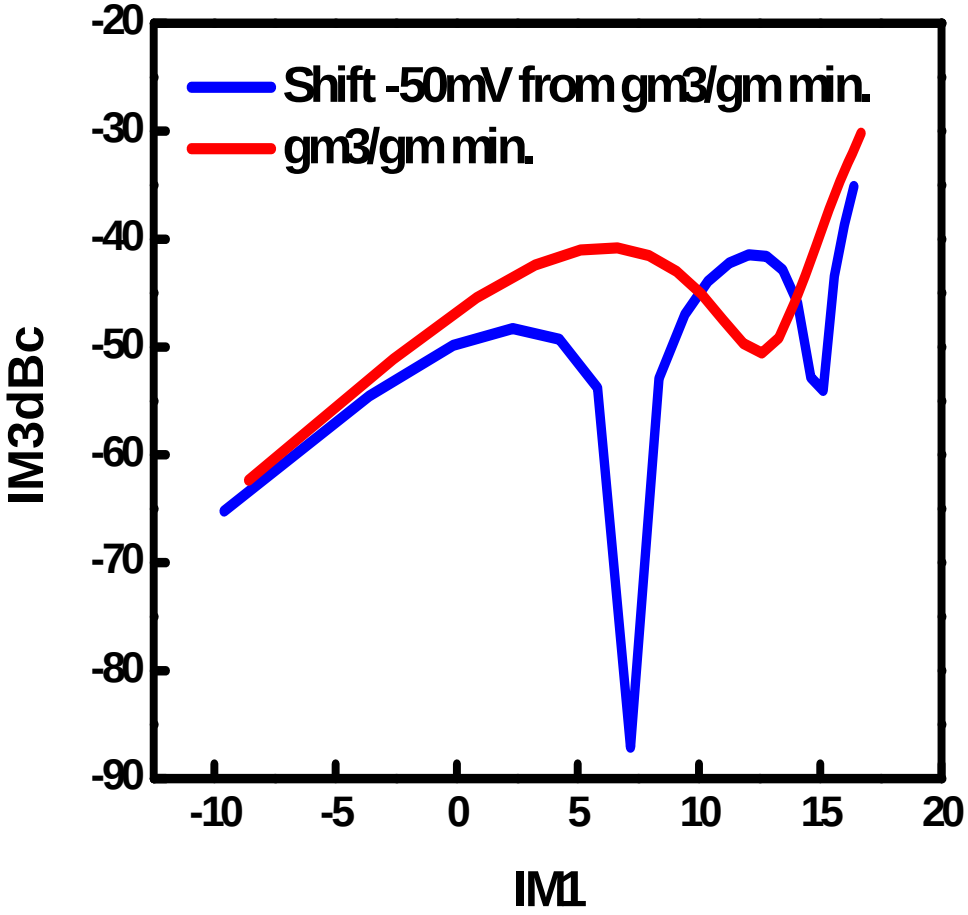




First, separate nonlinearities in static IV from capacitive effects → low freq. 10MHz.

More graded channel profile shows better linearity in intermediate power regime.

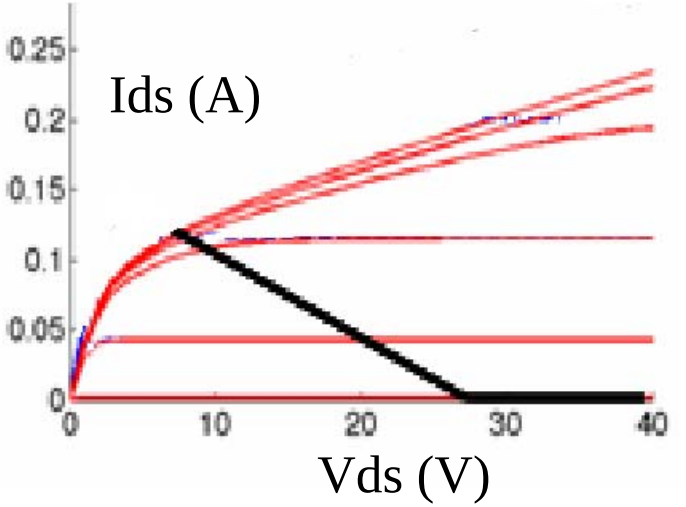
# Backup: Additional information (4 of 4)

## Realistic LDMOS: two sweet spots

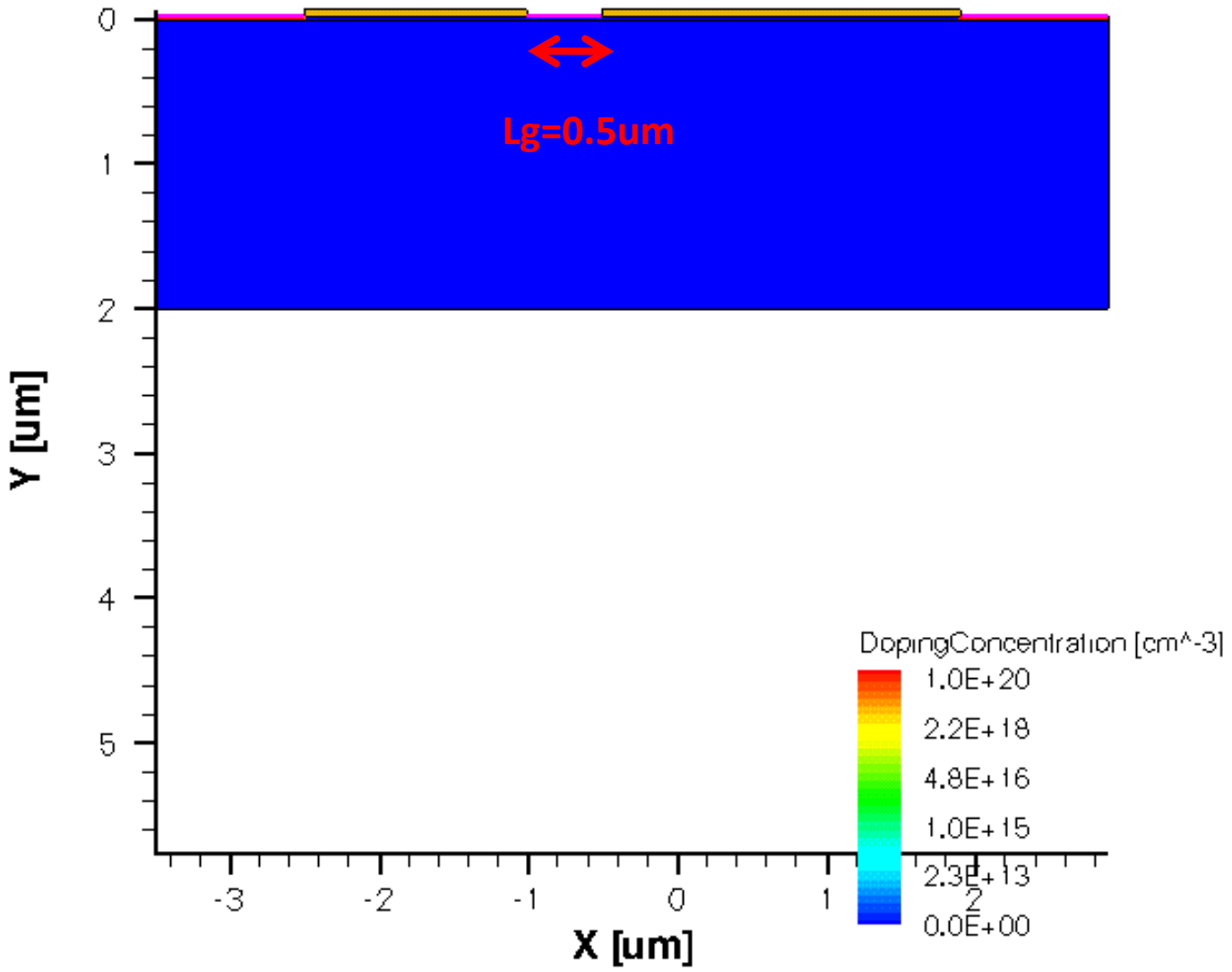



At high power, the compressing non-linearity along the load-line will dominate; the curves merge.

Lower Vgs → two sweet-spots appear.

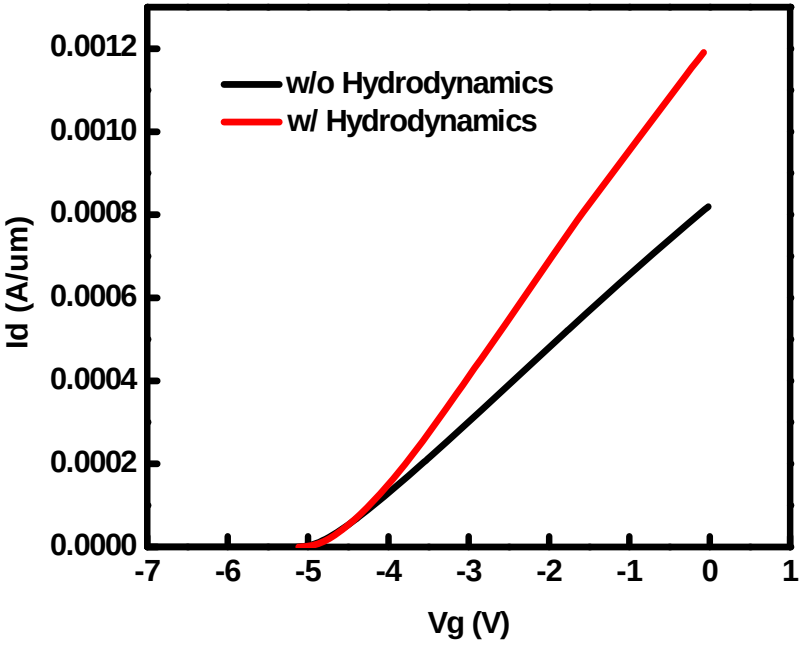


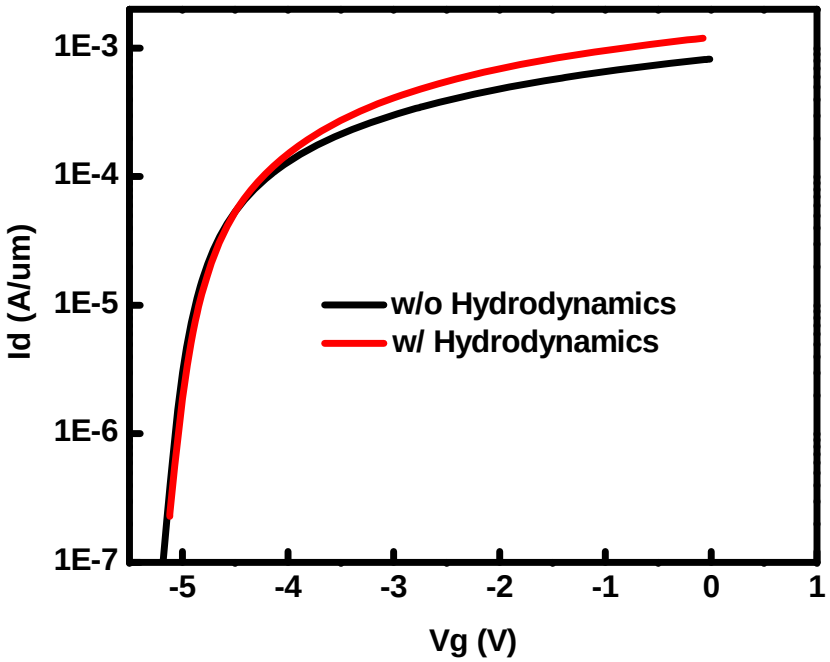
# Backup: GaN HEMT structure



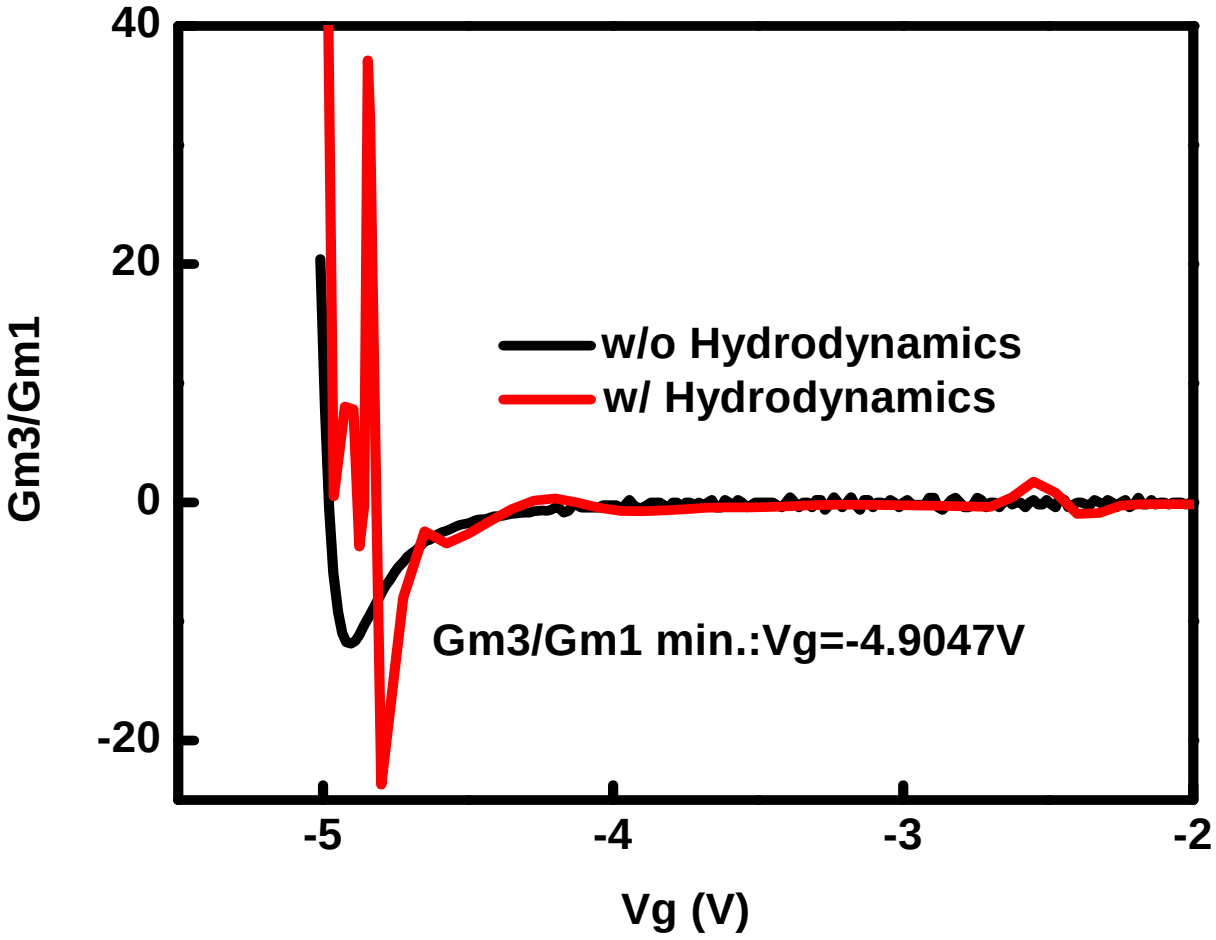
# Backup: Id-Vgs, GaN HEMT

## TCAD simulation results

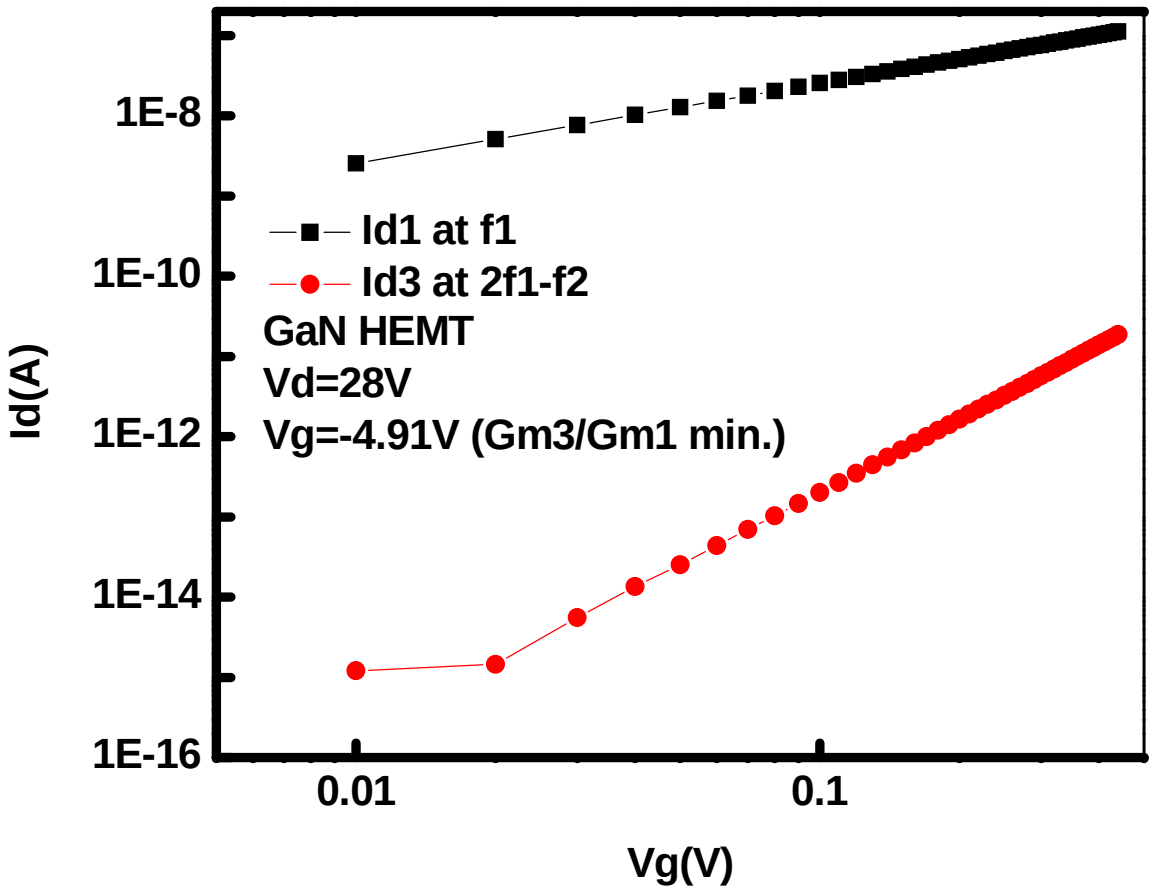


# Backup: Gm3/Gm1, GaN HEMT

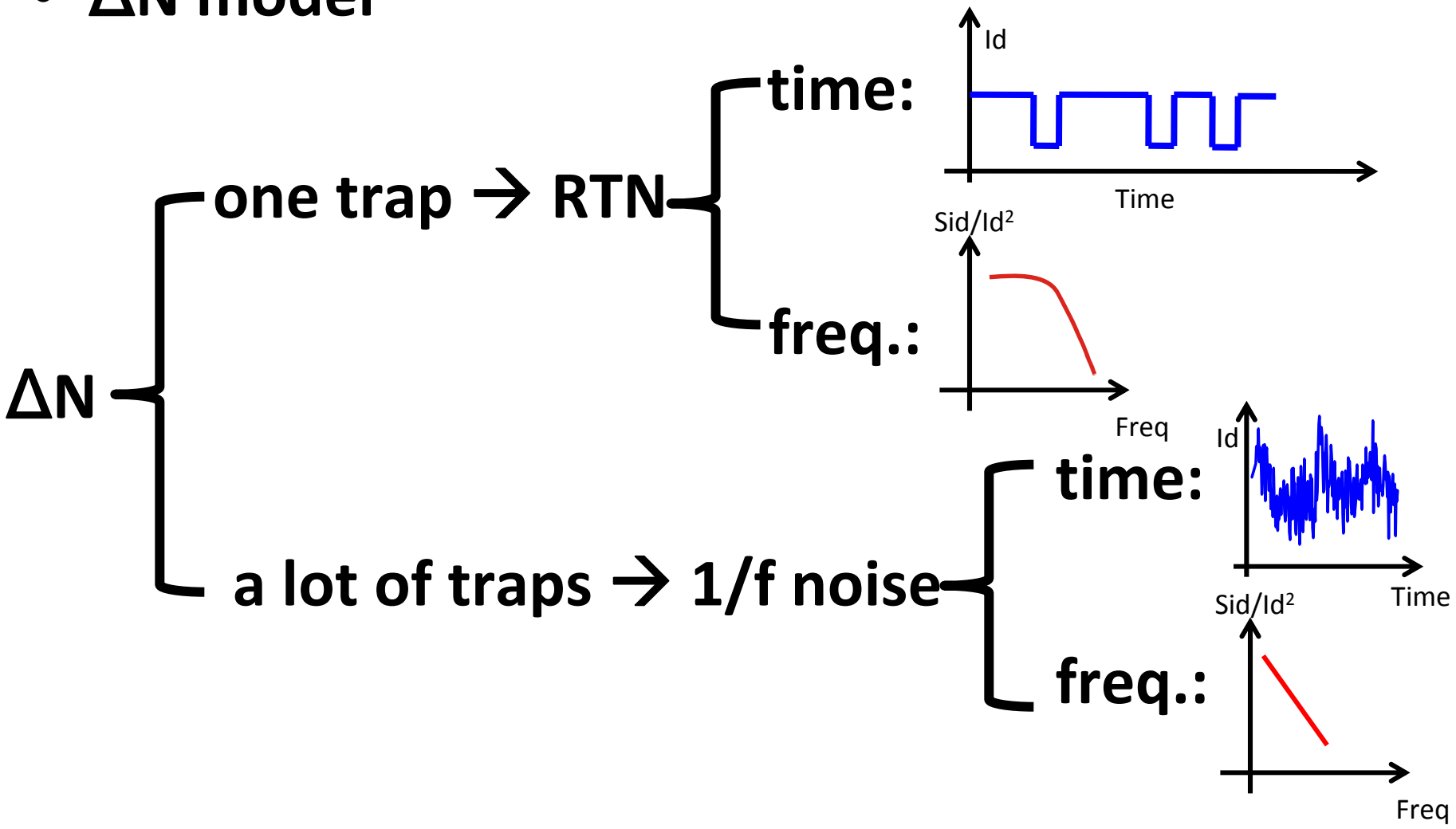


# Backup: Linearity, GaN HEMT



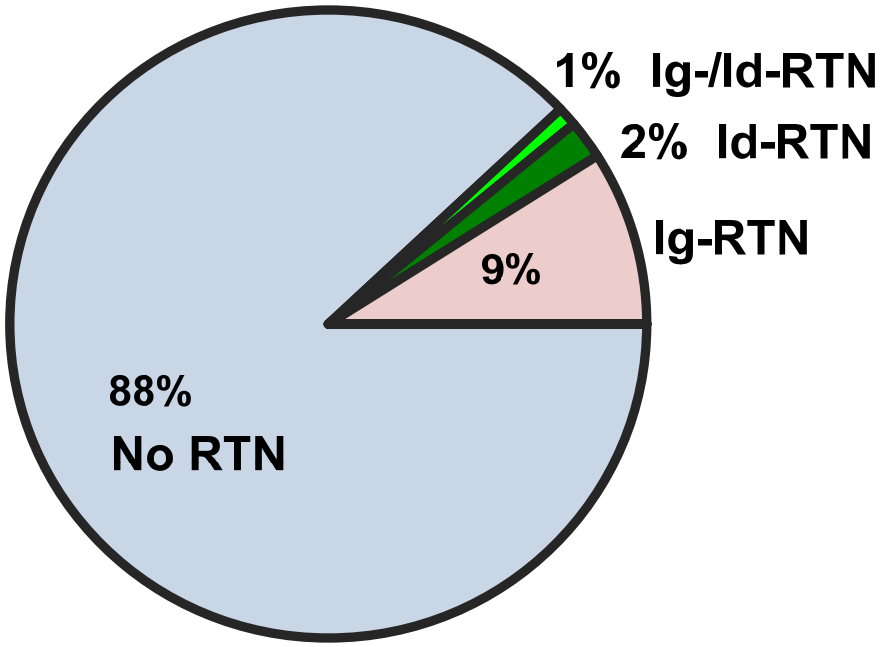
# Backup: The origin of LF noise

- ΔN model



# Backup: Statistics

- **Statistical results**

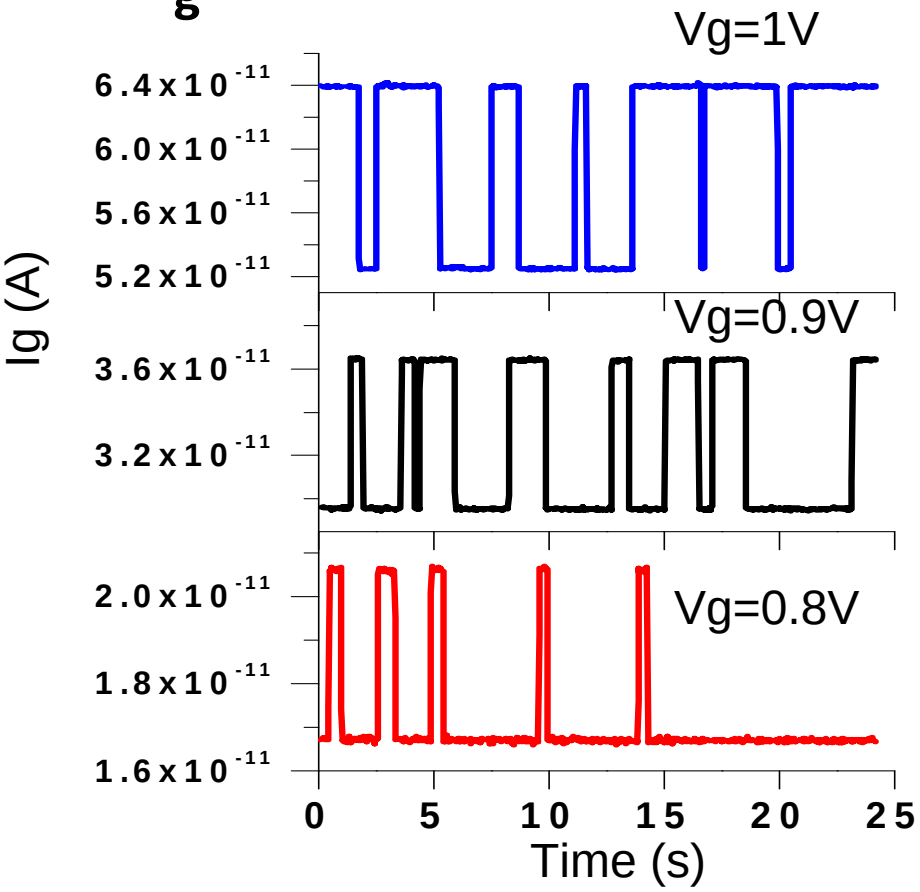


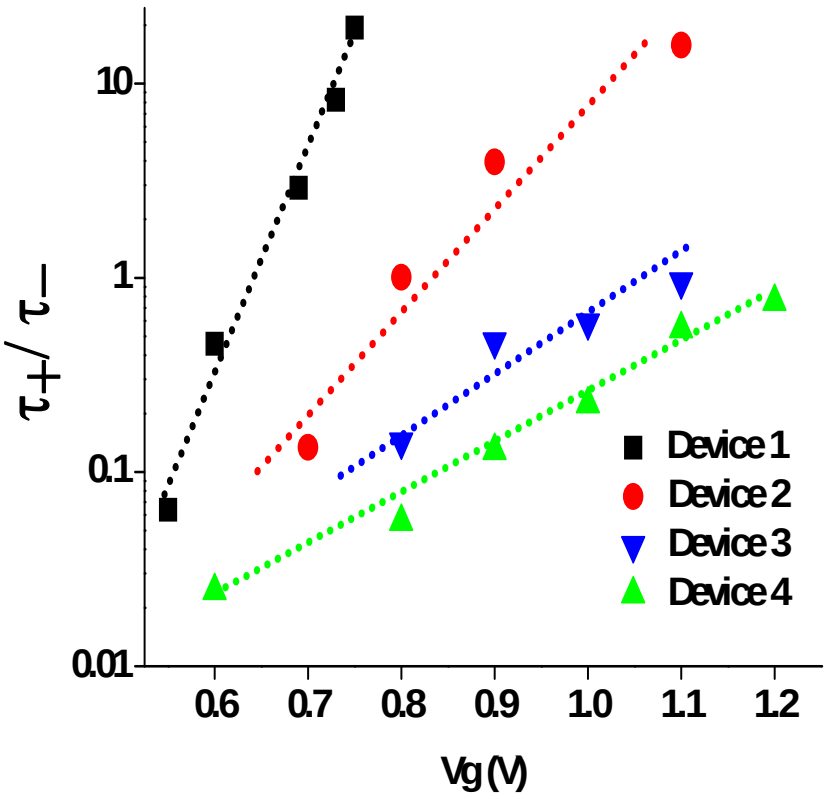

**About 12% MOSFETs show RTN: 9% Ig-RTN, 2% $I_d$-RTN, and 1% $I_g$-/$I_d$-RTN.**

**The statistical results are from 1000 devices with the same technology and structures.**

# Backup: Gate bias

- $I_g$-RTN

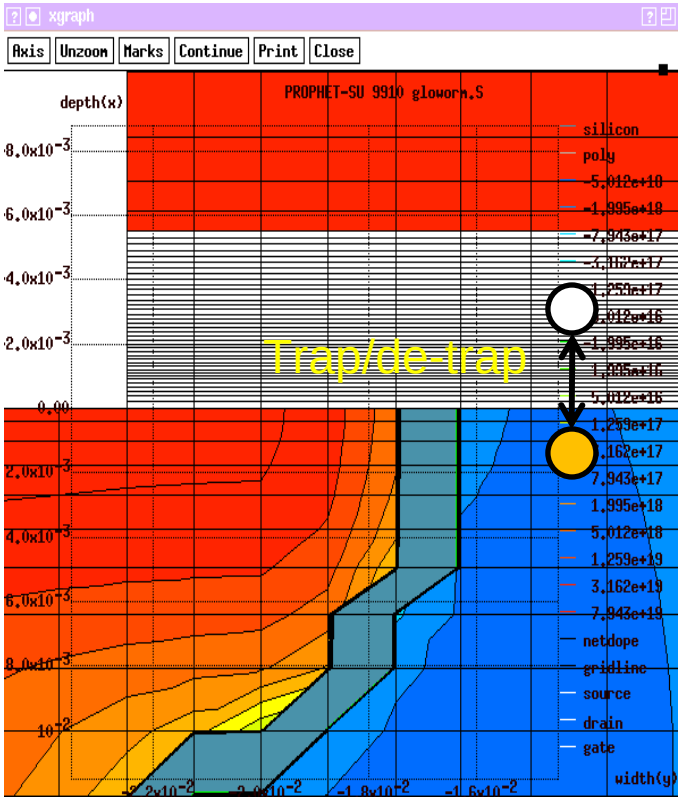



  - $V_g$ increases: Time in high-$I_g$ state increases.

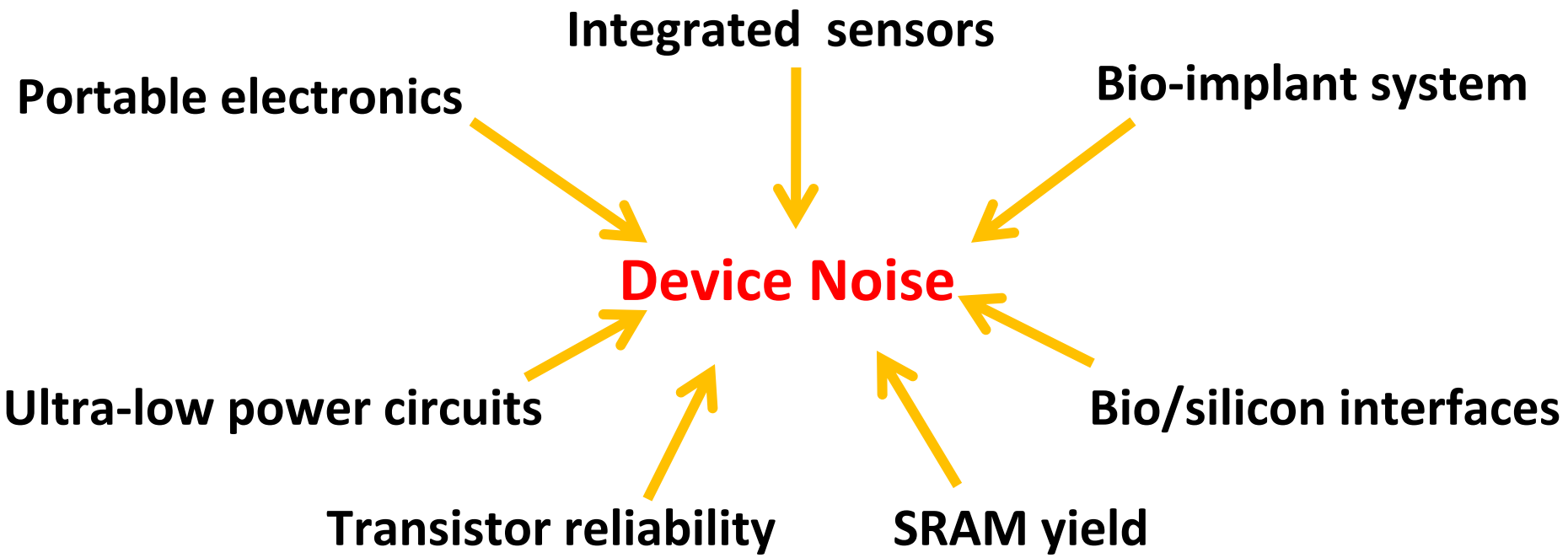
# Backup: TCAD

- $I_d$-RTN: High gm bias condition



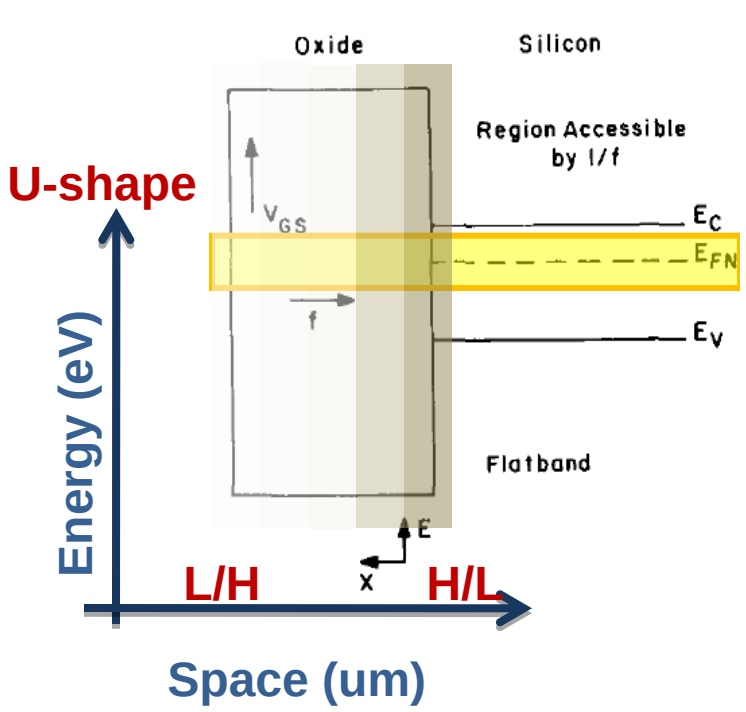

– TCAD simulations confirm the origin of RTN can be from one-trap/de-trap.

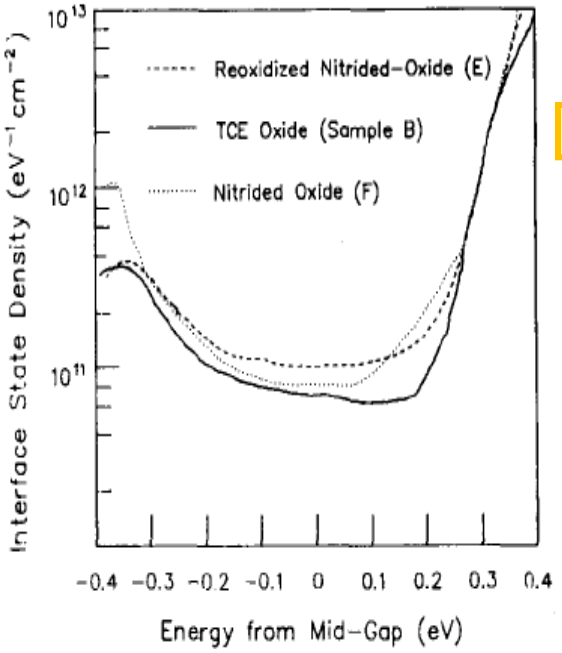
# Backup: Motivation

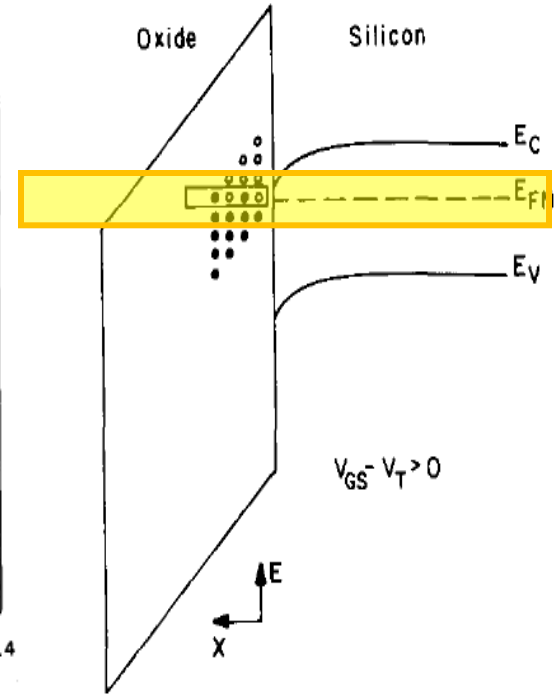



- **Noise: key issue for the future electronic system development.**

# Backup: Trap distribution (1 of 2)



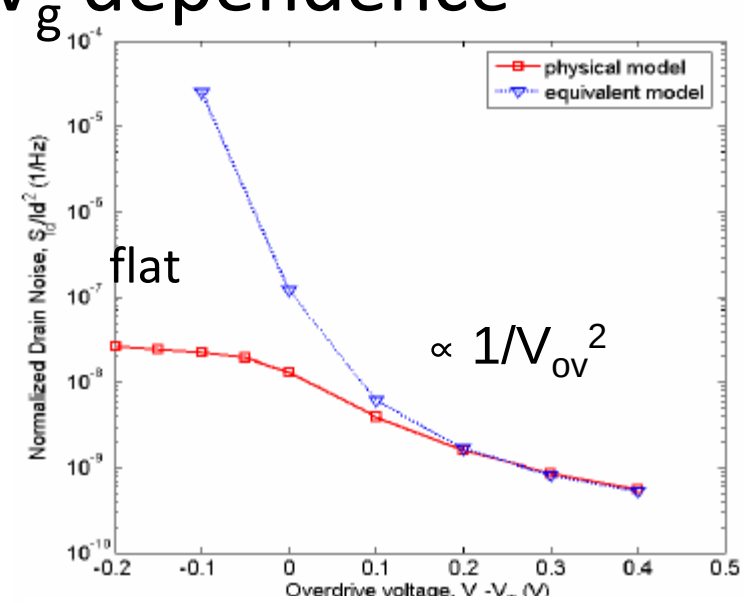

- Space: from gate to Si can be low-high or high-low.
- Energy: distribution is a U-shape in log-scale.


R. Jayaraman et al. *IEEE T-ED*, vol.36, no. 9, pp. 1773-1782, Sept., 1989.

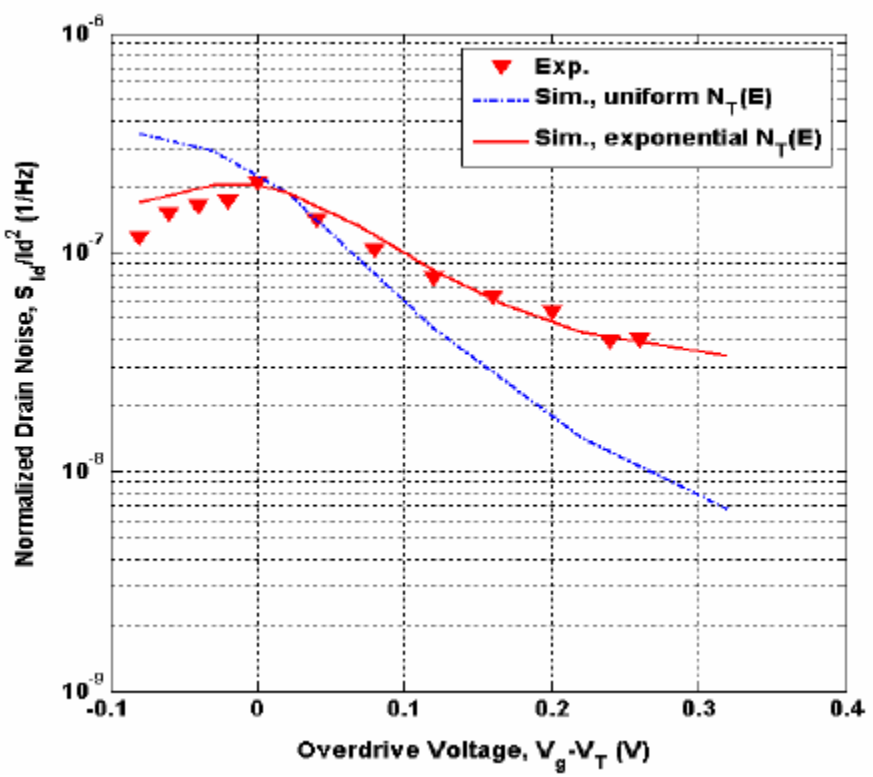
H. Wong et al. *IEEE T-ED*, vol.37 no. 7, pp. 1743-1749, July, 1990.

# Backup: Trap distribution (2 of 2)

- $V_g$ dependence




$$R = \frac{\delta \Delta N}{\delta \Delta N_t} = -\frac{C_i}{C_{ox} + C_i + C_d + C_{it}}$$



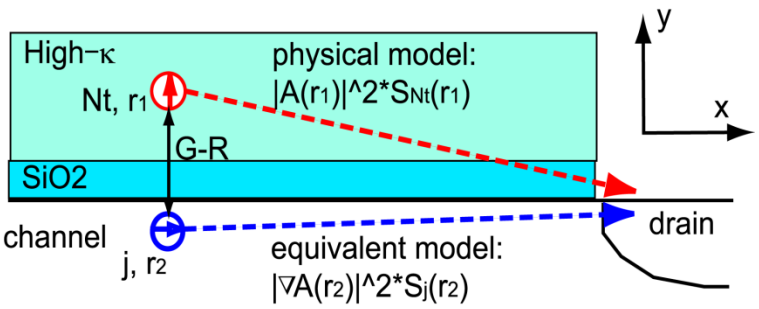

  - $V_g$ dependence shows flat region in weak inversion regime.
  - In the U-shape distribution $V_g$ dependence is less sensitive compared with uniform distribution.


K. K. Hung et al. *IEEE T-ED*, vol.37, no. 5, pp. 1323-1333, May, 1990.

Y. Liu et al. *SISPAD 2006*, pp. 99-102, 2006.

# Backup: Numerical method (1 of 2)

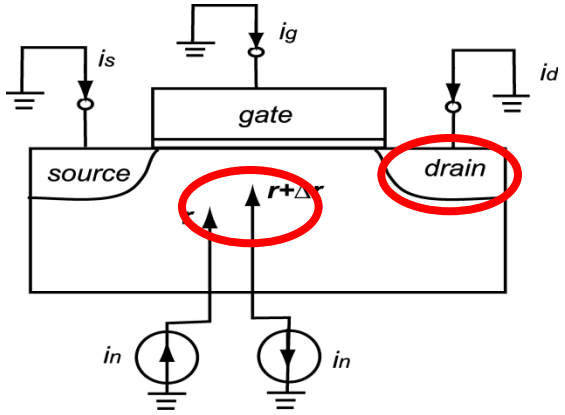
- Physical model




$$S_{nt}(\vec{r}) = 2(G+R)$$

$$dn_t / dt = G - R$$
$$= \left[(N_T - n_t)/\tau - n_t \exp(E_T - E_F / k_B T)/\tau\right]$$

- Impedance field method (IMF)




$$A_k(\vec{r}) = \frac{Current \quad fluctuatio\ n\ at\ kth\ electrode}{Injected \quad current \quad at\ \vec{r}\ in\ the\ device}$$

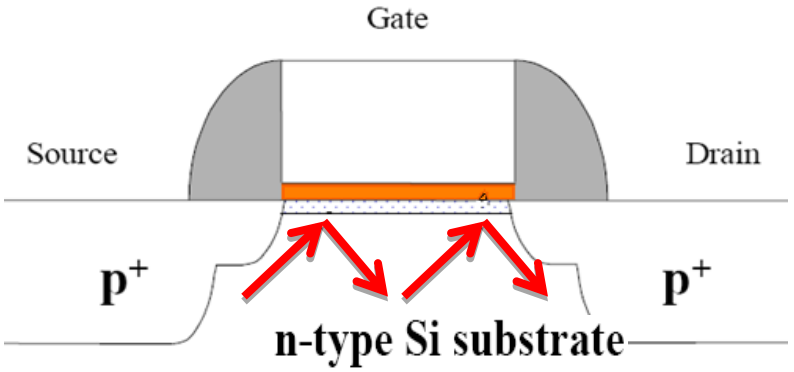
$$S = \int \left|A(\vec{r})\right|^2 S_{in}^{(s)}(\vec{r})\,dv$$


[5] A. McWhorter, *Semiconductor Surface Physics*, PA, Univ. Pennsylvania Press,1957, pp. 207-208.

[6] W. Shockley et al., *Quantum Theory of Atoms, Molecules and Solid State*, NY: Academic, 1966, pp. 537-563.

# Backup: Numerical method (2 of 2)

- Hooge mobility fluctuation (Δu model)
  - Bulk phonon scattering




  - Empirical equation

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_H}{WLQ_i f}$$

  - Numerical approach: Post process

    Hooge model is empirical → the post process with simulated parameters/reasonable $\alpha_H$ is used.

[7] F. N. Hooge, *IEEE T-ED*, vol.41, no. 11, pp. 1926-1935, Nov., 1994.

# Backup: Unified model (1 of 4)

- The fluctuating oxide charge density $\triangle Q_{ox}$ is equivalent to a variation in the flat-band voltage

$$\delta V_{fb} = -\delta Q_{ox} / C_{ox}$$

- The fluctuation in the drain current yields

$$\delta I_D = \frac{\partial I_D}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_D}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \qquad S_{I_D} = S_{V_{fb}} \left( 1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m} \right)^2 g_m^2$$

**Fluctuation of Num.** **Fluctuation of correlated mobility**

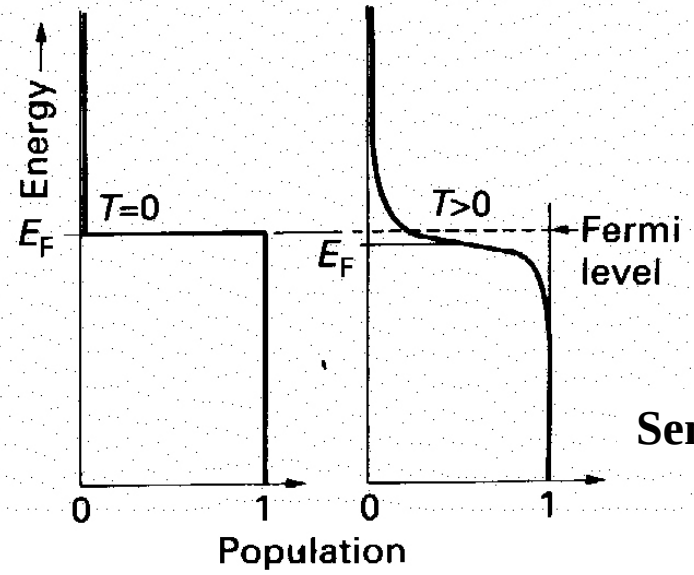
- The first term in the parentheses is due to fluctuating number of inversion carriers and the second term to correlated mobility fluctuations.

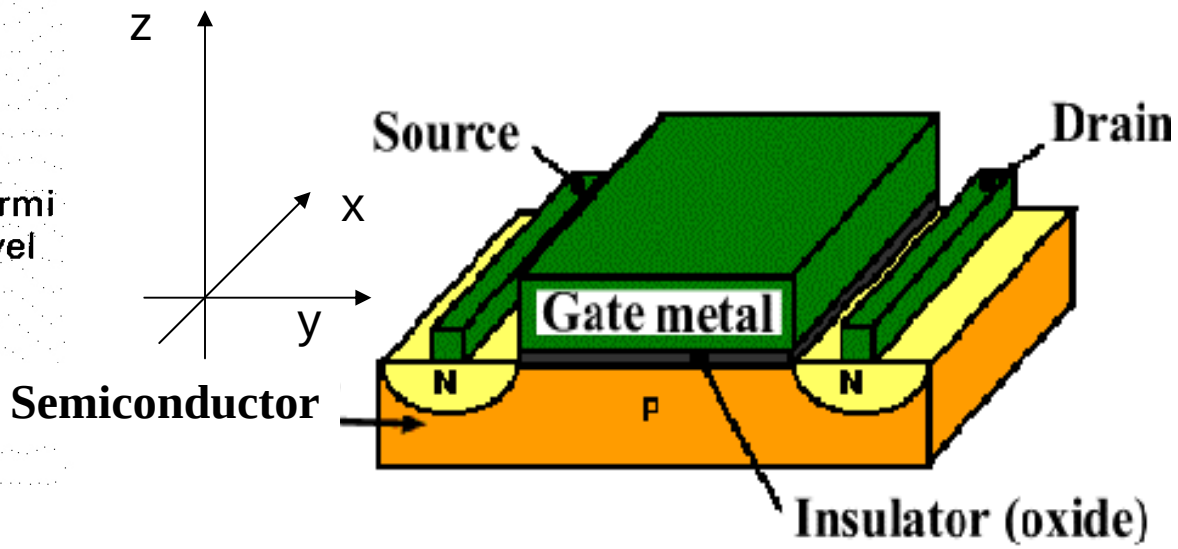
# Backup: Unified model (2 of 4)

- The power spectral density of the flat-band voltage fluctuations is calculated by summing the contributions from all traps in the gate oxide.

Fermi-Dirac distribution

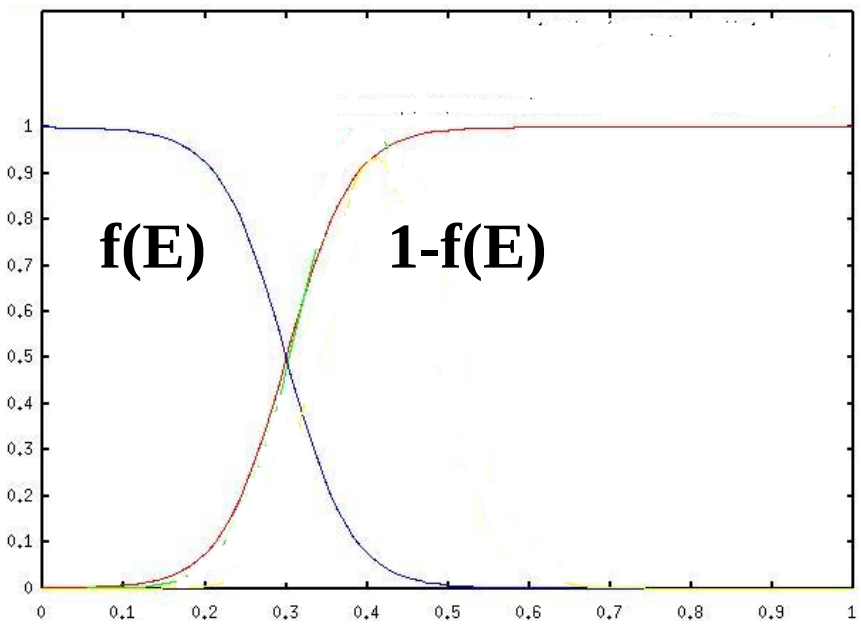
$$S_{Q_{ox}} = S_{V_{fb}} C_{ox}^2 = \frac{q^2}{W^2 L^2} \int_{E_v}^{E_c} \int_0^W \int_0^L \int_0^{t_{ox}} 4N_t f(E)(1-f(E)) \frac{\tau}{1+(2\pi f\tau)^2} dx dy dz dE$$

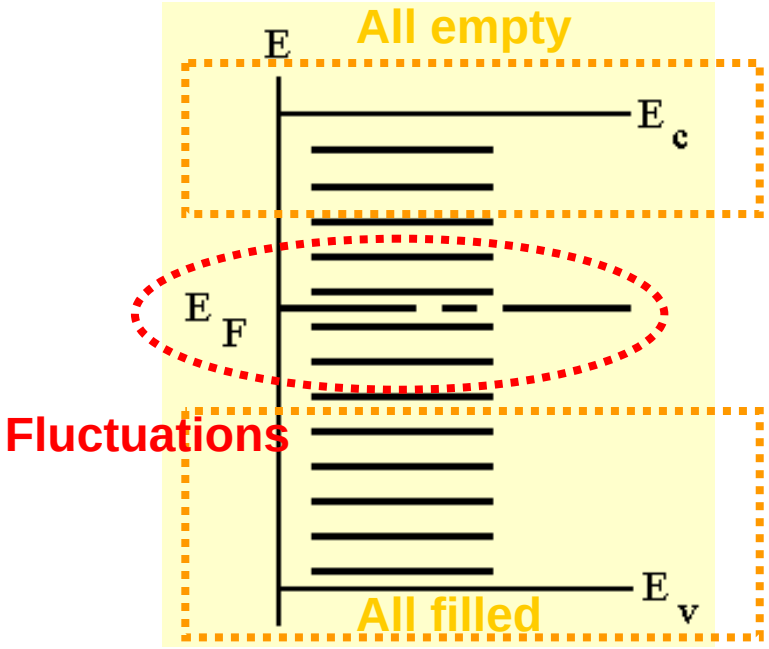


# Backup: Unified model (3 of 4)

- The product *f*(E)(1-*f*(E)) is sharply peaked around the quasi-Fermi level
- If the Fermi-level is far above or below the trap level, the trap will be filled or empty.



# Backup: Unified model (4 of 4)

$$S_{Q_{ox}} = \frac{q^2 kT}{WL} \int_0^{t_{ox}} 4N_t \frac{\tau}{1+(2\pi f\tau)^2} dz$$

→ Lorentzian spectrum

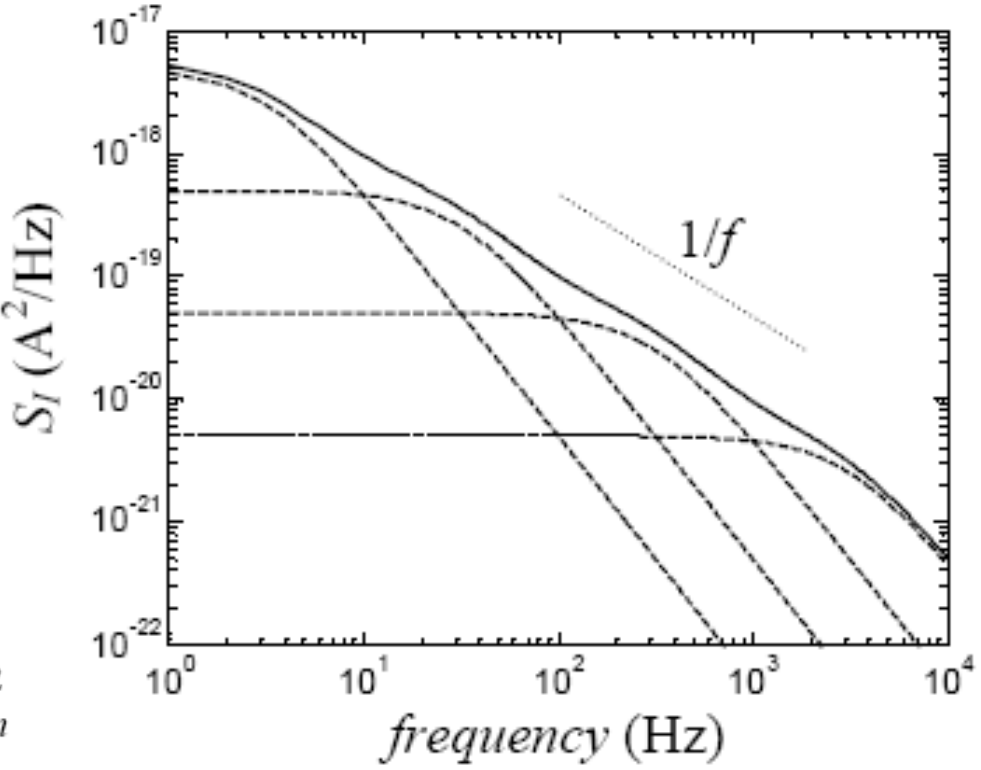
The trapping time constant (quantum tunneling)

$$\tau = \tau_0(\mathrm{E}) \cdot e^{z/\lambda}$$

Tunneling attenuation length

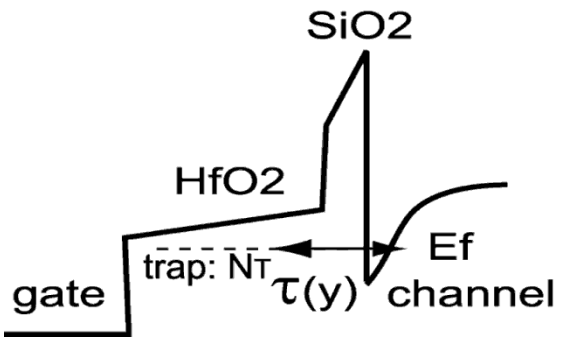
$$S_{V_{fb}} = \frac{q^2 kT\lambda N_t}{f^\gamma WLC_{ox}^2}$$

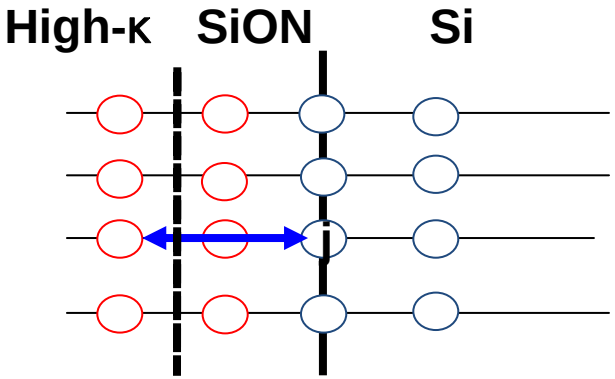
$$S_{I_D} = S_{V_{fb}} \left(1 + \frac{\alpha\mu_{eff} C_{ox} I_D}{g_m}\right)^2 g_m^2$$

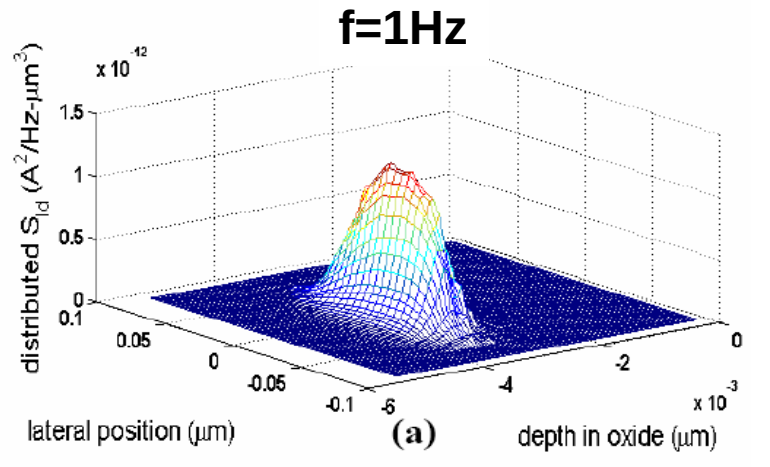


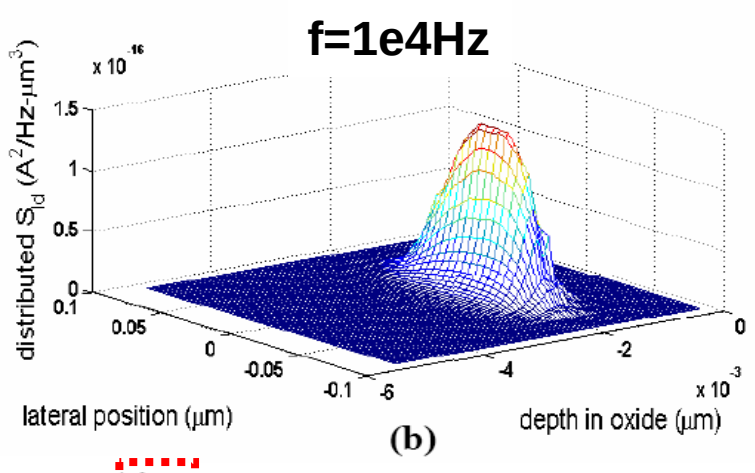
# Backup: High-κ

- Numerical approach




Different affinities and tunneling are considered→ $\gamma = \frac{4\pi}{h}\sqrt{2m^*\Phi}$ $\tau = \tau_0(\mathrm{E}) \cdot e^{z/\lambda}$

$1/\gamma$

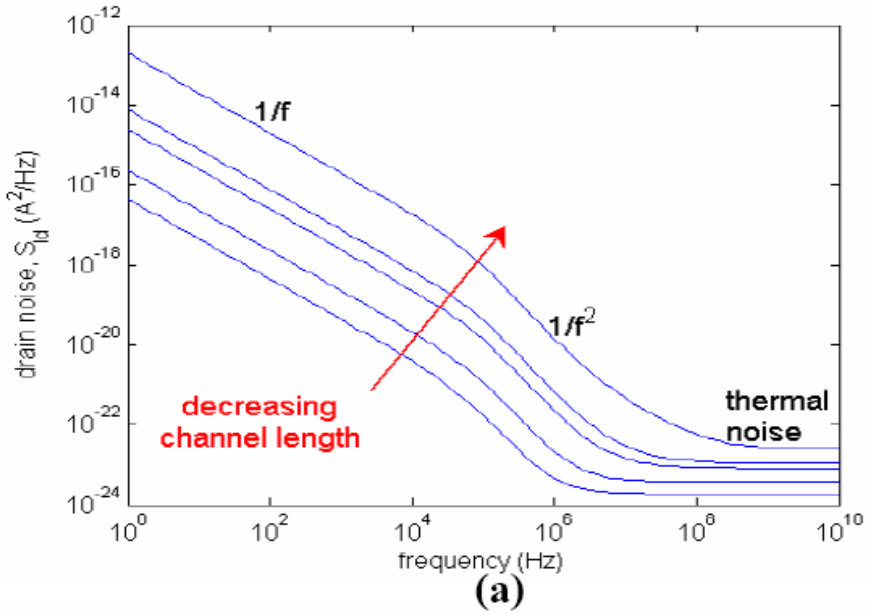
$SiO_2$: 1×10$^{-8}$ cm

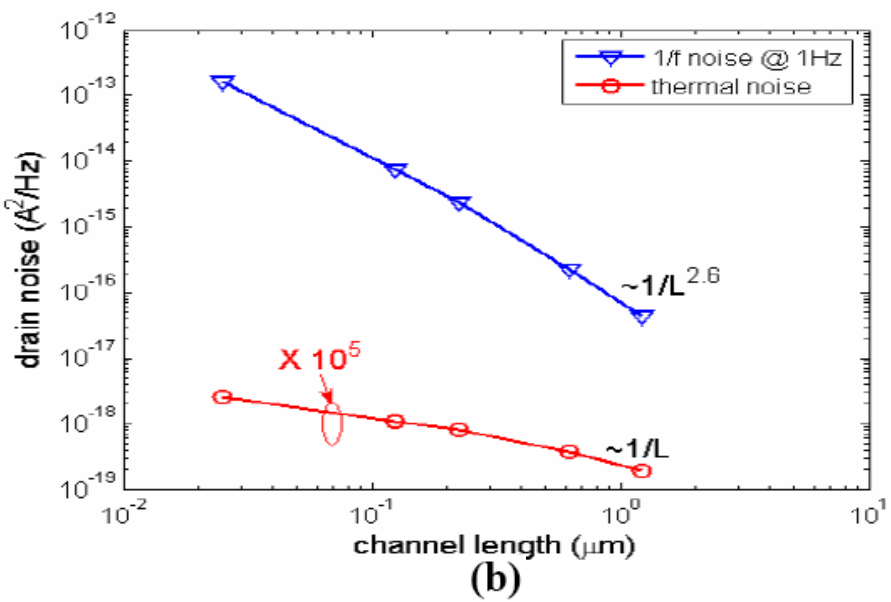
$HfO_2$: 2.1×10$^{-8}$ cm

[9] Y. Liu et al. *SISPAD 2006*, pp. 99-102, 2006.

# Backup: Noise scaling (1 of 2)

- Scaling trend: general trend

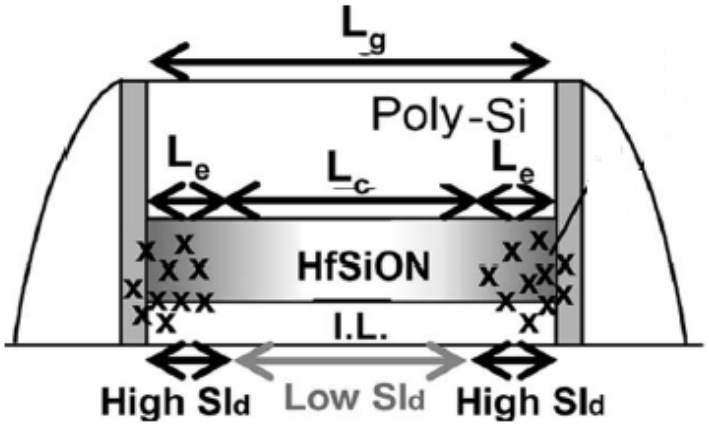



  - $SiO_2$ trap density is much smaller than that of $HfO_2$.
  - 1/f noise increases much faster than the thermal noise when size scales down.

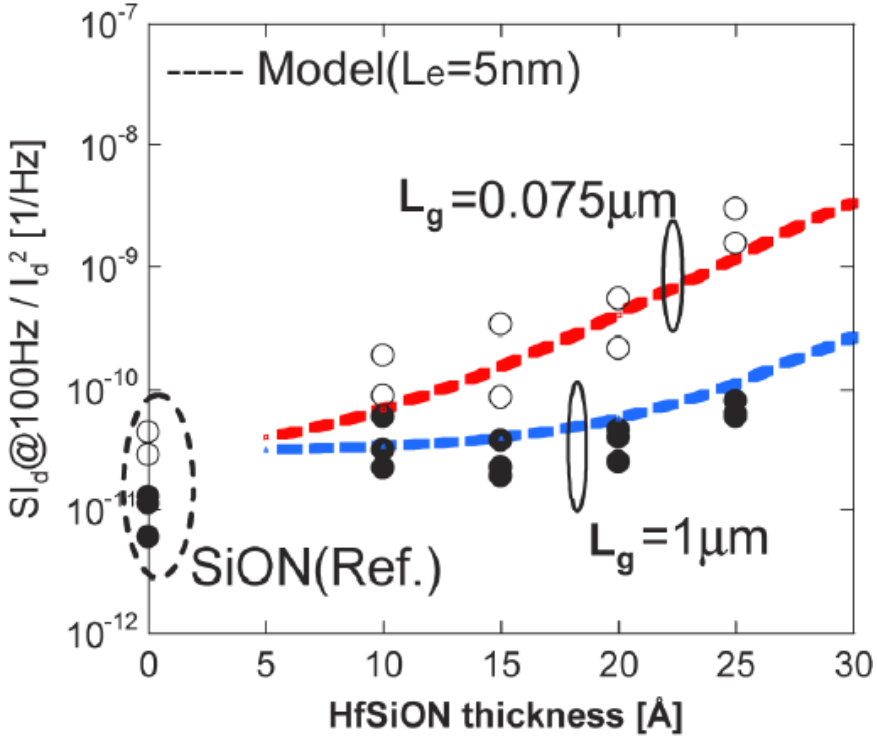
# Backup: Noise scaling (2 of 2)

- Scaling trend: traps at gate edge




$$SI_d/I_d^2 \propto N_t$$

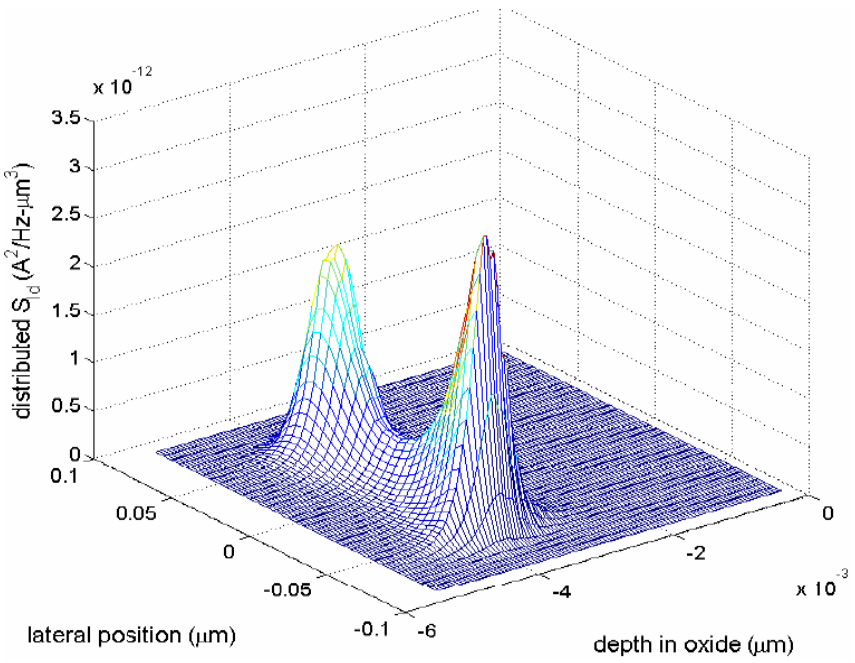
$$N_{t,\mathrm{HfSiON}} = (2 \times N_e \times L_e + N_c \times L_c)/L_g$$

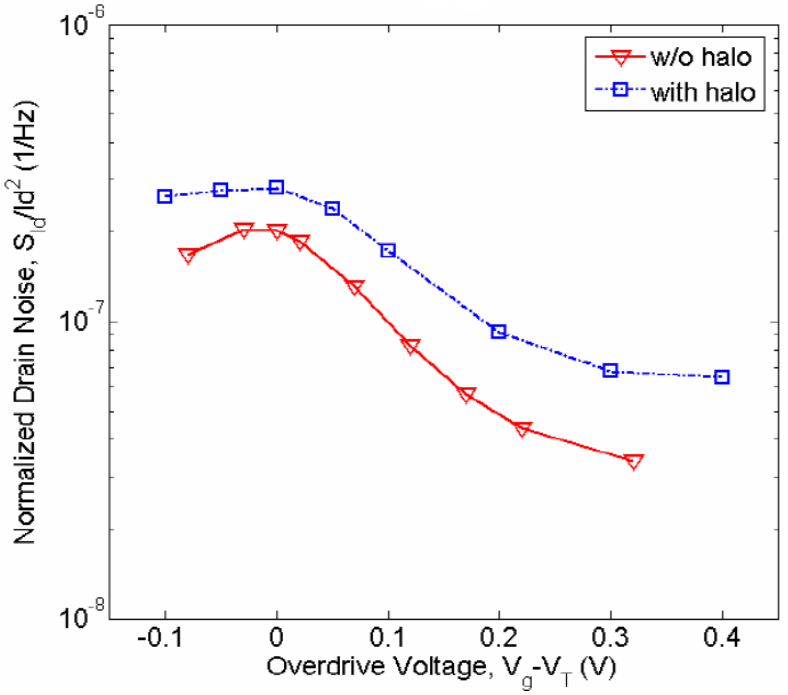



- High trap density in the gate edge region.
- In the scaled devices traps in the gate edge becomes important so $S_{id}/I_d^2$ increases significantly.

[14] Y. Yasuda et al., *IEEE T-ED*, vol.55, no. 1, pp. 417-422, Jan., 2008.

# Backup: Halo doping

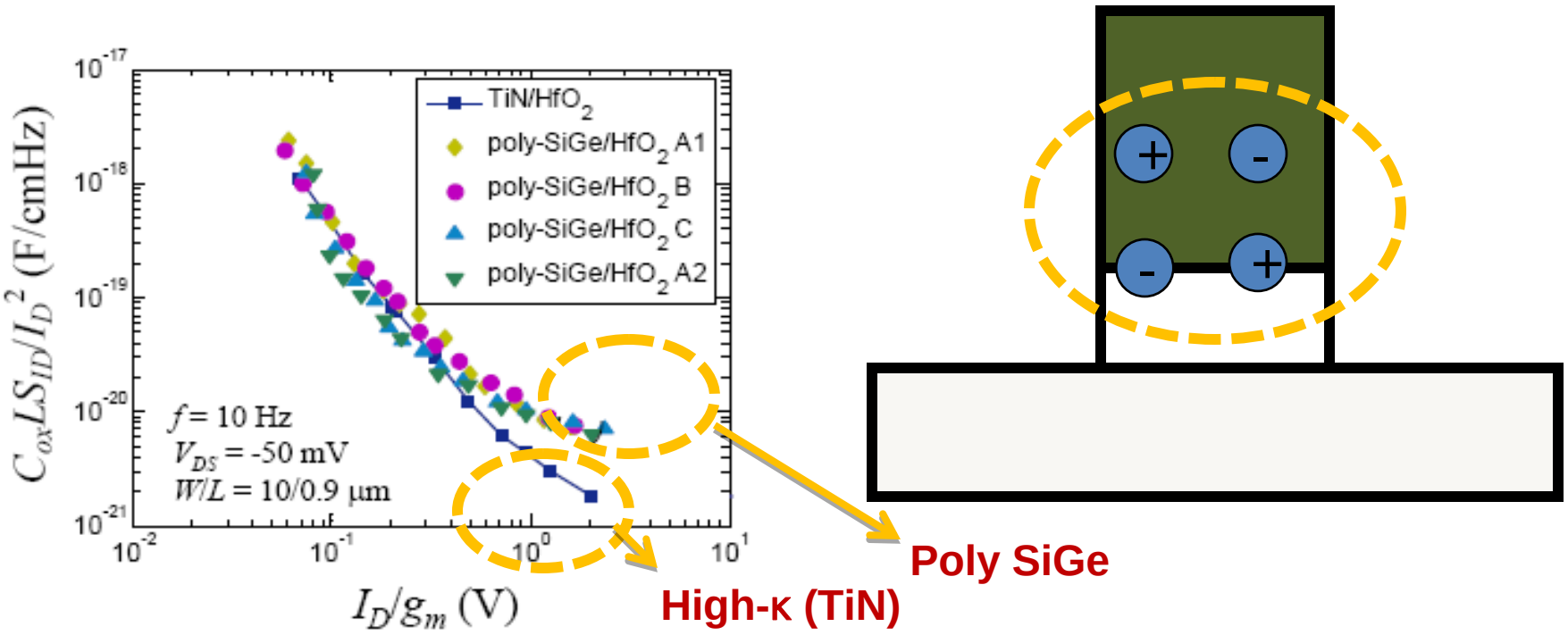



- Halo doping profiles → suppress the short channel effect.
- The same amount of electrons → greater $\Delta I_d$ in halo.
- Reduced inversion carrier density in the halo regions.

[8] Y. Liu et al. *SISPAD 2006*, pp. 99-102, 2006.

# Backup: Metal gate




- The lowering of the 1/f noise: observed in the strong inversion regime.
- Traps and charges at the gate dielectric interface: better screened by a metal gate→alleviate remote phonon scattering.

[15] E. Simoen et al., *IEEE T-ED*, vol.40, pp. 2054-2059, 1993.

# Backup: SiGe FET (1 of 2)

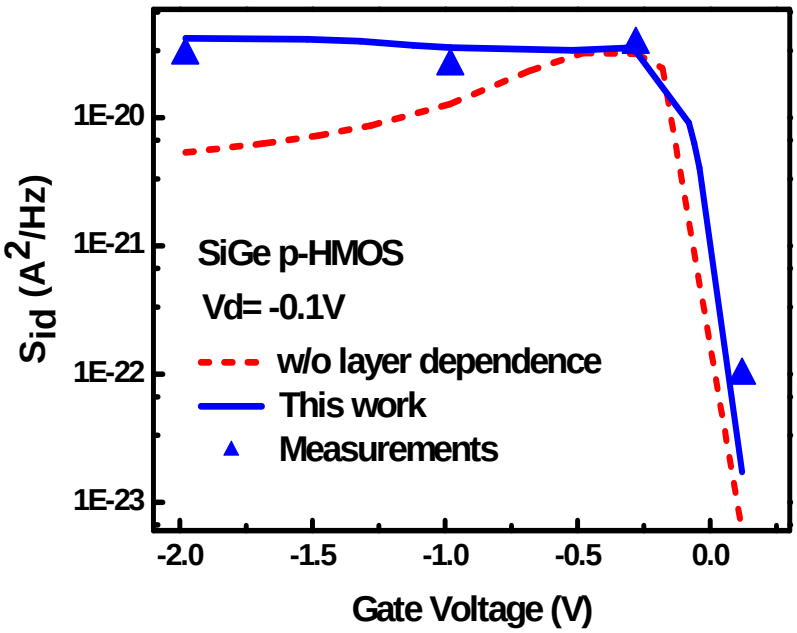
- Dual channel behavior
  - Surface and buried channels have different Coulomb interactions.

$$\eta = (1 + \mu\sqrt{n_{2\text{-D}}}/\mu_{c0})^2$$

$$\eta = (1 + \mu\sqrt{n_{3\text{-D}}}/\mu_{c0})^2$$

  - Both channels also have different material quality.

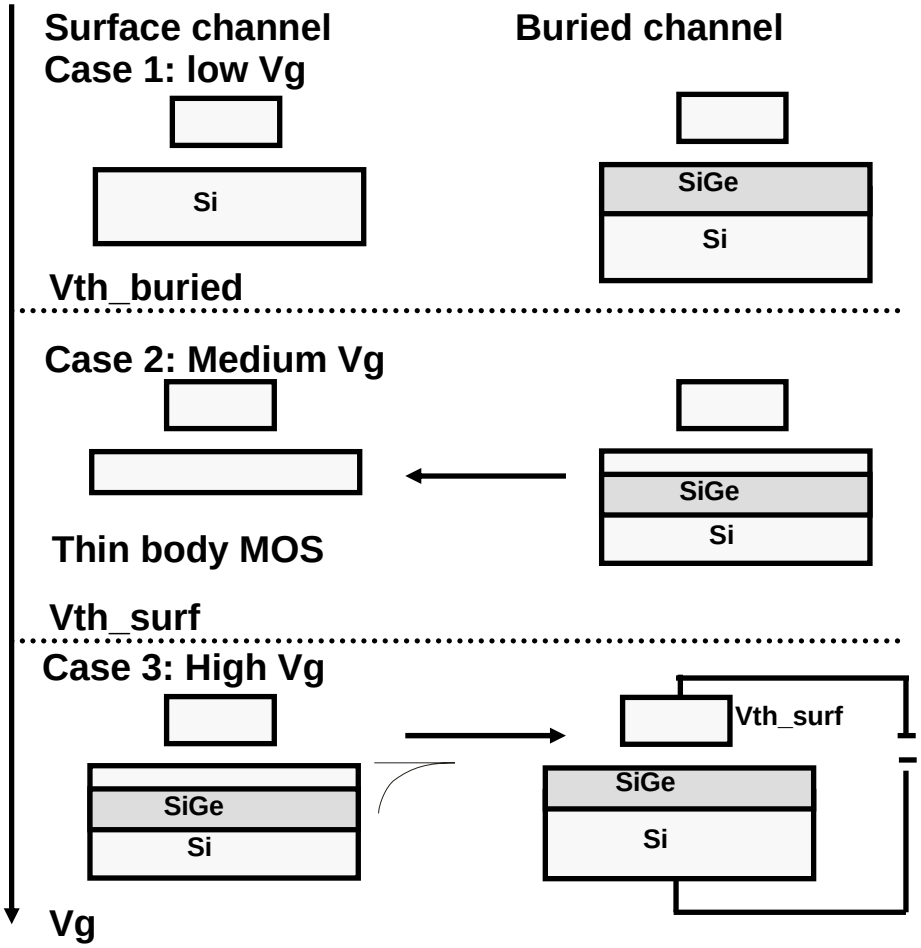
$$\frac{S_{\text{id}}}{I_d^2} = \left( \frac{q\alpha_{\text{cap}}}{WLQ_{\text{cap}}f} \frac{I_{d\,\text{cap}}^2}{I_d^2} + \frac{q\alpha_{\text{SiGe}}}{WLQ_{\text{SiGe}}f} \frac{I_{d\,\text{SiGe}}^2}{I_d^2} \right)$$

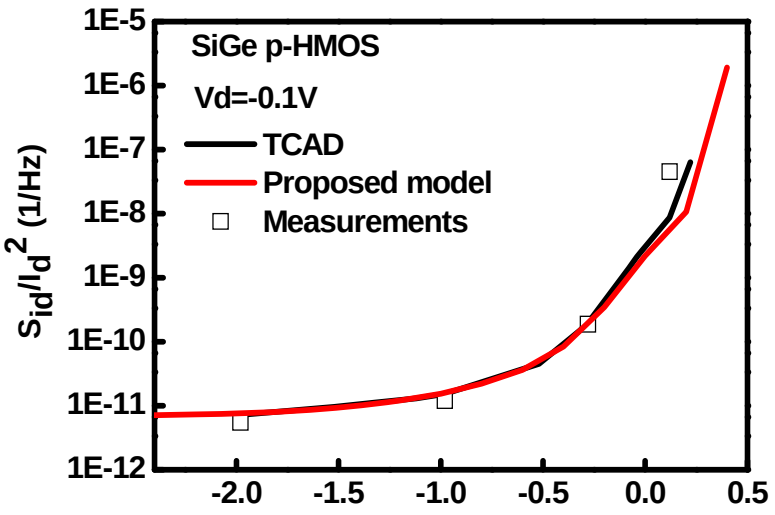


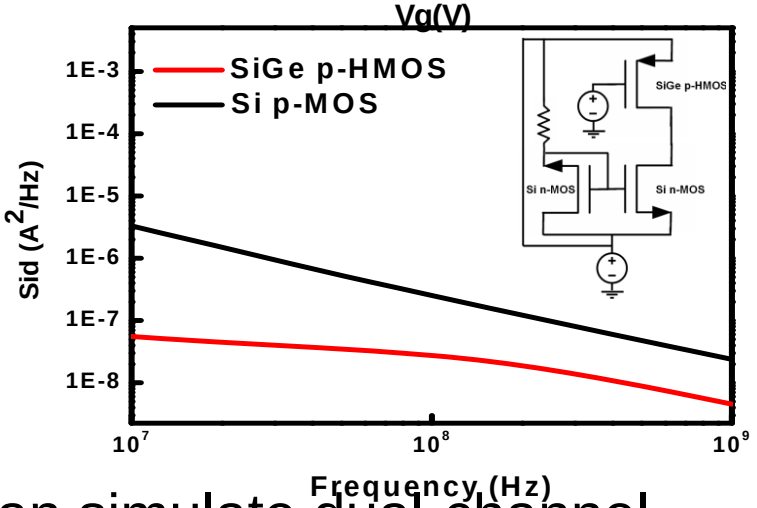

[16] C.-Y. Chen et al., *IEEE T-ED*, vol.55, no.7, pp. 1741-1748, 2008.

# Backup: SiGe FET (2 of 2)

- Compact model



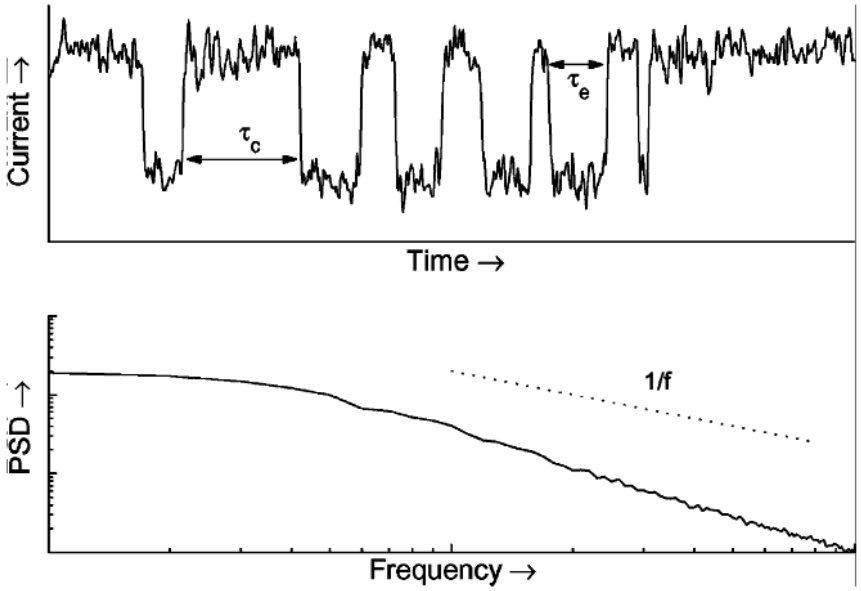



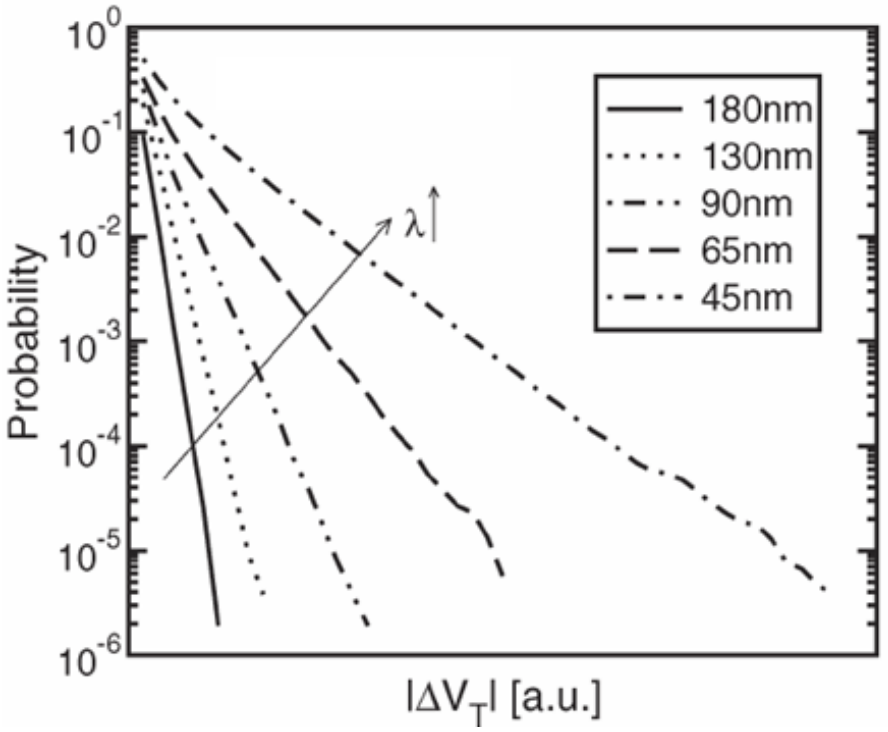




  - Physics based compact model can simulate dual-channel behavior for SiGe FETs.

# Backup: Random Telegraph Noise (1 of 2)

- Exponential tail in RTN



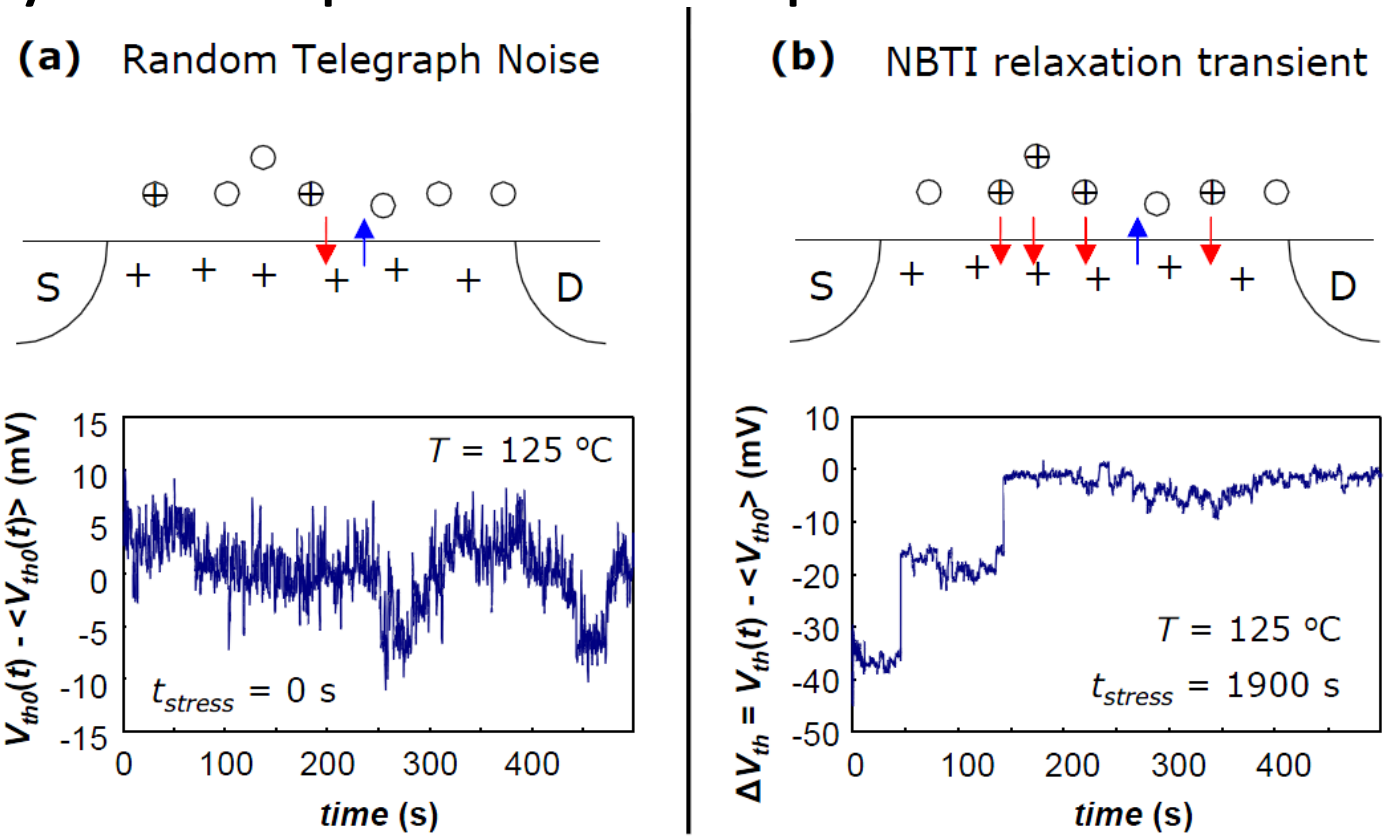




  - The slope of Vth instability shows an exponential tail.
  - The slope increases with technology scaling.

[18] A. Ghetti et al., *IEEE T-ED*, vol.56, no.8, pp. 1746-1752, 2009.

# Backup: Random Telegraph Noise (2 of 2)

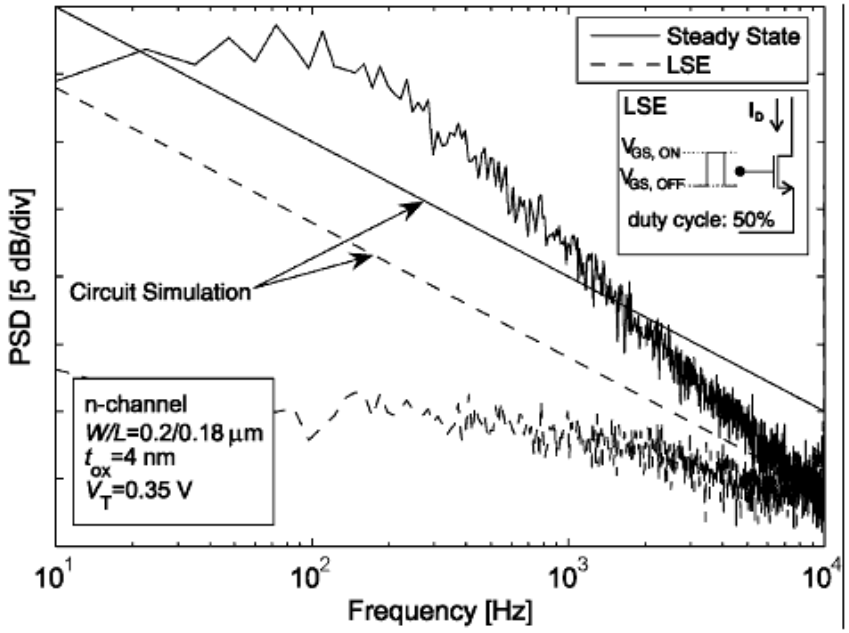
- Body bias dependence: explain

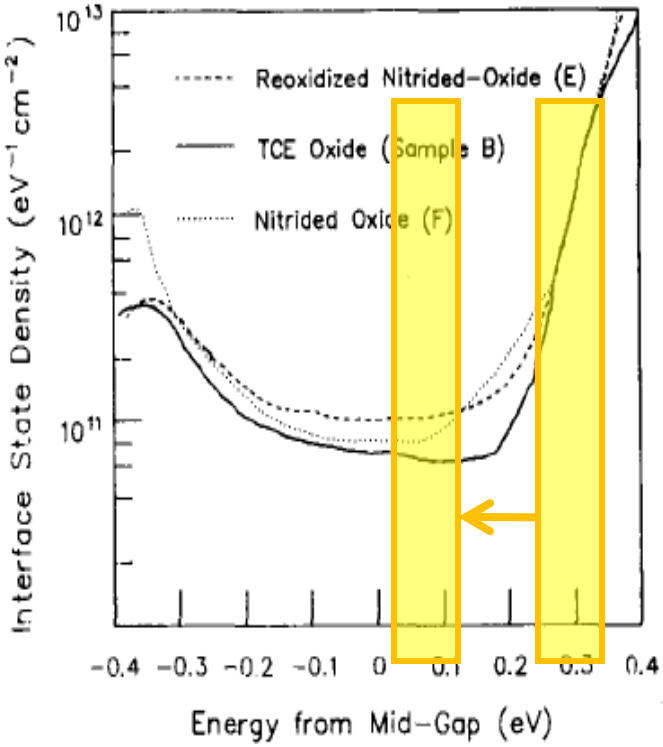



- RTN: channel/gate dielectrics system in dynamic equilibrium.
- NBTI relaxation: perturbed system returning to the equilibrium.

# Backup: Switched bias

- Switched MOS



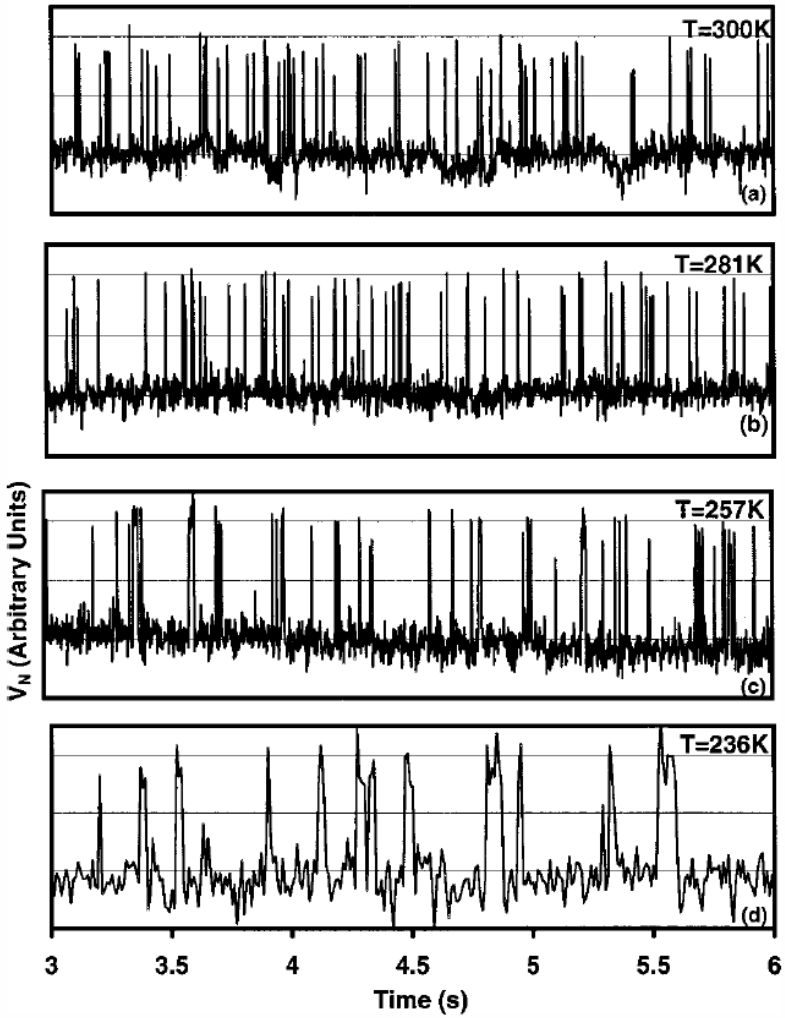




  - Large switch in gate can reduce 1/f noise.

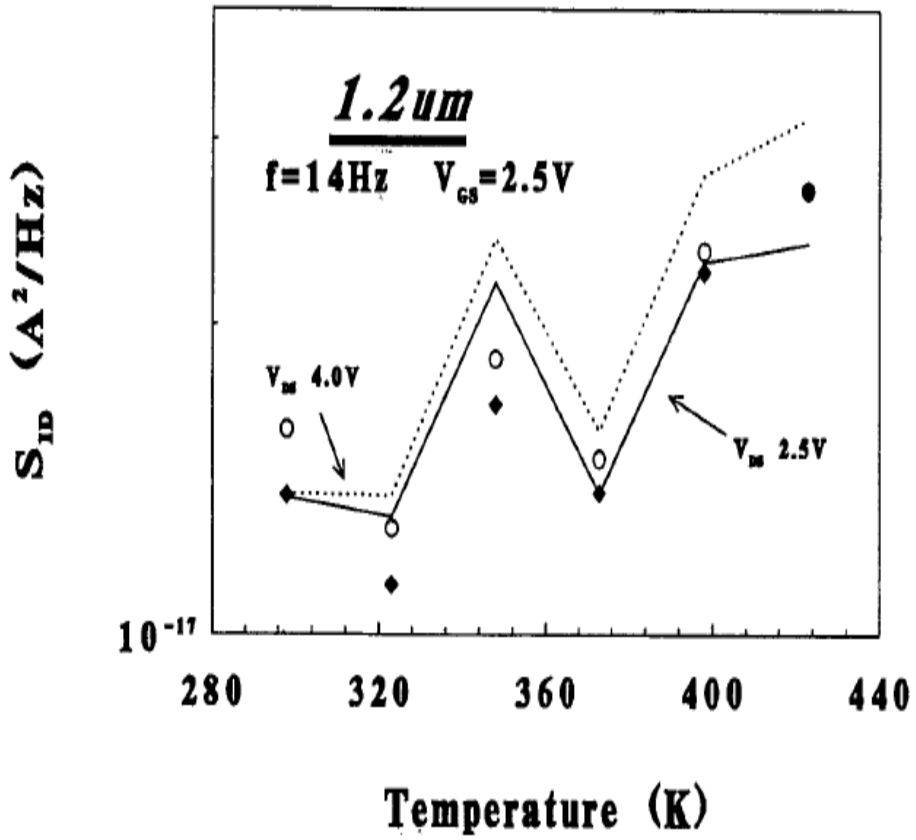
[19] A. P. Wel et al., *IEEE JSSC*, vol.42, no.3, pp. 540-550, 2007.

# Backup: Temperature effect

- RTN



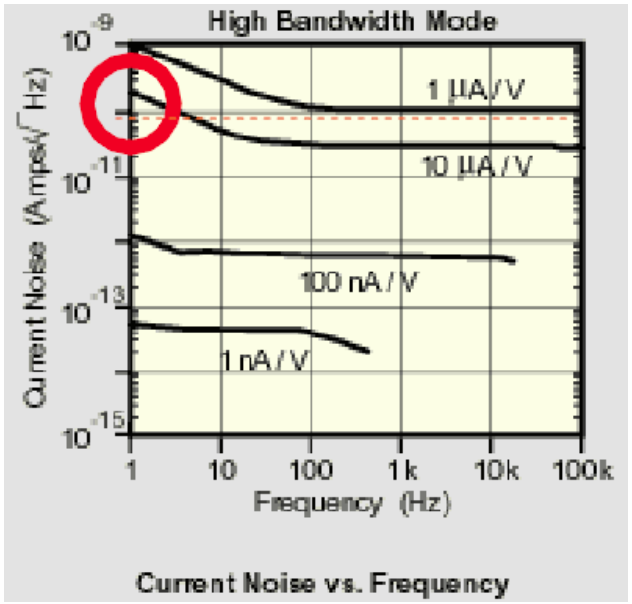

- 1/f noise



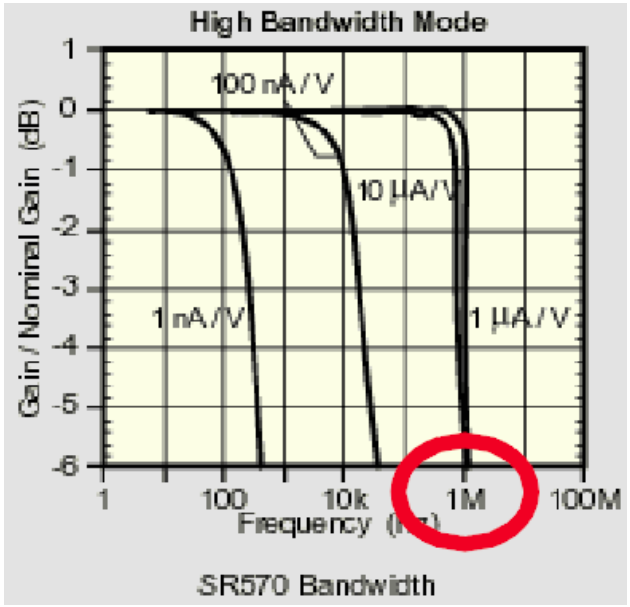

[20] M. J. Deen et al. *AIR conf.* vol. 282, pp. 165-188, 1992.

# Backup: 1/f noise characterization (1 of 4)

- **SR 570 settings**
  - The sensitivity is 2uA/V
  - High bandwidth mode is used.



Current Noise vs. Frequency



SR570 Bandwidth

**Noise floor ~ $10^{-10}$Amps/rootHz**

**Bandwidth ~ 1MHz**

# Backup: 1/f noise characterization (2 of 4)

- **SR 760 settings**

  - Impedance ~ 1MΩ, 15pF
  - Bandwidth: DC to 100kHz
  - The bandwidth of noise measurement is limited by SR760.
  - Good for very low frequency measurements.

# Backup: 1/f noise characterization (3 of 4)

- **HP4396A**

  - Impedance ~ 50Ω.
  - Bandwidth: 2Hz to 1.8GHz
  - Easy interface and high resolution.

- **Active probe HP41800A**

  - Impedance ~ 1MΩ.
  - Bandwidth: 5Hz to 500MHz
  - Convert high impedance to 50 Ω.

# Backup: 1/f noise characterization (4 of 4)

- **On-package measurements**