Solid State Technology and Devices Seminar

Innovations for Continuation of Moore's Law During Next 10 Years

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Abstract: Integrated circuit technologies have had a profound impact on the human society during the last 50 years. An early pioneer of integrated circuit age, Gordon Moore projected in 1965 that the transistor density would double every year, which he later modified to doubling every 2 years. An exponential increase in the transistor density during the last 5-decades has continued unabated. As a consequence, the transistor density for the state-of-the-art logic technology is now ~1-2M transistors/mm^2. The enormity of the challenges in maintaining an exponential growth over a period of 5-decades has led many naysayers to periodically announce the impending demise of Moore's Law. However, despite the enormity, these challenges have been surmounted, thanks to the ingenuity of generations of research and development engineers. With the critical dimensions now scaling to sub-10nm regime, there is again an increasing concern that the transistor density has reached close to a plateau. However, I believe that these concerns are again misplaced. In my talk I plan to present new innovations which will enable transistor density to continue to grow during foreseeable future (~10 years). I will describe Gate-all-Around transistor and subsequently a Vertically-Stacked transistor structure, which will serve as the foundation for improving the density and performance/watt metric in future. An increasing role of on-die interconnects, patterning innovations using EUV and novel packaging technologies will serve as effective solutions to improve density and performance at reasonable cost. Finally, I will highlight the ever increasing role of Design-Technology-Co-Optimization (DTCO) towards achieving density and performance improvement beyond pitch reduction. A combination of new transistors, novel interconnects and packaging, EUV patterning, and next generation DTCO tools is expected to enable continuation of Moore's Law into the future, with density reaching ~1B transistors/mm^2.

Bio: Dr. Tahir Ghani is a Senior Fellow and Director of Process Pathfinding Program at Intel Corporation. He received his PhD in Electrical Engineering from Stanford University in 1994. Since joining Intel in 1994, he has led the teams responsible for developing some of the most significant changes in semiconductor industry and implementing them into mainstream CMOS manufacturing. These include uniaxial strained silicon transistors, HiK+Metal Gate transistors and FinFET transistors. He currently leads Intel's Pathfinding Program with focus on technology definition, evaluation of new process innovations and demonstrating their early viability for technologies beyond 2025. His contributions have been recognized by many awards including IEEE Jun-ichi Nishizawa Medal in 2012. He is a Fellow of the IEEE and was elected to the U.S. National Academy of Engineering in 2015.