BOTS and other FinFET Processes to Enable CMOS Scaling to the 7nm Node

Abstract:

In the BOTS (Bottom-oxidation-through-STI) process, the bottom of a fin on bulk substrate is oxidized to electrically isolate the fin top from the substrate. With this capability to fabricate dielectric-isolated (SOI-like) devices on bulk wafer, we can have conventional bulk devices and SOI-based devices such as eDRAMs on the same chip. Through simulation and experiments, we confirmed that the fin is mechanically-stable and stress-free at end-of-process. In addition, the "fin-tail" in BOTS, which resembles birds beak in LOCOS isolation does not impact FinFET electrostatics as long as there is sufficient gate recess into the dielectric.

In this talk, we will also briefly discuss the fin-last FinFET process, where fin is formed after the source/drain is defined. This facilitates aggressive scaling of fin thickness, down to 4nm. In addition, large embedded SiGe strain can be incorporated in pFETs with the fin-last process.

Strain incorporation is challenging in scaled technology. Uniaxial strain from SiGe substrate for pFETs and SSDOI (Strained-silicon directly on insulator) for nFETs are effective means to incorporate strain in scaled FinFETs.

Bio:

Darsen Lu was one of the key contributors of the industry standard FinFET compact model, BSIM-CMG, and thin-body SOI compact model, BSIM-IMG. He received the B.S. degree in electrical engineering in 2005, from National Tsing Hua University, Hsinchu, Taiwan, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 2007 and 2011. Since 2011, he has been a Research Scientist with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY. His current research focuses on the modeling of novel semiconductor devices and processes such as SiGe FinFETs, phase change memory and carbon-based transistors.