EE 298-12
Solid State Technology and Devices Seminar

Friday, 21 March 2014
1-2pm
540A/B Cory Hall

New Materials and Interface Engineering for Advanced CMOS Devices

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Abstract

The performance of Si-based CMOS ICs has been enhanced over several decades by scaling the transistor size with the Moore's law. The gate length of the transistor has already been scaled down to sub-30 nm. Although Si FinFET device has been developed and show some merits compared with the planar Si MOSFET, the *International Technology Roadmap for Semiconductors*(ITRS) is still expecting new high mobility materials to replace Si as channels in order to enhance the device performance further. Actually, in the mass production technologies, new gate oxides, high permittivity(*k*) gate dielectrics, have been introduced to suppress the unacceptable leakage current of SiO_2 gate oxide with the scaling. No matter in high-*k* gate dielectric engineering or high mobility channel engineering, it is recognized that the MOS interface control technology is of great importance and critical to enhance the device performance. In the early years of my research career, I focused on high-*k* gate oxide and proposed the phase change technology for obtaining higher-*k* and more stable high-*k* lanthanum-based oxides. Recently, my research is mainly about MOS interface properties of strained-Si an Ge MOSFETs. I proposed a universal Coulomb scattering model for strained-Si n and pMOSFETs. This model could also be used to explain the alternated NBTI behaviors in strained-Si pMOSFETs.

Bio

Yi Zhao was born in Zhejiang, China, in 1977. He received the B.S. from Nanjing University of Astronautics and Aeronautics, M.S. from Zhejiang University, and PhD from the University of Tokyo, all in materials science and engineering, in 2000, 2003, and 2007, respectively. His PhD study was focused on Lanthanum based high permittivity (k) gate dielectrics. He is now a Professor of Zhejiang University, Hangzhou, China. From July 2003 to September 2004, he worked at Shanghai HuaHong NEC (HH-NEC), China, as a research and development engineer. At HH-NEC, he was engaged in the research and development on 0.25 μm, 0.18 μm, and 0.13 μm CMOS processes, specially in the wafer level reliability evaluation and test structure design. After finished his PhD study at the University of Tokyo, he stayed at the same university first as a research fellow and then a project assistant professor, where he had been engaged in the research about the physics of strained-Si MOS devices and 32/45nm SRAM devices. After that he worked at Globalfoudnries and IBM International Semiconductor Development Alliance for one year, where he was involved in the research and development of 14/20nm CMOS devices and processes. He joined Nanjing University, China in 2012 and moved to Zhejiang University, China in 2014 as a full professor. His recent research interests mainly are focused on advanced CMOS devices using new channel materials(strained Si/Ge, SiGe, Ge and III-V materials) and new structures (SOI, FinFET, UTB and nanowire).