Advanced MOSFET Structures and Processes for Sub-7nm CMOS Technologies

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The remarkable proliferation of information and communication technology (ICT) – which has had dramatic economic and social impact in our society – has been enabled by the steady advancement of integrated circuit (IC) technology following Moore's Law, which states that the number of components (transistors) on an IC "chip" doubles every two years. Increasing the number of transistors on a chip provides for lower manufacturing cost per component and improved system performance. The virtuous cycle of IC technology advancement (higher transistor density → lower cost / better performance → semiconductor market growth → technology advancement → higher transistor density *etc.*) has been sustained in this way for 50 years. Semiconductor industry experts predict that the pace of increasing transistor density will slow down dramatically in the sub-20 nm (minimum half-pitch) regime. Innovations in transistor design and fabrication processes are needed to address this issue.

The FinFET structure has been widely adopted at the 14/16 nm generation of CMOS technology. Gate-all-around (GAA) FETs are anticipated to be adopted in future generations, to enable ultimate gate-length scaling. This work firstly benchmarks the performance of GAA MOSFETs against that of the FinFETs at 10 nm gate length (anticipated for 4/3 nm CMOS technology). Variability in transistor performance due to systematic and random variations is estimated with the aid of TCAD 3-D device simulations, for both device structures. The yield of six-transistor (6-T) SRAM cells implemented with these advanced MOSFET structures is then investigated via a calibrated physically based compact model. The benefits of GAA MOSFET technology for lowering the minimum operating voltage (V_{min}) and area of a 6-T SRAM to facilitate increased transistor density following Moore's Law are assessed.

In order to achieve similar (or even better) layout area efficiency as a FinFET, a GAA FET must comprise stacked nanowires (NWs), which would add significant fabrication process complexity. This is because stacked NWs are formed by epitaxial growth of relatively thick (>10 nm) Si_xGe_{1-x} sacrificial layers between Si channel layers to accommodate gate-dielectric/gate-metal/gate-dielectric layers in-between the NWs, so that fin structures with very high aspect ratio (>10:1 height:width) must be etched prior to selective removal of the Si_xGe_{1-x} layers. Also, it will be more difficult to implement multiple gate-oxide thicknesses with GAA FET technology for system-on-chip (SoC) applications. In this work, a novel stacked MOSFET design, the inserted-oxide FinFET (iFinFET), is proposed to mitigate these issues. With enhanced performance due to improved electrostatic integrity and minimal added process complexity, iFinFET provides a pathway for future CMOS technology scaling.

Advancements in lithography have been key to sustaining Moore's Law. Due to the low transmittance of blank mask materials and/or the availability of high-intensity light sources for wavelengths shorter than 193 nm, the semiconductor industry has resorted to "multiple-patterning" techniques to increase the density of linear features patterned on a chip. The additional cost due to extra lithography or deposition and etch processes associated with multiple-patterning techniques threaten to bring Moore's Law to an end, stunting the growth of the entire ICT industry. This work proposes an innovative cost-efficient method for achieving sub-lithographic features and/or doubling the density of features, one that is capable of achieving arbitrarily small feature size, self-aligned to pre-existing features on the surface. Thus, it can enable the semiconductor industry to extend the era of Moore's Law, with broad economic and social benefit to society.