

## **Virtual Fabrication: Integrated Process Modeling for Advanced Technology**

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### **Abstract:**

Purely geometric scaling of transistors ended around the 90nm era. Since then, most power/performance and area/cost improvements have come from structural and material innovations. Both logic and memory technologies have moved to advanced 3D structures for performance, density and scalability requirements, such as FinFETs and 3D NAND. This shift towards increased structural complexity will continue in the future. Unfortunately, massive, time-consuming, resource-intensive technology development efforts have been required to bring these advanced technologies into production. Virtual fabrication with Coventor SEMulator3D® can dramatically reduce the time and resources required to develop an integrated process flow for logic and memory applications.

SEMulator3D is a powerful 3D semiconductor process modeling platform that offers wide ranging technology development capabilities. Based on highly efficient physics-driven voxel modeling technology, it has a unique ability to model complete process flows. Starting from input design data, SEMulator3D follows an integrated process flow description to create the virtual equivalent of the complex 3D structures created in the fab. Because the full integrated process sequence is modeled, it has the ability to predict downstream ramifications of process changes that would otherwise require build-and-test cycles in the fab.

In this seminar, Dr. Gu will provide a technical overview of SEMulator3D virtual fabrication platform and discuss its applications in industry and academia.

### **Bio:**

**Jiangjiang (Jimmy) Gu** received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 2012. Before joining Coventor, he was senior process integration engineer at Logic Technology Development group of Intel Corporation, Hillsboro, OR, where he was responsible for the development, yield ramp, and transfer of Intel 22nm tri-gate SOC front-end process technology. He has published over 50 papers in the area of semiconductor process and devices.