EUV Lithography: the Road to HVM and Beyond

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Abstract:
Development of EUV lithography for high-volume manufacturing started in early 2000s. In 2018, 250W of source power became available in the field, giving EUV exposure systems a throughput of >140 wph at an exposure dose of 20 mJ/cm^2. Concurrently, the rate of power degradation due to collector contamination has been driven down so that high system throughput can be maintained. Based on this and progress made in other areas of the technology infrastructure, EUV will enter HVM in 2019 to provide the necessary technology for continued economical scaling of integrated circuits. ASML continues to improve the performance of EUV systems with higher throughput and tighter overlay specifications to further enhance their productivity and capability. At the same time, our phase-inclusive source-mask optimization technique maximizes the lithographic process latitude. For manufacturing with EUV lithography beyond the first generation, issues such as the stochastic behavior of photoresists and the three-dimensional nature of the photomask are being addressed to enable single patterning at lower k_1 values. Overcoming these limitations will allow EUV lithography to extend into the next decade with minimal use of double patterning. Finally, ASML has started to develop the next-generation $NA = 0.55$ EUV exposure tools to enable scaling in semiconductor manufacturing well into the next decade.

Biography:

Anthony (Tony) Yen is VP and Head of ASML's Technology Development Centers. From 2006 to 2017, he was with TSMC where he led the development of EUV lithography for high-volume manufacturing. From 1991 to 1997, as a researcher with Texas Instruments, he worked on techniques to enhance the practical resolution of microlithography. From 1997 to 2003, he was with TSMC where he first led development of lithography processes for TSMC's 0.25, 0.18, 0.15, and 0.13 micron generations of logic integrated circuits and then co-led infrastructure development for next-generation lithography technologies at SEMATECH. From 2003 to 2006 he was with Cymer where he headed its marketing organization. Tony received his BSEE degree from Purdue University and his SM, EE, PhD , and MBA degrees from MIT. He is a fellow of IEEE and SPIE, and a 2018 recipient of Outstanding Electrical and Computer Engineer award from Purdue's School of Electrical and Computer Engineering. He holds over 100 US patents on EUV lithography and related areas.