

Understanding chemical-mechanical planarization: a ubiquitous process in modern IC manufacturing

Hayden Taylor

Chemical–mechanical planarization (CMP) is ubiquitous in the processing of semiconductor wafers, where it is used to achieve flat interfaces between successive layers of circuit structures. As circuit feature sizes reduce, CMP process innovation is constantly needed to maintain acceptable defect rates and throughput. Polishing performance depends in complex ways on the materials being removed, the mechanics and surface topography of the polymeric polishing pad, and the characteristics of the abrasive slurry between the pad and wafer. A particular challenge is to engineer the mechanical properties of the polishing pad so that it can adequately conform to the wafer surface without being overly sensitive to local variations in the characteristics of the circuit pattern being polished.

A key CMP performance metric is *planarization efficiency*, which captures the ability of the process to planarize even when the starting wafer surface is highly heterogeneous or rough. Recently, interest has developed in multi-material polishing pads, which may be structured at the millimeter scale as a way of enhancing die-scale planarization efficiency while maintaining wafer-scale conformation. In this talk, after reviewing some of the current challenges in CMP, I will describe a computational framework for predicting the dependence of planarization efficiency on pad geometry, material properties, asperity topography, and planarized feature size.

Biography:

Hayden Taylor is an Assistant Professor of Mechanical Engineering at the University of California, Berkeley. He holds B.A. and M.Eng. degrees in Electrical and Electronic Engineering from Cambridge University and a Ph.D. in Electrical Engineering and Computer Science from MIT. His research spans the invention, modeling and simulation of manufacturing processes. His group is particularly focused on processes that can be used to fabricate extremely rich and complex, multi-scale geometries, such as are found in semiconductor integrated circuits and biological tissues. Past and current work has addressed deep silicon etching, polymer bonding, chemical mechanical polishing, mechanical exfoliation of van der Waals-bonded solids, and nanoimprint lithography. Current research activities have the following themes: (A) contact mechanics in materials processing, (B) surface engineering for heat and mass transfer, and (C) multi-scale additive manufacturing, including the volumetric process of computed axial lithography.