"Conventional silicon transistor and spintronic based implementation of neural network algorithms in analog hardware"

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Neural Network algorithms, used extensively for classification, recognition and prediction tasks, can be executed at a higher speed and with lower energy consumption if they are implemented on specialized analog crossbar architecture which provides the advantages of parallel computation and memory-embedded computing. In this talk, I shall discuss my ongoing research on analog hardware neural network, using both spintronic devices [1,2] and conventional silicon transistors as synapses [3]. While spintronic synapses can result in extremely low energy [1,2,4,5] consuming neural networks for both on-chip and off-chip learning, conventional transistor based synapses offer the advantage of fabricating analog neural networks much more easily and are mainly meant for on-chip learning [3]. I shall discuss implementation of both non-spiking algorithms, which are widely used by the machine learning community, and spiking algorithms, which are based on biological data about neurons and synapses in the brain, in our proposed hardware systems. In addition, I shall also discuss some Quantum Neural Network algorithms that our group is working on to carry out the same kind of data classification with lower number of weight parameters and hence lesser hardware.

References/ related publications by the speaker:

1. D. Bhowmik,U. Saxena, A. Dankar, A. Verma, D. Kaushik, S. Chatterjee and U. Singh. "On-chip learning for domain wall synapse based Fully Connected Neural Network", Journal of Magnetism and Magnetic Materials 489, 165434 (2019)

2. U. Saxena, D. Kaushik, M. Bansal, U. Sahu and D. Bhowmik. "Low-Energy Implementation of Feed-Forward Neural Network With Back-Propagation Algorithm Using a Spin-Orbit Torque Driven Skyrmionic Device", IEEE Transactions on Magnetics, 44 (11), 2018.

3. U. Saxena, N. Dey, J. Sharda, D. Kaushik, A. Dankar, A. Verma, R. Sharma and D. Bhowmik, "On chip learning in a conventional silicon MOSFET based Analog Hardware Neural Network", to be presented at International Conference on Neuromorphic Systems (ICONS), Knoxville TN, 2019 (archive version of the full paper: N. Dey et al. arxiv:1907.00625)

4. D. Bhowmik, M Nowakowski, L You, OJ Lee, D Keating, M Wong, J Bokor and S. Salahuddin, "Deterministic Domain Wall Motion Orthogonal To Current Flow Due To Spin Orbit Torque", Scientific Reports 5, 11823 (2015)

5. D. Bhowmik, L. You and S. Salahuddin, "Spin Hall effect clocking of nanomagnetic logic without a magnetic field", Nature Nanotechnology, 9, 59-63 (2014)

Biography:

Debanjan Bhowmik is currently an Assistant Professor in Department of Electrical Engineering, Indian Institute of Technology Delhi. He obtained B.Tech. degree in Electrical Engineering from Indian Institute of Technology Kharagpur in 2010 and PhD degree from University of California Berkeley in 2015. His doctoral thesis was in the field of nano-magnetism and spintronics.