A Framework for Information Processing:
Computing Beyond Moore's Law

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The computer revolution, rolling past its fifty-year march as one of the most significant advancements of human civilization, has been enabled by a confluence of breakthroughs in science and engineering. This revolution known by the moniker Moore's Law has evidently slowed leading to the question of how computing of the future will evolve. With this as the backdrop, we present the rationale for and describe an adaptable and scalable framework ("Co-design Version 3.0"), which can be used to configure, and "personalize" computing driven by the specific needs of applications. We will examine 6 different scaling paradigms that are driving this need for a change in thinking: combinatorial nature of scientific problems, multi-scale nature of systems, algorithms, complexity of applications, Moore's law, and economics of scaling.

To realize this vision in a cost-effective way, this should be done in a scalable manner to help in wider dispersion of the benefits of computing rather than to niche scientific communities. We think that both research and development in natural, computational, and mathematical sciences along with centers of computational and physical sciences need to be formally engaged. In addition, the co-design should also address manufacturing of complex materials and devices. As part of this talk, we will also briefly illustrate a new class that we have developed in which students are taught hands-on about using extreme computing to address real applications. With a focus on real applications, we anticipate co-design will shift the way computing is evaluated and enable many possibilities in applying computing to solve societal problems.

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Sadasivan (Sadas) Shankar is an Associate in Applied Physics, with the Paulson School of Engineering and Applied Sciences in Harvard University. He was the first Margaret and Will Hearst Visiting Lecturer in Computational Science and Engineering at Harvard, where he was involved in teaching and research in the areas of large-scale computational methods, chemistry, and materials. In fall 2013, as the first Distinguished Scientist in Residence at the Institute of Applied Computational Sciences in Harvard, he co-instructed a graduate-level class on *Computational Materials Design*, which covered fundamental atomic and quantum techniques and practical applications for new materials by design. He also co-developed and co-instructed classes on *Extreme Computing for Real Applications* and *Mitigating Toxicity by Materials Design*.

Dr. Shankar and his team have enabled several critical technology decisions in Intel in materials, processing, packaging, manufacturing, and design rules for over nine generations of Moore's law in semiconductor technology: First advanced process control application in Intel; introduction of flip-chip packaging; optimization of laser annealing process; design, integration, and packaging of low dielectric constant materials; optimization of planarization, chemical vapor deposition, plasma etching, and epoxy underfill process; 100% Pb-elimination in 45 nm technology; 3D packaging thermal analysis; design guidelines for co-optimizing microprocessor design with materials, processing, and packaging.

Dr. Shankar has been also involved in several collaborative national and international efforts with Semiconductor Research Corporation, SEMATECH, and Semiconductor Industry Association in laying out roadmaps for *Process Equipment, Emerging Research on Materials and initiating research efforts on Nanomaterials.* In addition, he has worked with National Institute of Standards and Technology, and Department of Energy for highlighting needs for materials research. He has also provided inputs to the Chemical Industry R&D Roadmap for Nanomaterials by Design (2006), Integrated Computational Materials and Engineering (2009), President's Materials Genome Initiative (2011), NASA Vision 2040 for Computational Design of Materials (2016).

Dr. Shankar earned his Ph.D. in Chemical Engineering and Materials Science from University of Minnesota, Minneapolis. He is a co-inventor in over 20 patent filings covering areas in new chemical reactor designs, semiconductor processes, bulk and nano materials, device structures, and algorithms. He is also a co-author in over 100 publications and presentations in multi-scale and multi-physics methods spanning from quantum scale to macroscopic scales, in the areas of chemical synthesis, plasma chemistry and processing, non-equilibrium electronic, ionic, and atomic transport, energy efficiency of information processing, and machine learning methods for bridging across scales. Dr. Shankar has also been a Senior Fellow in UCLA Institute of Pure and Applied Mathematics (2016), Invited to White House event for Materials Genome (2012), Visiting Lecturer in Kavli Institute of Theoretical Physics in UC-SB (2010), Intel Distinguished Lecturer in Caltech (1998) and in MIT (1999). He has also given several colloquia and lectures in Caltech, Cambridge U, Cornell, Harvard, Stanford, MIT, Northwestern, Purdue, Lawrence Livermore National Labs, Institute of Science-Bangalore, Oakridge National Lab, UNC, UC-Berkeley, UCLA, UC-Santa Barbara, U of Florida, USC, UT-Austin, U of Vienna, Tata Institute of Fundamental Research-Mumbai. His team's work was also featured in the journal *Science* (March 2012) and in *TED* (March 2013). Dr. Shankar piloted a research lab in collaboration with VNIIEF-Russia on Physical Modeling that became part of Intel Corporation.