Solid State Technology and Devices Seminar

Low Thermal Budget Trends for Interconnect RDL Polyimides For 3D Advanced IC Backend Applications

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Abstract: In the ongoing effort to extend and move beyond Moore's Law, advances in backend IC processing are extending the capabilities of heterogeneous and 3D integration. 3D stack memory has already fueled considerable progress in 3D integration, enabling high-bandwidth memory (HBM) and dynamic random-access memory (DRAM). In addition to the 3D stacking ofmemory, 3D system integration allows a variety of chiplets and other components to bestacked, delivering high compute density and high performance at low cost. Multi-layer RDLs(Redistribution layers) are used to connect these dissimilar chips on organic, glass, silicon or fan-out substrates. The need to transition to all-Cu interconnect as well as to manage fan-out stress has resulted in a temperature limit of 250°C for large numbers of these products. Consequently, process technology for Polyimide, Photo Imageable Dielectric (PID) and Photo Sensitive Polyimide (PSPI) must now enable a faster cure at lower temperatures resulting in lower thermal budget, while also delivering better film properties. In this seminar, the physical, mechanical, thermal, and electrical properties of different types of Polyimide and Poly-Benz-Oxazole (PBO) materials, were studied as a function of different process parameters, under atmospheric and vacuum process conditions. Vacuum cure even in lower temperatures resulted in higher thermal stability, lower outgassing, and better thermal properties. In electrical characterization, vacuum cure showed better dielectric strength as well as lower dissipation factor. These results are consistent with the assumption that cure under vacuum reduces the amount of volatile and volatilizable material remaining in the film after the cure process. The use of sub-atmospheric curing or annealing technology at low temperature improved both the quality and the performance of the cured polyimide films for RDL applications that are relevant to the multi-level metallization process of Fan Out Wafer Level Packaging (FOWLP) and Fan Out Panel Level Packaging (FOPLP), and therefore to 3D stack integration.

Bio: Zia Karim is currently Sr. Vice President and Chief Marketing Officer (CMO) at Yield Engineering Systems, a leading Semiconductor Equipment Company for Backend Advanced IC Packaging Processes. Dr. Karim most recently was Vice President of Business Development and Technology at AIXTRON/Genus (acquisitions) where he worked for over 15 years. Dr. Karim has held senior management positions in Applied Materials, and Novellus (acquired by LAM Research) after he started his career in Sharp Microelectronics in 1994. Dr. Karim recently completed Certificate of Business Excellence in Executive Education from UC Berkeley Hass School of Business. Dr. Karim received Ph.D, in Electronic Engineering from Dublin City University in Ireland, and B.Sc and M.Sc degree from Bangladesh University of Engineering and Technology in Electrical and Electronic Engineering. Dr. Karim took a pioneering role in positioning W/WSi CVD, Low k PECVD, High K ALD, and III-V MOCVD process in Semiconductor Logic and Memory Devices. Dr. Karim owns sixteen (16) patents. Other than organizing or co-organizing several

Conferences, Symposiums and related Transactions, Dr. Karim also authored more than forty (40) published papers.