FinFET 3D Transistor & the Concept Behind It

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• Intel will use 3D FinFET at 22nm
• Most radical change in decades
• There is a competing SOI technology
New MOSFET Structures

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Good Old MOSFET Nearing Limits

- Vt, S, Ioff are bad & sensitive to Lg
- Dopant fluctuations.

Requiring
- higher Vt, Vdd, and power consumption
- higher design cost

Finally painful enough for change.

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MOSFET becomes “resistor” at very small L – Drain competes with Gate to control the channel barrier.
Making Oxide Thin is Not Enough

Gate cannot control the leakage current paths that are far from the gate.

C.Hu,”Modern Semicon. Devices for ICs” 2010, Pearson
One Way to Eliminate Si far from Gate

A thin body controlled by gate from more than one side.

FinFET body is a thin fin

N. Lindert et al., DRC paper II.A.6, 2001
FinFET - 1999

Undoped Body. 30nm etched thin fin. Vt set with gate work-function.

X. Huang et al., IEDM, p. 67, 1999
FinFET is “Easy” to Scale

Leakage is well suppressed if \( \text{Fin thickness} \leq L_g \)

- Thin fin and gate can be made with the same lithography and etching tools.
Body thickness is the new scaling parameter.

C.Hu,”Modern Semicon. Devices for ICs” 2010, Pearson
Two Improvements to FinFET

Original FinFET had thick oxide on fin top & used SOI for process simplicity.

• 2002 FinFET with thin oxide on fin top. F.L.Yang et al. (TSMC) 2002 IEDM, p. 225.

• 2003 FinFET on bulk substrate. T. Park et al. (Samsung) 2003 VLSI Symp. p. 135.
State-of-the-Art FinFET

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20nm Hi Perf
C.C. Wu et al.,
2010 IEDM
2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI) →
No leakage path far from the gate.


Drain Current [A/μm]

Gate Voltage [V]

T_{si}=8nm
T_{si}=6nm
T_{si}=4nm

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Most Leakage Flows >5nm Below Surface

Silicon Body Needs to be \(<Lg/3\)

For good swing and device variation


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UTB-SOI
3nm Silicon Body, Raised S/D


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State-of-the-Art 5nm Thin-Body SOI

ETSOI, IBM
K. Cheng et al, IEDM, 2009
Both Thin-Body Transistors Provide

- Better swing.
- S & Vt less sensitive to Lg and Vd.
- No random dopant fluctuation.
- No impurity scattering.
- Less surface scattering (lower E_{eff}).

\[ \Downarrow \]

- Higher on-current and lower leakage
- Lower V_{dd} and power consumption
- Further scaling and lower cost
Similarities between FinFET & UTBSOI

Device Physics

- Superior S, scalability and device variations
- use body thickness as a new scaling parameter
- can use undoped body for high $\mu$ and no RDF

History

- 1996: UC Berkeley proposed both to DARPA as “25nm Transistors”.
- 1999: demonstrated FinFET
- 2000: demonstrated UTB-SOI
- Since 2001: ITRS highlights FinFET and UTBSOI

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Main Differences

- **FinFET** body thickness \( \sim L_g \). Investment by fab.
- **UTBSOI** thickness \( \sim 1/3 L_g \). Investment by Soitec.
- **FinFET** has clearer long term scalability. **UTBSOI** may be ready sooner than FinFET for some companies.
- **FinFET** has larger \( I_{on} \).
- **UTBSOI** has a good back-gate bias option.

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What May Happen

• **FinFET** will be used at 22nm by Intel and later by more firms to <10nm.

• Some firms may use **UTBSOI** to gain market from regular CMOS at 20/18/16nm.

If so, competition between **FinFET** and **UTBSOI** will bring out the best of both.
**Berkeley Short-channel IGFET Model**

- 1997: became first *industry standard* MOSFET model for IC simulation
- BSIM3, BSIM4, BSIM-SOI used by hundreds of companies for design of ICs worth half trillion dollars
- BSIM models of FinFET and UTBSOI are available – free 😊
Global fitting with 30nm-10um FinFETs
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Temperature Model Verified for FinFET

-50°C --> 200°C in steps of 50°C

$V_{gs}$ (V)

Drain Current (μA)

$L_G = 60\text{nm}
20\text{ fins}$

$V_{gs}$ (V)

Drain Current (A)
Summary

• FinFET and UTB-SOI allows lower $V_t$ and $V_{dd}$ $\rightarrow$ Lower power.

• Body thickness is a new scaling parameter $\rightarrow$ Better short channel effects to and beyond 10nm.

• Undoped body $\rightarrow$ Better mobility and random dopant fluctuation.

• BSIM models of FinFET and UTBSOI are available – free 😊