Research of Germanium on Insulator

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Institute of Microelectronics  
Peking University, Beijing, China

ULKI      SOC     MEMS

Professors : 49
Undergraduate students : 60~80/year
Graduate students : 40~55/year

Wang Yangyuan
Professor and Director of
Institute of Microelectronics
National Key Micrometer/Nanometer Processing Lab

- Over 10-million USD process and analyzing equipment in a 900m² clean room.
- CMOS, Bipolar, especially MEMS baseline process.
OUTLINE

Part I  State of the art on GeOI
• An introduction to GeOI
• Main approaches for GeOI fabrication

Part II  Our research about GeOI
• Bulk and Epi Ge wafer are transferred on substrate
• A new method was presented to extract mobility
• Mobility and interface trap density are improved
Part I State of the art on GeOI

- An introduction to GeOI

**What is GeOI?**  GeOI = “Ge”+ “OI”
Why GeOI?

Advantages of “Ge”
- Significantly higher bulk electron and hole mobilities
- Higher thermal injection velocity
- Lower Schottky barrier due to smaller Ge band-gap
- Allowing a smaller $V_{DD}$

Advantages of “on-Insulator”
- Partially overcoming the high leakage current
- Potential substrate for FinFET structures
Texas Instruments' first IC made by Jack Kilby in 1958

The first transistor was invented in 1947 by William Shockley, John Bardeen and Walter Brattain.

The first transistor and IC are all made of Germanium
The Myth: Si is the newer technology

Identified by Lavoisier in 1787

<table>
<thead>
<tr>
<th>B</th>
<th>C</th>
<th>N</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>Si</td>
<td>P</td>
</tr>
<tr>
<td>Ga</td>
<td>Ge</td>
<td>As</td>
</tr>
<tr>
<td>In</td>
<td>Sn</td>
<td>Sb</td>
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</table>

Identified in 1886

In 1886, Coca Cola was invented

It’s the real thing. Coke.

It’s the real thing. Germanium.
Part I State of the art on GeOI

- An introduction to GeOI
- **Main approaches for GeOI fabrication**
  - Ge condensation method
  - Rapid Melt Growth
  - Mechanical and Thermal Ion-Cut
Ge condensation method

(This method is first presented by S. Nakaharai, MIRAI-ASET, Japan)

- Ge condensation technique: (a) Commercial SOI wafer, (b) SiGe layer is grown epitaxially on an SOI wafer, (c) Oxidation of SGOI, (d) Complete Ge condensation and (e) GeOI wafer after removing surface oxide.
Rapid Melt Growth (RMG)

(a) Seed windows are etched
(b) Ge is deposited by CVD
(c) Ge film is patterned into stripes
(d) Ge stripes is covered by LTO

TEM image of GeOI obtained by RMG

Y.Liu et al., Stanford University

Feb.29th, 2008
Mechanical and Thermal Ion-Cut

(a) H+ implantation to Ge (dose:6x10^{16}/cm^2);
   i) LPCVD Si_3N_4 on Si
   ii) Thermal SiO_2 on Si

(b) Oxygen plasma activation for 15sec

(c) Ramp anneal at 200~250°C

A 200mm GeOI formed by thermal-cut method (Soitec, France)

Seminar
GeOI device

P-Channel Germanium FinFET Based on RMG
Jia Feng, et al. (Stanford University), EDL, 2007

First Deep Sub-Micron GeOI PMOSFET
A. Pouydebasque, et al.
(CEA-LETI MINATEC, FRANCE)

Feb. 29th, 2008
Advantages of ion-cut method

- Wafer-scale transfer for all wafer sizes
- Layout Pattern independent
- High quality GeOI decided by bulk Ge or Epi-Ge
- An extension of mature SOI technology
Part II  Our research about GeOI

• Bulk and Epi Ge wafers were transferred
• A new method was presented to extract mobility
• Mobility and interface trap density are improved
Large-area GeOI formed by layer transfer processing

Fabrication processes:
(1) HF/DIW surface cleaning (pre-bonding cleaning); (2) N₂ plasma activation;
(3) Direct bonding; (4) Post-bonding annealing at 220 °C; (5) Mechanical-cut or thermal-cut at T>270 °C;
The pillow defects of GeOI annealed at various temperatures. No Ge wafer surface cleaning is performed before wafer bonding. The origin of pillow defects is usually attributed to contamination on the Germanium wafer surface such as hydrocarbons.
Layer Transfer Process Improvement

(A) GeOI sample after 540°C anneal for 90 min without pre-bonding cleaning

(B) GeOI sample after 540°C anneal for 90 min with pre-bonding cleaning
Bonding energy of Ge with (I) SiO$_2$/Si, O$_2$ plasma surface activation; (II) Si$_3$N$_4$/Si, O$_2$ plasma surface activation; (III) SiO$_2$/Si, N$_2$ plasma surface activation.
GeOI surface smoothing with CMP

- GeOI surface can be smoothed down to RMS = 0.3nm by CMP (CMP slurry: 0.2µm SiO2 particle mixed with KOH)
- GeOI substrates are ready for device fabrication
The GeOI surface smoothing by CMP

(a) as-cut GeOI

RMS: 0.3 nm; Ra: 0.23 nm
Z-range: 3 nm

(b) after CMP and HF dip

RMS: 11.8 nm; Ra: 9.5 nm
Z-range: 87.8 nm
300mm Ge wafers (UMICORE)
Surface steps of Epi-Ge wafer

AFM image of a Epi-Ge surface
Large area Epi-Ge is transferred

3 days furnace annealing    7 days furnace annealing

Temperature increases slowly from 120 °C to 300 °C

Feb. 29th, 2008
Part II Our research about GeOI

- Bulk and Epi Ge wafer are transferred on substrate
- A new method was presented to extract mobility
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Pseudo MOSFET Measurement (4-probe configuration)

- Rapid electrical evaluation of semiconductor-on-insulator substrate
- Extracting interface carrier mobility of GeOI
The pseudo-MOSFET experimental data

\[ G = \frac{|I_{1,4}|}{V_{2,3}} (\Omega^{-1}) \]

\[ V_{FB} = -10.2 \text{V} \]

\[ V_T = 6.8 \text{V} \]

G vs VG plot, which shows the accumulation, depletion and inversion regions. In depletion mode, the bulk Ge mobility is extracted by fitting theoretical data with experimental data, which is 143.8 cm\(^2\)/V-sec.
In inversion mode, Channel conductance $G_{ch}$ is given by:

$$G_{ch} = f_g \mu_n^0 C_{ox} (V_G - V_T) / [1 + \theta (V_G - V_T)]$$
Differentiating $G_{ch}$, we obtain:

$$G'_{ch} = \frac{dG_{ch}}{dV_G} = \frac{f_g \mu_n C_{ox}}{[1 + \theta(V_G - V_T)]^2}$$

$$\frac{G_{ch}}{G'_{ch}^{0.5}} = \left(f_g \mu_n C_{ox}\right)^{0.5} (V_G - V_T)$$
The extraction of the threshold voltage $V_T$; The low field electron mobility at interface was extracted from the slope of the fit lines, which is 87.3 cm$^2$/V-sec.
In accumulation mode:

\[
G'_{ch} = \frac{dG_{ch}}{dV_G} = \frac{f_g \mu p_0 C_{ox}}{[1 + \theta'(V_G - V_{FB})]^2}
\]

\[
\frac{G_{ch}}{G'_{ch}} = \left( f_g \mu p_0 C_{ox} \right)^{0.5} (V_G - V_{FB})
\]
The extraction of the flatband voltage $V_{FB}$; The low field hole mobility at interface was extracted from the slope of the fit lines, which is $117.5\text{cm}^2/\text{V-sec}$. 

Accumulation mode

$\mu_{p0} = 117.5\text{cm}^2/\text{V-sec}$

$V_{FB} = -10.2\text{V}$

Slope = $(f_{g}\mu_{p0}C_{ox})^{0.5}$
The pseudo-MOSFET experimental data

G vs VG plot, which shows the accumulation, depletion and inversion regions. In depletion mode, the bulk Ge mobility is extracted by fitting theoretical data with experimental data, which is 143.8 cm²/V·sec.

G = \frac{I_{1,4}}{V_{2,3}^2} (\Omega^{-1})
I-V of intrinsic point-probe MOSFET in partially depleted GeOI

$I_{1,4} = I_{\text{bulk}} + I_{\text{interface}}$

$V_G$

$W_d (0 \sim W_{d_{\text{max}}})$

$V_G$

$400 \text{nm OX}$

$V_{2,3}$

$I_{\text{bulk}}$

$I_{\text{interface}}$

$t_{\text{Ge}}$
I_{1,4} is given by:

$$I_{1,4} = I_{bulk} + I_{interface}$$

In depletion mode:

$$I_{bulk} \gg I_{interface}$$

$$I_{1,4} = I_{bulk} + I_{interface} = I_{bulk} = f_g q \mu_p (t_{Ge} - w_d) N_{Ge} V_{2,3}$$
\[ G = \frac{I_{1,4}}{V_{2,3}} = f_g q \mu_p \left( t_{Ge} - W_d \right) N_{Ge} \]

\[ W_d = \sqrt{\frac{2\varepsilon_s}{qN_{Ge}}} \psi = \sqrt{\frac{2\varepsilon_s}{qN_{Ge}}} \left( V_G - V_{FB} - V_{ox} \right) \]
\[(A - G)^2 = BV_G + C\]

\[A = f_g q \mu_p N_{Ge} \left( t_{Ge} + \varepsilon_s / C_{ox} \right)\]

\[B = 2q \left( f_g \mu_p \right)^2 \varepsilon_s N_{Ge}\]

\[C = \left( f_g q \mu_p N_{Ge} \right)^2 \left[ \left( \varepsilon_s / C_{ox} \right)^2 - \frac{2\varepsilon_s V_{FB}}{qN_{Ge}} \right]\]
The pseudo-MOSFET experimental data

\[ G = \frac{I_{1,4}}{V_{2,3}} (\Omega^{-1}) \]

G vs VG plot, which shows the accumulation, depletion and inversion regions. In depletion mode, the bulk Ge mobility is extracted by fitting theoretical data with experimental data, which is 143.8 cm²/V·sec.
The extraction of interface fixed charge density, $Q_f$

$$V_{FB} = \Phi_{Ge-Si} - \frac{Q_f}{C_{ox}}$$

The extracted $V_{FB}$ by pseudo-MOSFET is used to obtain $Q_f$

The extraction of interface trap density, $Q_{it}$

Hysteresis behavior is observed when $V_G$ is swept along opposite directions. This is attributed to the interface traps between Ge and the buried oxide. The shift of $V_T$ is used to obtain interface trap density $Q_{it}$.
## Current GeOI Summary

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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<tbody>
<tr>
<td>Interface fixed charge density, $Q_f$</td>
<td>$\sim 10^{11}q/cm^2$</td>
</tr>
<tr>
<td>Interface trap density, $Q_{it}$</td>
<td>$\sim 10^{11}q/cm^2$</td>
</tr>
<tr>
<td>Interface hole mobility, $\mu_{p0}$</td>
<td>117.5 cm$^2$/V-sec</td>
</tr>
<tr>
<td>Interface electron mobility, $\mu_{n0}$</td>
<td>87.3 cm$^2$/V-sec</td>
</tr>
<tr>
<td>Bulk hole mobility, $\mu_p$</td>
<td>143.8 cm$^2$/V-sec</td>
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Part II Our research about GeOI

- Bulk and Epi Ge wafer are transferred on substrate
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The condition of forming gas annealing

- Gas ratio: 10%\(H_2\), 90%\(N_2\)
- Gas flow: 8L/min
- Temperature: 400 °C ~ 600 °C
- Time: 10min or 30min at each temperature point
Interface trap ($Q_{it}$) and Interface charge ($Q_f$) improved through forming gas annealing

- Both interface trap density $Q_{it}$ and interface fixed charge density $Q_f$ decrease to $10^{10} \text{q/cm}^2$ after forming gas annealing.
Carrier mobility improved through forming gas annealing

(A) • 3X improvement of bulk hole mobility with fast ramp
• 3X improvement of interface hole mobility with fast ramp
• 2X improvement of interface electron mobility with slow ramp

(B)
In Progress

- Prototype GeOI MOSFET performance with ALD high-K dielectric (with Prof. J. Chang, UCLA)
- Demonstrate Strained GeOI layer transfer
Conclusion

- GeOI is a potential next-generation substrate
- A new pseudo-MOSFET methodology is presented to extract bulk mobility of GeOI
- Mobility and Interface trap is improved by forming gas annealing
Thanks!