Amorphous silicon thin-film transistors for flexible electronics

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Flexible displays

Lucent, E-Ink

http://www.eink.com/iim/sale.html
Transistor “backplane” and display “frontplane”

Schematic cross section of a display

Amorphous silicon thin film transistor generic backplane

- TFT backplane is generic for all flat panel technologies
- Add display layer on top

Outline

- Metal versus plastic foil substrate
- a-Si:H TFT deposition temperature
- Overlay alignment
Steel versus plastic

<table>
<thead>
<tr>
<th>Property</th>
<th>Polymer Foil</th>
<th>Steel Foil</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process temperature</td>
<td>up to ~1000°C</td>
<td>low</td>
</tr>
<tr>
<td>Dimensional stability</td>
<td>&gt; 10 times higher</td>
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</tr>
<tr>
<td>Visually clear</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Permeable to O₂ or H₂O</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Surface roughness</td>
<td>rough</td>
<td>moderate</td>
</tr>
<tr>
<td>Inert to chemicals</td>
<td>yes</td>
<td>some</td>
</tr>
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<td>Electrical conductor</td>
<td>yes</td>
<td>no</td>
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Kattamis A.Z., Princeton University

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<tr>
<th>Property</th>
<th>Steel Foil</th>
<th>Plastic Foil</th>
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<tbody>
<tr>
<td>Process Temperature</td>
<td>up to ~1000°C</td>
<td>&lt; 280°C</td>
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$\frac{I_{on}}{I_{off}} > 10^7$, $\mu_{lin} \sim 0.45 \text{ cm}^2/\text{Vs}$, $V_T \sim 2 \text{ V}$

Acceptable TFT performance, but …

Bias-stress instability of a-Si:H TFTs

Stress time: 600 sec
Initial
After stress of $V_g = 20$ V

a-Si TFT stability rises with process temperature

⇒ Must make a-Si:H TFTs at high process temperature

α-Si:H TFTs made on clear plastic at 280°C

Cherenack K., Princeton University
\( \Delta V_T \) depends only on process T, not on substrate material

Steel versus plastic

- Polymer foil substrate
- Steel foil substrate

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<tr>
<td>Substrate stiffness affects dimensional stability</td>
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<tr>
<td>------------------------------------------------</td>
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<tr>
<td>$Y_s \cdot d_s$ versus $Y_f \cdot d_f$</td>
<td>thin film (small $d_f$)</td>
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<tr>
<td>stiff (large $Y_f$)</td>
<td>compliant (small $Y_f$)</td>
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<td>poly-Si TFT / steel substrate</td>
<td>OLED / steel substrate</td>
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<tr>
<td>stiff (large $Y_s$)</td>
<td>$Y_s \cdot d_s \gg Y_f \cdot d_f$</td>
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<tr>
<td>thick substrate (large $d_s$)</td>
<td>$Y_s \cdot d_s \gg Y_f \cdot d_f$</td>
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<td>compliant (small $Y_s$)</td>
<td>$Y_s \cdot d_s \approx Y_f \cdot d_f$</td>
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<td>a-Si TFT / polymer substrate</td>
<td>OTFT / polymer substrate</td>
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<tr>
<td>Gleskova H., Princeton University</td>
<td>Jackson T., Penn State Univ.</td>
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**a-Si:H TFT process**

1. Front SiN\textsubscript{x} passivation
2. Back SiN\textsubscript{x} passivation
3. Cr gate metal deposition
4. Cr gate patterning - **mask 1**

5. PECVD TFT stack: 5 W SiN$_x$
   (i) a-Si:H
   (n$^+$) a-Si:H

6. Cr S/D deposition

7. S/D patterning – **mask 2**

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Location of alignment marks

feature of mask 1: bottom gate metal layer

feature of mask 2: S/D layer

5W gate SiN$_x$

Average shrinkage ~ 500 ppm

12W gate SiN<sub>x</sub>

Average change ~ 100 ppm

Film grown on foil substrate at elevated temperature

Substrate at room temperature $T_r$

Substrate at deposition temperature $T_d$

Free-standing film at $T_d$

Workpiece at $T_d$ after film growth

Film and substrate at $T_r$ if they were separated

Workpiece at $T_r$ when held flat

$$
\varepsilon_s(T_r) = \left[ \left( \alpha_f - \alpha_s \right) \cdot (T_r - T_d) + \varepsilon_{bi} \right] \frac{Y_s d_s}{1 + \frac{Y_f d_f}{Y_f d_f}}
$$

$$
\nu_f = \nu_s
$$


Film release from the substrate holder

Workpiece at $T_r$ when held flat

Workpiece at $T_r$ when released from the substrate holder

SiN$_x$

Bare 8 19 24 40 mW/cm$^2$

\[
R = \frac{d_s}{6 \frac{Y_f d_f}{Y_s d_s} (1 + \nu) \left[ (\alpha_f - \alpha_s) \cdot (T_r - T_d) + \varepsilon_{bi} \right]} \cdot \frac{\left( 1 - \frac{Y_f d_f^2}{Y_s d_s^2} \right)^2}{\left( 1 + \frac{d_f}{d_s} \right) \left( 1 + \frac{d_f}{d_s} \right)^2} + 4 \frac{Y_f d_f}{Y_s d_s} \left( 1 + \frac{d_f}{d_s} \right)^2
\]


Steel foil

A rigid substrate foil is not changed much by CTE mismatch
Possible to maintain reasonable overlay accuracy

Stress built into the Si$_{N_x}$ can compensate thermal mismatch and eliminate curvature and misalignment.

Kapton foil

Summary

• Higher deposition temperatures needed for good TFT stability

• Deposition at elevated temperature changes in-plane dimensions

• Changes are small if \( \frac{d_f}{d_s} \leq 0.05 \) (steel) or \( \frac{d_f}{d_s} \leq 0.001 \) (Kapton)

• CTE mismatch change in in-plane dimensions is
  \(~ 20 \text{ ppm for a-Si:H TFTs on 100-\textmu m steel foil}~\)
  \(~ 500 \text{ ppm for a-Si:H TFTs on 100-\textmu m Kapton foil}~\)

• Tailor built-in stress in the film to compensate CTE mismatch
  \( \Rightarrow \) possible to eliminate misalignment
  \( \Rightarrow \) possible to eliminate curvature of the workpiece