Low Frequency Noise in Advanced MOS Transistors

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Motivation

- CMOS scaling

Low Frequency Noise becomes important!

Happy days of scaling

It’s ok.

It’s noisy.

“African Elephant”

“Elephant mouse”

IEDM 2008 short course

Year of production
Motivation

• Low Frequency (LF) noise
Outline

- Introduction
- Methodology
- SiGe channel
- Size effect
- Conclusions
Outline

• **Introduction**
  - Why LF noise is important?
  - The origin of LF noise
  - CMOS scaling

• **Methodology**

• **SiGe channel**

• **Size effect**

• **Conclusions**
Why LF noise is important?

- **Noise in a MOSFET**

  - **White noise**: thermal noise and shot noise.
  - **1/f noise**: certain trap distribution or fluctuation in mobility.
  - **G-R noise**: trap/de-trap mechanism; one special case is **RTN**.

![Graph showing LF noise](image)
Why LF noise is important?

• Analog domain

- LF noise is up-converted and causes phase noise.
- Phase noise limits channel capacity.
Why LF noise is important?

- Digital domain

- LF noise increases with scaling.
- Noise margin becomes small.

Outline

- **Introduction**
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  - The origin of LF noise
  - CMOS scaling
- **Methodology**
- **SiGe channel**
- **Size effect**
- **Conclusions**
The origin of LF noise

• Two schools

\[ \sigma = \mu_{\text{eff}} N \]

– Conductivity fluctuation.

– Two schools: number fluctuations (\(\Delta N\)) and mobility fluctuations (\(\Delta \mu\)).
The origin of LF noise

- \( \Delta N \) model: one trap

Random telegraph noise


Surface effect

Lorentzian

\( \tau_h \)

\( \tau_i \)

\( \Delta I \)
The origin of LF noise

- $\Delta N$ model: a lot of traps

\[ \Delta \mu \text{ is also induced.} \]

The origin of LF noise

• ΔN model: a lot of traps

- Sum of Lorentzians: $1/f$ noise
The origin of LF noise

- **ΔN model:** $I_d$ and $V_g$ dependence

\[ \frac{S_{id}}{I_d^2} \propto \frac{(g_m/I_d)^2}{(1/\text{Hz})}. \]

Fix $V_d$ and increase $V_g$:

- $I_d$: $S_{id}/I_d^2 \propto (g_m/I_d)^2$.
- $V_g$: flat in weak inversion.
The origin of LF noise

- **Δμ model**
  - Bulk phonon scattering
  - Empirical equation

\[
\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{WLQ_i f}
\]

T-ED 1994, F. N. Hooge
The origin of LF noise

- **Δμ model:** $I_d$ and $V_g$ dependence

\[
\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{W L Q_i f}
\]

- $I_d$: $S_{id}/I_d^2 \propto 1/I_d$.
- $V_g$: $S_{id}/I_d^2$ increases when $V_g$ decreases.
The origin of LF noise

- $\Delta N$ or $\Delta \mu$?

![Graph showing the relationship between $S_{id}/I_d^2$ (A²/Hz) and Drain current (A) with two lines for number fluct. and mobility fluct.](image1)

![Graph showing the relationship between $S_{id}/I_d^2$ (A²/Hz) and Gate voltage (V) with two lines for $\Delta N$ and $\Delta \mu$.](image2)

- Different trend in $I_d$ and $V_g$ dependence.

Outline

• Introduction
  ▪ Why LF noise is important?
  ▪ The origin of LF noise
  ▪ CMOS Scaling

• Methodology
• SiGe channel
• Size effect
• Conclusions
CMOS scaling: provide new opportunity to optimize LF noise.
Outline

• Introduction
• Methodology
  ▪ Overview
  ▪ TCAD simulations
  ▪ Noise characterization
• SiGe channel
• Size effect
• Conclusions
Overview

TCAD simulations

Explain low frequency noise mechanism

Noise characterization

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Outline

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$S_{id\_total} = S_{id\_\Delta N} + S_{id\_\Delta \mu}$

- Total noise is the sum of $\Delta N$ and $\Delta \mu$.
- No correlation.
**TCAD simulation**

- **Impedance field method (IMF)**

  \[ Z_{kr} = \frac{\text{Voltage fluctuation at kth electrode}}{\text{Injected current at r in the device}} \]

• Impedance field method (IFM)
• $\Delta N$ model

- Noise source is inside oxide.
- A rate equation to correlate oxide traps and channel carriers and then apply IMF to calculate $S_{id}$. 

TCAD simulation
• $\Delta \mu$ model

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{W L Q_i f}$$

Extract from TCAD

- Extract parameters from TCAD simulations such as $Q_i$. 

IEEE T-ED 2008, C.-Y. Chen
Noise characterization

- **Basic schematic**

  ![Schematic Diagram]

  - Offset current removes the DC component at the input.
  - SR570 is used to drive high impedance loads and input impedance of signal analyzer should be high.


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Noise characterization

• Measurement bench

- SR 570
- SR760 FFT spectrum analyzer
- Wafer (DUT)
- Drain
- Gate
- Source
- Bulk
- Cascade probe station
- HP4156
Outline

• Introduction
• Methodology
• SiGe channel
  ▪ Device schematic
  ▪ Gate bias
  ▪ Body bias
• Size effect
• Conclusions
• **Si/SiGe/Si p-HFET**

  ![Device schematic](image)

  - Two channels: SiGe buried channel and parasitic surface channel.

  **Parameters**:
  - L/W = 1um/10um
  - Oxide thickness = 6nm

  **Devices from Panasonic**
• Advantage

- Improve LF noise: (1) longer tunneling distance and (2) smaller Coulomb interaction.
Outline

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Gate bias

- Dual-channel behavior

When buried channel dominant LF noise is reduced.
Gate bias

- $V_g$ dependence

![Graph showing Gate Voltage (V) vs. $\Delta N$ and $\Delta \mu$](image)

- Weak inversion: $\Delta \mu$
- Medium/strong inversion: $\Delta N$
Gate bias

- $I_d$ dependence

![Graph showing $\Delta \mu$ and $\Delta N$]

- Weak inversion: $\Delta \mu$
- Medium/strong inversion: $\Delta N$
Outline

• Introduction
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Body bias

- SiGe p-HFET

LF noise in SiGe p-HFET has strong body bias dependence.

SISPAD 2007, C.-Y. Chen
Body bias

- SiGe p-HFET

- Body bias changes carrier distribution in dual channels
Body bias

- SiGe p-HFET

- FL noise is mainly from surface channel.
Body bias

- Si p-FET

- Si p-MOS does not show body bias dependence.
Outline

• Introduction
• Methodology
• SiGe channel
• Size effect
  ▪ Device schematic
  ▪ Mechanism
  ▪ Gate bias

• Conclusions
• Scaled MOSFETs (small gate area)

- Only a few traps are involved.
- $\Delta N$ predicts RTN; $\Delta \mu$ shows 1/f noise.
Outline

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  ▪ Mechanism
  ▪ Gate bias

• Conclusions
Mechanism

- **Ig- / Id-RTN**

  - A few trap/de-trap

  - Two types: Ig-RTN and Id-RTN.
• Where are traps?

- Traps should be inside high-κ oxide.
Mechanism

- **Trap/de-trap**

  - Capture: $V_{th}$ and TAT increase $\Rightarrow I_d \downarrow$ and $I_g \uparrow$
  - Emission: $V_{th}$ and TAT decrease $\Rightarrow I_d \uparrow$ and $I_g \downarrow$
Mechanism

- PBTI and RTN

Consistent with RTN results.
Outline

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  ▪ Gate bias

• Conclusions
Gate bias

- $I_g$-RTN

$V_g$ increases: Time in high-$I_g$ state increases.
Gate bias

- **I\textsubscript{d}-RTN: Low V\textsubscript{g}**

Measurement still shows 1/f noise; \(\Delta\mu\) model is dominant.
Gate bias

- $I_d$-RTN: High gm bias condition

- RTN and Lorentzian shape are observed in high gm region.
Gate bias

- $I_d$-RTN: High $V_g$

- $1/f$ noise is shown in a very scaled MOSFET: $\Delta \mu$ is dominant.
• $I_d$-RTN: summary

- RTN should be considered especially in high gm region.
**Gate bias**

- $I_d$-RTN: summary

- RTN should be considered especially in high $gm$ region.
Outline

• Introduction
• The origin of LF noise
• Methodology
• SiGe channel
• Size effect
• Conclusions
  ▪ Summary
  ▪ Contributions
  ▪ Future work
## Summary

<table>
<thead>
<tr>
<th>Bias</th>
<th>SiGe H-MOS (Lg~1um)</th>
<th>Scaled MOS (Lg~40nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weak inversion</td>
<td>$\Delta \mu$ model is dominant.</td>
<td>$\Delta \mu$ model is dominant.</td>
</tr>
<tr>
<td>High gm region ($\sim V_{dd}/2$)</td>
<td>$\Delta N$ model is important; LF noise is mostly surface effect.</td>
<td>$\Delta N$ model becomes important; RTN should be considered.</td>
</tr>
<tr>
<td>High $V_g$ condition</td>
<td>$\Delta N$ is dominant in our device, but in general it can be technology dependence.</td>
<td>$\Delta \mu$ model is dominant</td>
</tr>
</tbody>
</table>
The origin of LF noise: (1) $\Delta N$ model and (2) $\Delta \mu$ model.

Methodology: TCAD simulations and noise measurements

SiGe channel: Dual-channel is important to explain the low frequency noise performance.

Size effect: $I_g$-RTN is directly related to physical trapping or de-trapping and the $I_d$-RTN reflects sensitivity to charge trapping as determined by $g_m$.

CMOS scaling: provides a new opportunity for LF noise study.
Contributions

- Detailed LF noise mechanisms in SiGe p-HFET are proposed.
- LF noise mechanisms in scaled MOSFETs are measured and analyzed.

- Other parts: (1) LF noise mechanisms in high-κ MOSFET, (2) A LF noise compact model in SiGe p-HFET, (3) linearity of asymmetric channel doping for LDMOS, (4) linearity in GaN HEMTs, and (5) asymmetric FET scaling.
Future work

Rethink “device noise” “distortion” and “reliability”
Publications

Backup: Linearity analysis of lateral channel doping in RF power MOSFETs

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• Introduction

• Quasi-1D structure

• Realistic LDMOS structure

• Conclusions
Linearity:

Low distortion is one of the most important concerns for wireless communication systems.

Analysis of the distortion generated by the device itself has been fairly limited.
Harmonic balance device simulations:

A unique harmonic balance (HB) device simulator with the capability of including external circuitry is used.

In the HB simulations, variations in device parameters are directly reflected in the final large signal RF performance.
Backup: Quasi-1D structure (1 of 3)

Device schematic:

0.5um gate length, 30nm oxide thickness.

Avoid 2D-effects.

Very high source and drain dopings to avoid compensation effects at source and drain junctions.

4 cases: 2 uniform doping and 2 laterally graded.

Test circuit consisting of bias feeds and blocking capacitors on input and output.
Different \( gm_3/gm \) magnitudes for different cases.

Devices were biased at \( gm_3/gm \) minima, close to overall best linearity.

First data point correlates to magnitude of \( gm_3/gm \) minima.

Shorter char. length / lower uniform doping: higher IM3 at low input power lower IM3 at high input power.
Field distribution:

- Graded cases $\rightarrow$ more uniform field.
- Smaller uniform doping $\rightarrow$ more uniform field.
- Uniform lateral field $\rightarrow$ better linearity at higher power.
Device schematic (based on Infineon 7th generation design):

Two different lightly doped drain regions: optimize on-resistance and breakdown voltage.

Source doping and lightly doped drain kept the same for all cases.

Four different lateral grading cases in channel, defined through analytical expressions.
Backup: Realistic LDMOS (2 of 4)

**gm3/gm:**

![Graph showing gm3/gm vs. gate voltage for different channel lengths.]

- Bias-point at gm3/gm minima.

**Test circuitry:**

- Circuitry with internal and external matching and bias.
- Infineon product PTF210451.
Effect of graded doping is significant → the nonlinearities in capacitances will not swamp the studied effects at high frequency.

More graded channel profile shows better linearity in the intermediate power regime.
Vgs shifts from gm3/gm:

Vgs shifts from gm3/gm minima → IM3 change is quite sensitive.

Different device designs give different IM3 that cannot be compensated for by simply changing Vgs bias (Idq setting).
• A graded channel has better linearity for intermediate to high powers. By contrast, for increased back-off, the situation is reversed.

• Nonlinearities in intrinsic capacitances will not swamp the effect of graded channel doping at high frequency.

• The effect of graded channel doping cannot be fully compensated for by adjusting the Idq bias point.

• The analysis lays ground-work for RF device optimization for improved linearity.
Quasi-1D structure: \( \text{IdVgs} \)

Clearly different \( \text{gm3/gm} \) magnitudes for different cases. Shorter characteristic length and lower doping give larger \( \text{gm3/gm} \) magnitudes.

Devices were biased at \( \text{gm3/gm} \) minima, close to overall best linearity for many applications.
Quasi-1D structure: velocity saturation:

When Vsat model is not included:
1. $gm_3/gm$ shifts to a smaller magnitude.
2. IM3 is much lower, both initially and for high powers.
First, separate nonlinearities in static IV from capacitive effects $\rightarrow$ low freq. 10MHz.

More graded channel profile shows better linearity in intermediate power regime.
At high power, the compressing non-linearity along the load-line will dominate; the curves merge. Lower $V_{gs}$ → two sweet-spots appear.
Backup: GaN HEMT structure

Lg=0.5\,\text{um}
Backup: Id-Vgs, GaN HEMT

TCAD simulation results

![Graph showing TCAD simulation results for GaN HEMT with and without hydrodynamics.](image)
Backup: Gm3/Gm1, GaN HEMT

Gm3/Gm1 min.: Vg = -4.9047 V

Graph showing the comparison of Gm3/Gm1 without and with hydrodynamics.
Backup: Linearity, GaN HEMT

GaN HEMT
Vd=28V
Vg=-4.91V (Gm3/Gm1 min.)
Backup: The origin of LF noise

- $\Delta N$ model

- One trap $\rightarrow$ RTN

- A lot of traps $\rightarrow$ $1/f$ noise

- Time:

- Frequency:

- Frequency:

- Time:

- Frequency:

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About 12% MOSFETs show RTN: 9% $I_g$-RTN, 2% $I_d$-RTN, and 1% $I_g$/$I_d$-RTN.

The statistical results are from 1000 devices with the same technology and structures.
- $I_g$ increases: Time in high-$I_g$ state increases.
Backup: TCAD

- $I_d$-RTN: High $gm$ bias condition
  
  TCAD simulations confirm the origin of RTN can be from one-trap/de-trap.
Noise: key issue for the future electronic system development.
Space: from gate to Si can be low-high or high-low.

Energy: distribution is a U-shape in log-scale.


- $V_g$ dependence shows flat region in weak inversion regime.

- In the U-shape distribution $V_g$ dependence is less sensitive compared with uniform distribution.


Backup: Numerical method (1 of 2)

- Physical model

\[ S_{nt}(\vec{r}) = 2(G + R) \]
\[ \frac{dn_t}{dt} = G - R \]
\[ = \left[ \frac{(N_T - n_t)}{\tau} - n_t \exp\left(\frac{E_T - E_F}{k_B T}\right) \right] / \tau \]

- Impedance field method (IMF)

\[ A_k(\vec{r}) = \frac{\text{Current fluctuation at kth electrode}}{\text{Injected current at } \vec{r} \text{ in the device}} \]
\[ S = \int |A(\vec{r})|^2 S_{in}(\vec{r}) \, dv \]


• Hooge mobility fluctuation ($\Delta \mu$ model)
  – Bulk phonon scattering

  – Empirical equation

  \[
  \frac{S_{I_D}}{I_D^2} = \frac{q\alpha_H}{W_L Q_i f}
  \]

  – Numerical approach: Post process

  Hooge model is empirical $\rightarrow$ the post process with simulated parameters/reasonable $\alpha_H$ is used.

The fluctuating oxide charge density $\Delta Q_{ox}$ is equivalent to a variation in the flat-band voltage

$$\delta V_{fb} = -\Delta Q_{ox} / C_{ox}$$

The fluctuation in the drain current yields

$$\delta I_D = \frac{\partial I_D}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_D}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \Delta Q_{ox}$$

$$S_{I_D} = S_{V_{fb}} \left( 1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m} \right)^2 g_m^2$$

- The first term in the parentheses is due to fluctuating number of inversion carriers and the second term to correlated mobility fluctuations.
The power spectral density of the flat-band voltage fluctuations is calculated by summing the contributions from all traps in the gate oxide.

\[
S_{Q_{ox}} = S_{V_{fb}} C_{ox}^2 = \frac{q^2}{W^2 L^2} \int_{E_v}^{E_c} \int_0^W \int_0^L 4N \left( f(E)(1-f(E)) \right) \frac{\tau}{1+(2\pi f \tau)^2} dx dy dz dE
\]
The product $f(E)(1-f(E))$ is sharply peaked around the quasi-Fermi level.

If the Fermi-level is far above or below the trap level, the trap will be filled or empty.
Backup: Unified model (4 of 4)

\[ S_{Q_{ox}} = \frac{q^2 kT}{WL} \int_0^{t_{ex}} 4N_t \frac{\tau}{1 + (2\pi f \tau)^2} \, dz \]

Lorentzian spectrum

The trapping time constant (quantum tunneling)

\[ \tau = \tau_0 (E) \cdot e^{z/\lambda} \]

Tunneling attenuation length

\[ S_{V_{fb}} = \frac{q^2 kT \lambda N_t}{f^\gamma WL C_{ox}^2} \]

\[ S_{I_D} = S_{V_{fb}} \left( 1 + \frac{\alpha \mu_{\text{eff}} C_{ox} I_D}{g_m} \right)^2 g_m^2 \]
• Numerical approach

Different affinities and tunneling are considered →

\[ \gamma = \frac{4\pi}{\hbar} \sqrt{2m^{*}\Phi} \quad \tau = \tau_{0}(E) \cdot e^{-\frac{\lambda}{\gamma}} \]

\[ \text{SiO}_2: 1 \times 10^{-8} \text{ cm} \]

\[ \text{HfO}_2: 2.1 \times 10^{-8} \text{ cm} \]

• Scaling trend: general trend

- SiO$_2$ trap density is much smaller than that of HfO$_2$.
- $1/f$ noise increases much faster than the thermal noise when size scales down.
• Scaling trend: traps at gate edge

- High trap density in the gate edge region.
- In the scaled devices traps in the gate edge becomes important so $S_i/L_d^2$ increases significantly.

$S_i/I_d^2 \propto N_t$

$N_{t,HfSiON} = (2 \times N_e \times L_e + N_c \times L_c)/L_g$

Halo doping profiles → suppress the short channel effect.

The same amount of electrons → greater $\Delta I_d$ in halo.

Reduced inversion carrier density in the halo regions.

- The lowering of the $1/f$ noise: observed in the strong inversion regime.

- Traps and charges at the gate dielectric interface: better screened by a metal gate→alleviate remote phonon scattering.

• Dual channel behavior
  – Surface and buried channels have different Coulomb interactions.
  – Both channels also have different material quality.

\[
\eta = \left(1 + \mu \sqrt{\frac{n_{2-D}}{\mu c_0}}\right)^2
\]

\[
\eta = \left(1 + \mu \sqrt{\frac{n_{3-D}}{\mu c_0}}\right)^2
\]

\[
\frac{S_{id}}{I_d^2} = \left( \frac{q\alpha_{cap}}{WLQ_{cap} f} \frac{I_{d_{cap}}^2}{I_d^2} + \frac{q\alpha_{SiGe}}{WLQ_{SiGe} f} \frac{I_{d_{SiGe}}^2}{I_d^2} \right)
\]

\[\text{SiGe p-HMOS} \quad \text{Vd= -0.1V} \]

- w/o layer dependence
- This work
- Measurements


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Compact model

- Physics based compact model can simulate dual-channel behavior for SiGe FETs.

SiGe p-HMOS
Vd=-0.1V

<table>
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<tr>
<th>SID/ID^2 (1/Hz)</th>
<th>TCAD</th>
<th>Proposed model</th>
<th>Measurements</th>
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</thead>
<tbody>
<tr>
<td>Vg(V)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SiGe p-HMOS
Si p-MOS

10^2 10^3 10^4 10^5 10^6

Frequency (Hz)

10^3

Vg(V)
• Exponential tail in RTN

- The slope of $V_{th}$ instability shows an exponential tail.
- The slope increases with technology scaling.

Backup: Random Telegraph Noise (2 of 2)

- **Body bias dependence**: explain

- **RTN**: channel/gate dielectrics system in dynamic equilibrium.
- **NBTI relaxation**: perturbed system returning to the equilibrium.
Backup: Switched bias

- Switched MOS

- Large switch in gate can reduce 1/f noise.

Backup: Temperature effect

- **RTN**

- **1/f noise**

![Graph showing temperature effect on noise]

\[ S_{1f} (A^2/Hz) \]

\[ f=14Hz \quad V_{gs}=2.5V \]

\[ V_{dd} 4.0V \quad V_{dd} 2.5V \]

\[ T=300K \]

\[ T=281K \]

\[ T=257K \]

\[ T=236K \]

\[ \text{Temperature (K)} \]

\[ 10^{-17} \]

\[ 280 \quad 320 \quad 360 \quad 400 \quad 440 \]

\[ 1.2um \]

\[ [20] \text{M. J. Deen et al. AIR conf. vol. 282, pp. 165-188, 1992.} \]

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Backup: 1/f noise characterization (1 of 4)

- **SR 570 settings**
  - The sensitivity is 2uA/V
  - High bandwidth mode is used.

- **Noise floor ~ 10^{-10}Amps/rootHz**
- **Bandwidth ~ 1MHz**
SR 760 settings

- Impedance ~ 1MΩ, 15pF
- Bandwidth: DC to 100kHz
- The bandwidth of noise measurement is limited by SR760.
- Good for very low frequency measurements.
Backup: 1/f noise characterization (3 of 4)

- **HP4396A**
  - Impedance ~ 50Ω.
  - Bandwidth: 2Hz to 1.8GHz
  - Easy interface and high resolution.

- **Active probe HP41800A**
  - Impedance ~ 1MΩ.
  - Bandwidth: 5Hz to 500MHz
  - Convert high impedance to 50 Ω.
Backup: 1/f noise characterization (4 of 4)

- On-package measurements

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DC Power Supply

Low noise current amplifier: SR570

D.U.T. PCB and low loss filter

Connect

Spectrum Analyzer: HP4396A

Active Probe: HP41800A

Connect

D.U.T.